AN159

# Application Note

# PLL FILTER OPTIMIZATION FOR THE CS8415A, CS8420, AND CS8427

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## 1. INTRODUCTION

The purpose of this application note is to give users of the CS8415A, CS8420, and CS8427 the information needed to optimize the performance of the Phase-Locked Loop for their requirements. Equations are provided to determine the filter values when driving the PLL from the AES Receiver or from the Serial Input Port.

The PLL design of the CS8415A, CS8420, and CS8427 is different from that of the CS8411/12 and CS8413/14. The filter values computed by the equations in this applications note are not applicable to the older devices. The sections on capacitor choice and board layout are applicable to both the old and the new parts.

## 2. PLL SYSTEM PARAMETERS

Figure 1 is a simplified diagram of the PLL in these parts. When the PLL is locked to an AES3 input stream, it is updated at each preamble in the AES3 stream. This occurs at twice the sampling frequency, $F_S$. When the PLL is locked to ILRCK, it is updated at $F_S$ so that the duty cycle of the input doesn't affect jitter.

The following operating parameters of the PLL system are used in the filter calculations:

VCO Gain: $K_{VCO}$ = 4 MHz/V

Charge Pump Current: $I_{CP}$ = 300 µA

Divider for AES3: N = 128

Divider for ILRCK: N = 256

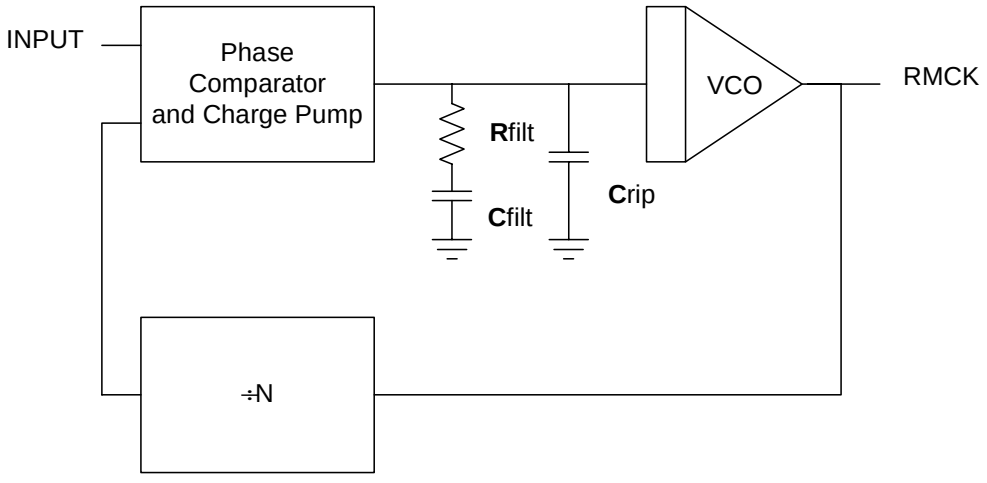


**Figure 1. PLL Block Diagram**

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## 3. CAPACITOR CHOICE

Users frequently ask what capacitors to select for the PLL filter. Large or exotic film capacitors are not necessary. Their leads and the longer circuit board traces they require add undesirable inductance to the circuit. Surface mount ceramic capacitors are a good choice because their own inductance is low, and they can be mounted close to the FILT pin to minimize trace inductance. For $C_{RIP}$, a C0G or NPO dielectric is recommended, and for $C_{FILT}$, an X7R dielectric is preferred. Avoid capacitors with large temperature co-efficients, or capacitors with high dielectric constants, that are sensitive to shock and vibration. These include the Z5U and Y5V dialectrics.

## 4. BOARD LAYOUT

Board layout and capacitor choice affect each other and determine the performance of the PLL. Figure 2 contains a suggested layout for the PLL filter components and for bypassing the analog supply voltage. The 0.1 µF bypass capacitor is in a 1206 form factor. $R_{FILT}$ and the other three capacitors are in an 0805 form factor. The traces are on the top surface of the board with the IC so that there is no via inductance. The traces themselves are short to minimize the inductance in the filter path. The VA+ and AGND traces extend back to their origin and are shown only in truncated form in the drawing.

## 5. PLL DESIGN EQUATIONS

The following equations provide a loop phase margin of 60º. This has been tested in the lab and found to be optimum. It gives the best performance in tolerating jitter on the incoming signal and maximizes DAC THD+N performance. Jitter transfer function peaking is 0.74 dB with the given equations (EQ1, EQ2, EQ3, EQ4, EQ6, and EQ8). The AES3 standard permits a maximum jitter peaking of 2 dB. The IEC60958 consumer specification allows a maximum of 3 dB of jitter peaking.

To use the design equations, first determine the minimum sample frequency that the PLL will have to lock to.

If you are using only the AES receiver use the equations in the AES3 design example.

If you are using the Input Serial Port or the Input Serial Port and the AES Receiver, use the equations in the Serial Input Port design example.

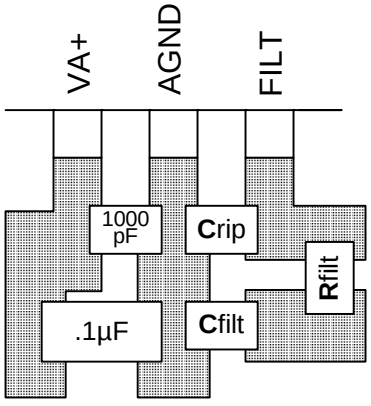


**Figure 2. Recommended Layout Example**

## 5.1 AES3 Design Example

Assume an application in which the incoming AES3 stream may have a sample rate from 32 kHz to 96 kHz. Using the minimum $F_S$ of 32 kHz, the following can be computed:

$$f_{pole} = \frac{f_s}{2} = \frac{32000}{2} = 16000 \quad \text{EQ 1}$$

$$f_{lpbw} = \frac{f_s}{4} = \frac{32000}{4} = 8000 \quad \text{EQ 2}$$

$$f_{zero} = \frac{f_s}{80} = \frac{32000}{80} = 400 \quad \text{EQ 3}$$

With these values the filter components can then be determined.

$$\frac{2\pi \cdot N \cdot f_{lpbw}}{I_{CP} \cdot K_{VCO}} = R_{FILT} \quad \text{EQ 4}$$

$$\frac{2\pi \cdot 128 \cdot 8000}{300\times10^{-6} \cdot 4\times10^{6}} = 5362 \quad \text{EQ 5}$$

Select $R_{FILT}$ = 5100 Ohms, the nearest standard 5% value.

$$\frac{1}{2\pi \cdot R_{FILT} \cdot f_{zero}} = C_{FILT} \quad \text{EQ 6}$$

$$\frac{1}{2\pi \cdot 5100 \cdot 400} = 0.078\times10^{-6} \quad \text{EQ 7}$$

Select $C_{FILT}$ = 0.082 µF, the nearest standard value.

$$\frac{1}{2\pi \cdot R_{FILT} \cdot f_{pole}} = C_{RIP} \quad \text{EQ 8}$$

$$\frac{1}{2\pi \cdot 5100 \cdot 16000} = 1.95\times10^{-9} \quad \text{EQ 9}$$

Select $C_{RIP}$ = 2.2 nF, the nearest standard value.

| $F_s$ | $R_{FILT}$ | $C_{FILT}$ | $C_{RIP}$ |
|---|---|---|---|
| **96 kHz** | 16k Ω | 8.2 nF | 220 pF |
| **88.2 kHz** | 15k Ω | .01 F | 270 pF |
| **48 kHz** | 8.2k Ω | .033 µF | 820 pF |
| **44.1 kHz** | 7.5k Ω | .039 µF | 1000 pF |
| **32 kHz** | 5.1k Ω | .082 µF | 2200 pF |
| **24 kHz** | 3.9k Ω | .15 µF | 3900 pF |
| **16 kHz** | 2.7k Ω | .33 µF | 8200 pF |
| **8 kHz** | 1.3k Ω | 1.2 µF | .033 µF |

**Table 1. Pre-computed values for operation from an AES3 input**

## 5.2 Serial Input Port Design Example

Assume an application in which the Input Serial Port is driven at a sample rate of 32 kHz. The following can be computed:

$$f_{pole} = \frac{f_s}{4} = \frac{32000}{4} = 8000 \qquad \text{EQ 10}$$

$$f_{lpbw} = \frac{f_s}{8} = \frac{32000}{8} = 4000 \qquad \text{EQ 11}$$

$$f_{zero} = \frac{f_s}{160} = \frac{32000}{160} = 200 \qquad \text{EQ 12}$$

With these values the filter components can then be determined.

$$\frac{2\pi \cdot N \cdot f_{lpbw}}{I_{CP} \cdot K_{VCO}} = R_{FILT} \qquad \text{EQ 13}$$

$$\frac{2\pi \cdot 256 \cdot 4000}{300\times10^{-6} \cdot 4\times10^{6}} = 5362 \qquad \text{EQ 14}$$

Select $R_{FILT}$ = 5100 Ohms, the nearest standard 5% value.

$$\frac{1}{2\pi \cdot R_{FILT} \cdot f_{zero}} = C_{FILT} \qquad \text{EQ 15}$$

$$\frac{1}{2\pi \cdot 5100 \cdot 200} = 0.156\times10^{-6} \qquad \text{EQ 16}$$

Select $C_{FILT}$ = 0.15 µF, the nearest standard value.

$$\frac{1}{2\pi \cdot R_{FILT} \cdot f_{pole}} = C_{RIP} \qquad \text{EQ 17}$$

$$\frac{1}{2\pi \cdot 5100 \cdot 8000} = 3.90\times10^{-9} \qquad \text{EQ 18}$$

Select $C_{RIP}$ = 3.9 nF, the nearest standard value.

| $F_s$ | $R_{FILT}$ | $C_{FILT}$ | $C_{RIP}$ |
|---|---|---|---|
| **96 kHz** | 16k Ω | .018 µF | 390 pF |
| **88.2 kHz** | 15k Ω | .022 µF | 560 pF |
| **48 kHz** | 8.2k Ω | .068 µF | 1800 pF |
| **44.1 kHz** | 7.5k Ω | .082 µF | 2200 pF |
| **32 kHz** | 5.1k Ω | .15 µF | 3900 pF |
| **24 kHz** | 3.9k Ω | .27 µF | 6800 pF |
| **16 kHz** | 2.7k Ω | .68 µF | .015 µF |
| **8 kHz** | 1.3k Ω | 2.7 µF | .062 µF |

**Table 2. Pre-computed values for operation from ILRCK or from ILRCK and AES3**

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