# Application Note

# A Collection of Bridge Transducer Digitizer Circuits

by
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## Introduction

Bridge transducers are common in instrumentation. This application note illustrates some bridge transducer digitizer circuits which use the CS5504/5/6/7/8/9 A/D converters and the CS5516/20 A/D converters.

The CS5504/5/6/7/8 converters can be operated with a variety of power supply arrangements; including operating from a single +5 V supply; operating from +5 and -5 analog supplies with +3.3 V or +5 V on the digital supply; or operating with an analog supply from +5 to +11 V and a digital supply of +5 V.

The CS5509 can operate with +5 V on its analog and digital supplies; or with +5 V analog and +3.3 V digital.

The CS5516 and CS5520 are A/D converters optimized for bridge transducer applications and are designed to operate from +5 and -5 V supplies. Several circuits which utilize these ADCs will be presented.

The application note is divided into two sections:

1. DC-excited bridge circuits.
2. AC-excited bridge circuits with a discussion of the benefits of AC excitation.

## Bridge Transducers

Bridge transducers are manufactured with various technologies. The strain-sensing elements which make up the bridge may be made of diffused silicon, bonded silicon bars, deposited thin film, or bonded foil materials. The choice of technology will determine the performance of the transducer, including the sensitivity, the linearity, and the thermal stability. Silicon-based gages have good linearity with sensitivities between 3 mV/V and 20 mV/V, but tend to exhibit more drift as temperature changes. Metal foil or thin film gages have good linearity with sensitivities between 1 mV/V and 4 mV/V. Precision bridge transducers include some type of temperature compensation as part of the bridge.

Most bridge circuits are excited with a dc voltage, 10 volts being very common. With 10 V excitation, the full scale signals from the various transducers, can be as low as 10 mV to as high as several hundred millivolts. When digitizing these signals to high resolution (for discussion in this application note, high resolution means greater than 10,000 counts), one count can represent a very small voltage. It can be difficult to amplify and digitize these low level bridge transducer signals. Measurement performance can be hindered by such things as amplifier

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offset drift, amplifier noise (both thermal and 1/f), amplifier finite open loop gain, and parasitic thermocouples. Parasitic thermocouples are introduced any time two dissimilar metals are connected. For example, using tin-lead solder to solder a wire to a copper PC trace can introduce an unwanted thermocouple junction which changes as much as 3 µV/°C when subjected to temperature gradients.

This application note will introduce some A/D converter circuits which illustrate a number of application ideas to the design engineer who uses bridge transducers. In the AC-excited bridge section, a number of design ideas will be introduced which offer very good solutions to some of the problems encountered in low level bridge measurement.

## DC-EXCITED BRIDGE CIRCUITS

### CS5507,8,9 Bridge Transducer Operating From a Single +5 V Supply, or with the Analog Supply at +5 V and Digital Supply at +3.3 V

Figure 1 illustrates the low cost CS5509 16-bit converter operating from +5 V. The A/D can operate in either unipolar or bipolar mode and yields 20 conversions/second when running from a low cost 32.768 kHz crystal. When operated at 32.768 kHz the digital filter in the converter notches out 50 and 60 Hz line interference.

The LTC1051 dual chopper amplifier is used as the bridge amplifier. Bandwidth is limited to about 3.8 Hz by the 100k and 0.47 µF feedback

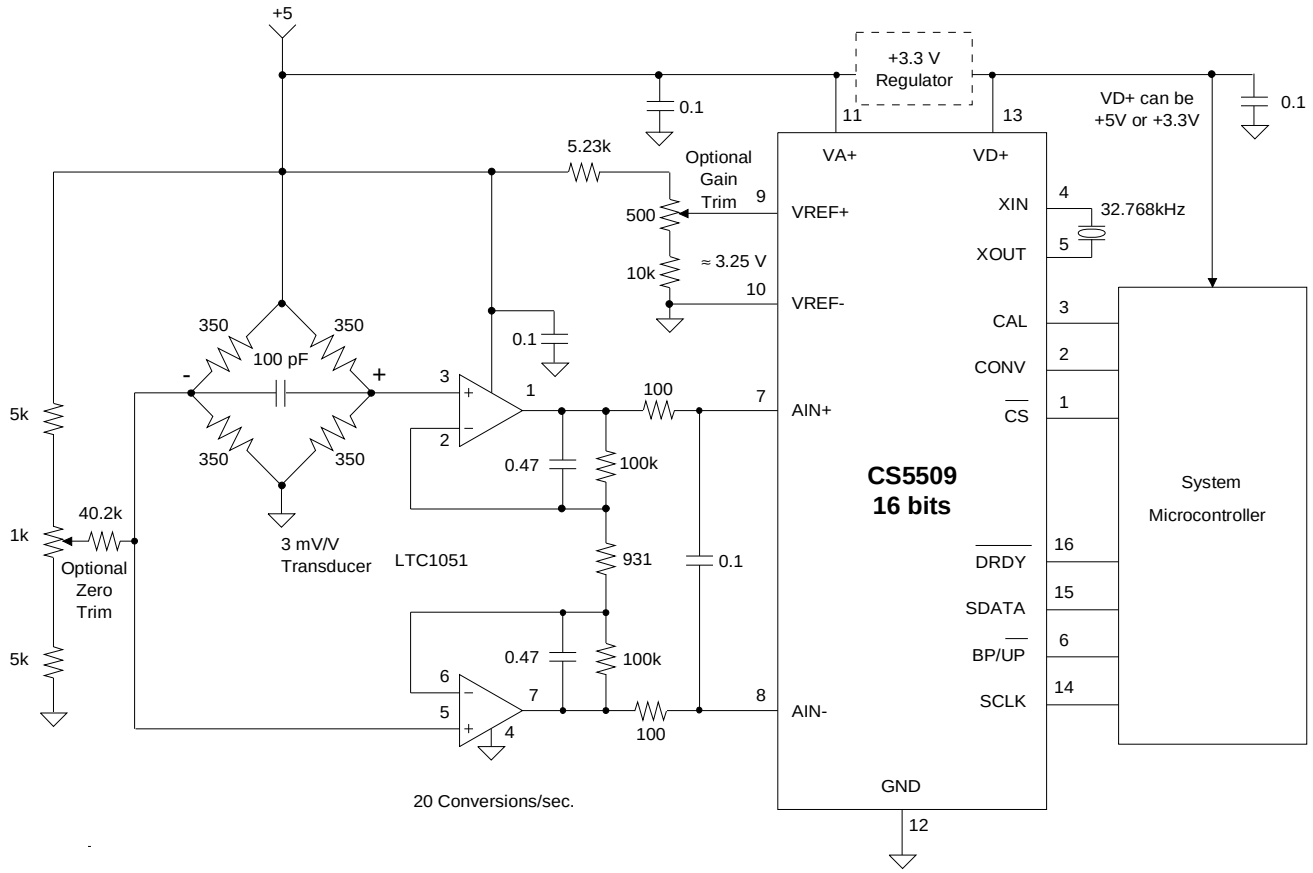



**Figure 1. CS5507,8,9 Bridge Transducer Operating from a Single +5 V Supply, or with the Analog Supply at +5 V and Digital Supply at +3.3 V.**

elements of the amplifier stage. Note that an instrumentation amplifier is not needed because the A/D input is fully differential. The dual amplifier functions as a differential in, differential out amplifier. The circuit yields about 9000 noise-free counts when measuring unipolar signals. Averaging 10 samples increases this to about 28,500 noise-free counts. "Noise-free counts" means full scale signal divided by six times the rms noise. Noise-free counts is good figure of merit for comparing A/D converters used in dc measurement applications. There is more discussion on this topic at the end of the application note.

The circuit illustrated uses a 3 mV/V transducer excited with +5 V for a full scale transducer output of 15 mV. The transducer output is amplified with a gain of about 216 to yield 3.25 V full scale. A dual stage amplifier, as shown in Figure 2 may be preferred to minimize errors due to limited loop gain. The A/D is operated in bipolar mode to achieve more µV/LSB. The reference voltage for the converter is derived from the +5 V excitation voltage. The measurement remains ratiometric should the +5 V excitation change.

Figure 1 includes potentiometers for offset and gain adjustment, as do a number of other circuits in this application note. Many system designers prefer to eliminate potentiometers and do all offset and gain correction in software. To achieve this in some of the circuits may require changes to gain stages or voltage references, but potentiometers are shown for all the engineers who are more comfortable with screwdrivers than software.

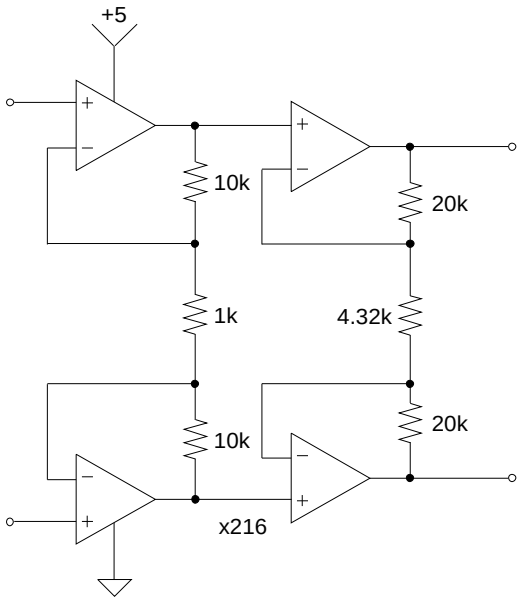
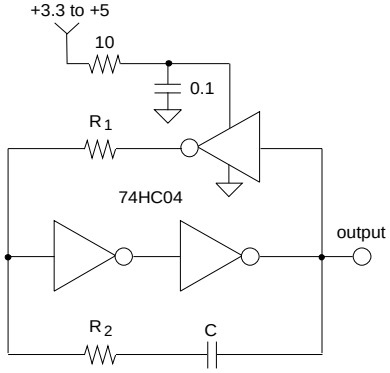



**Figure 2. Dual Stage Amplifier**

The CS5509 in Figure 1 can run as fast as 200 conversions per second if operated with a 330kHz external clock. Figure 3 shows an RC gate oscillator which can produce stable frequencies, or a CMOS 555 timer can be used. The gate oscillator can be operated from either a +5 or +3.3 V supply and maintains fairly good frequency stability over temperature.




| f | $R_1$ | $R_2$ | C |
|---|---|---|---|
| 162kHz | 10k | 3.4k | 330pF |
| 200kHz | 8.2k | 2.7k | 330pF |
| 330kHz | 5k | 1.6k | 330pF |

$$f \approx \frac{1.44}{2\,(R_1 + R_2)\,C} \qquad R_2 \approx \frac{R_1}{3}$$

**Figure 3. Temperature-Stable Gate Oscillator for +5 or +3.3 Volts.**

All of the converters (CS5504-09) can be operated with a single +5 V supply. All of the converters can also be operated with +5 V analog supply and +3.3 V on the digital supply. If this dual supply arrangement is used, the digital supply should be derived from the analog supply to ensure proper operation. Under all conditions, including start-up, the voltage on the VA+ pin must be the more positive than any other pin on the device to ensure proper substrate biasing of the chip.

### CS5507/8 with +10 V Analog Supply and +5 V Digital Supply

It is common for many weigh scales to be operated from batteries with a 12 V automotive-type battery being common. The CS5504/5/6/7/8 devices can be operated with higher supply voltage on the analog portion of the chip than on the digital portion (Note: the CS5509 is an exception and is specified with an analog supply of +5 V only). The analog supply (VA+) must always be the most positive voltage on the chip to ensure proper operation. Figure 4 illustrates the CS5507 operating from +10 V on the analog and +5 V on the digital. The bridge is excited with the +10 V and resistors are used to divide this excitation supply to obtain a ratiometric voltage reference of about 3.33 V for the converter. The circuit is designed to operate with the A/D in bipolar mode to yield more μV/count. The A/D is set-up for an input span of ± 3.33 V. A 200k pull down resistor forces a

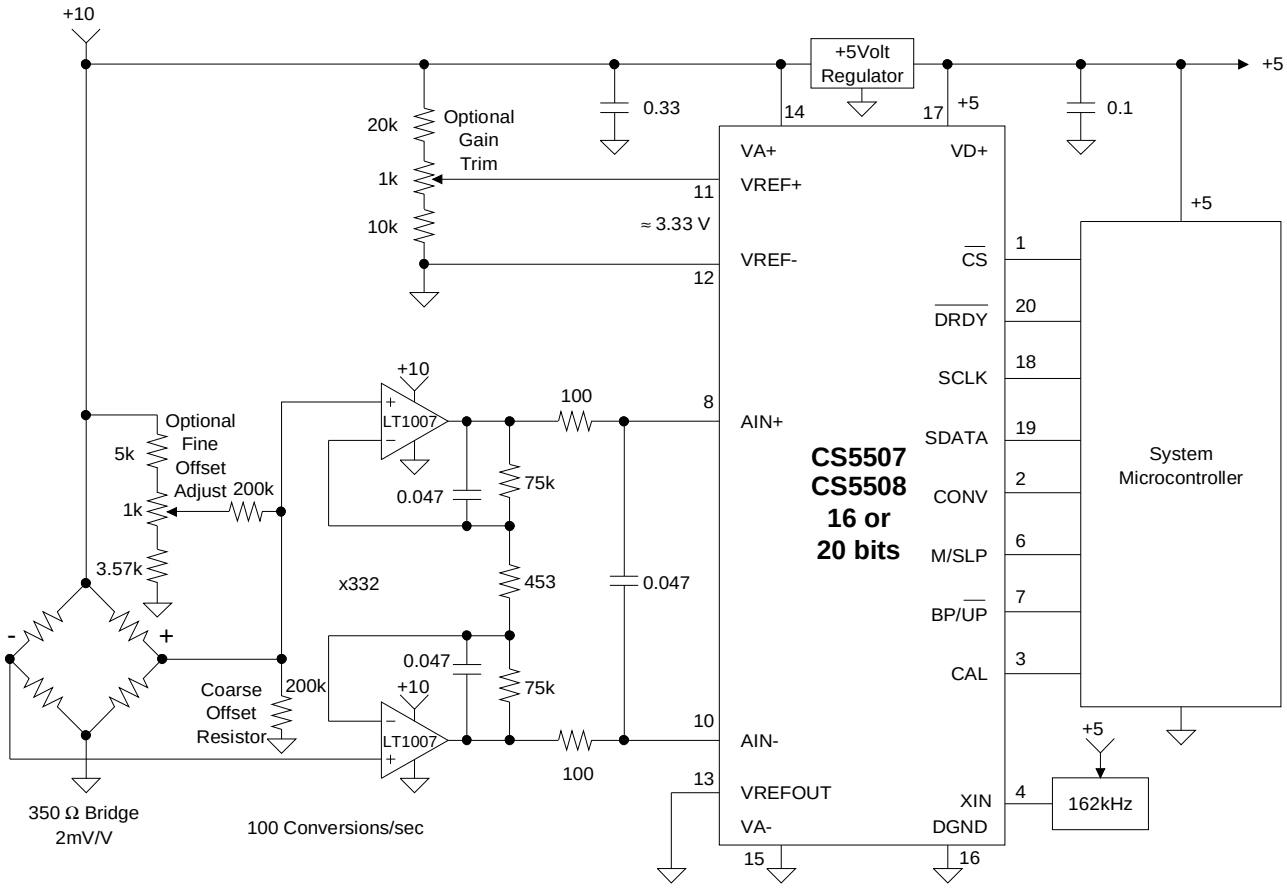



**Figure 4. CS5507/8 with +10V Analog Supply and +5 V Digital Supply.**

negative offset into the amplifier and the zero trim is used to finely adjust this offset. With zero weight on the scale, the zero trim is adjusted to yield -30,000 counts if the CS5507 16-bit A/D is used or to -500,000 counts if a 20-bit CS5508 is used. With full scale weight on the scale the gain trim is adjusted for +30,000 counts in the CS5507 or +500,000 counts in the CS5508 (Note that the CS5507 and CS5508 are pin compatible). This leaves some counts for both zero underflow and for overrange. The amplifier components set the bandwidth to 45 Hz. With the 45 Hz bandwidth, the circuit exhibits about 50,000 noise-free counts. With an external 162 kHz clock, the converter can operate at 100 conversions per second. If 20 conversion words from the CS5508 are averaged, the circuit will yield more than 200,000 noise-free counts. A limitation of this circuit is that the bipolar amplifiers can exhibit significant offset drift as the temperature changes. There are several circuits in this application note which will show how to overcome offset drift.

## CS5505/6 Operating From ± 5 V Supplies

The CS5504/5/6/7/8 converters (not the CS5509) can be operated with ±5 V on the analog section of the converter, and with either +5 V or +3.3 V on the digital section.

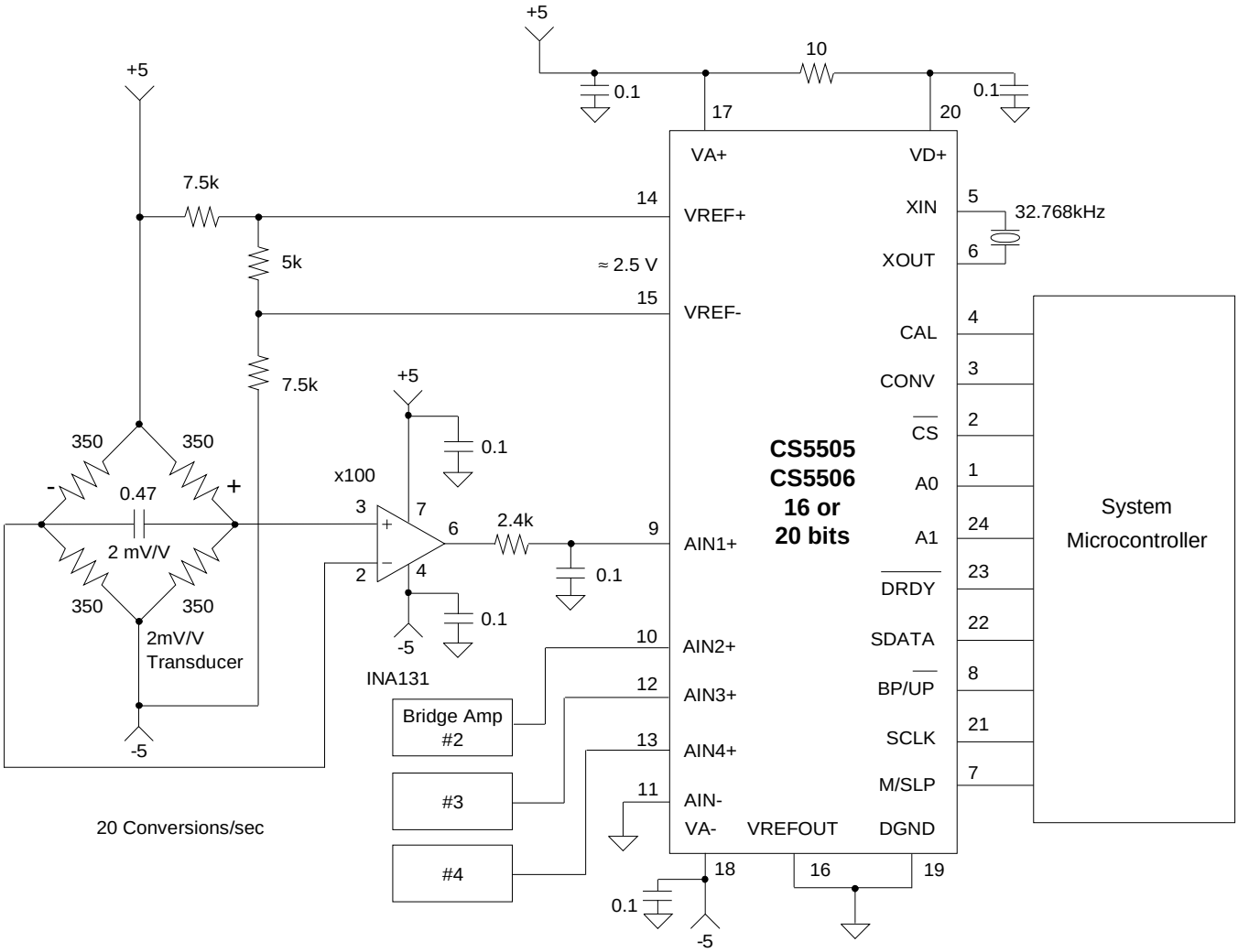



**Figure 5. CS5505/6 Operating from ± 5V Supplies.**

Figure 5 illustrates an application which uses an instrumentation amplifier to amplify and convert the differential bridge signal to a ground-referenced signal for the converter. Full scale for the converter is set by the divider resistors which determine the voltage reference input to the VREF+/- pins of the converter. The reference voltage in the figure is set to 2.5 V. The bridge sensitivity is 2 mV/V so the full scale bridge output is 20 mV. This is amplified by the 100 gain of the instrumentation amplifier to obtain 2.0 V into the converter. The converter can be operated in either unipolar or bipolar mode. Up to four load cells, each with its own amplifier, can be input to the CS5506. The measurement assumes the voltage reference will remain ratiometric across all four load cells.

## CS5507 Switched-Bridge Low-power Digitizer with +10 V Excitation

Some applications call for reduced operating power. One method of significantly reducing the power consumption is to apply the supply voltage to the bridge transducer only when a

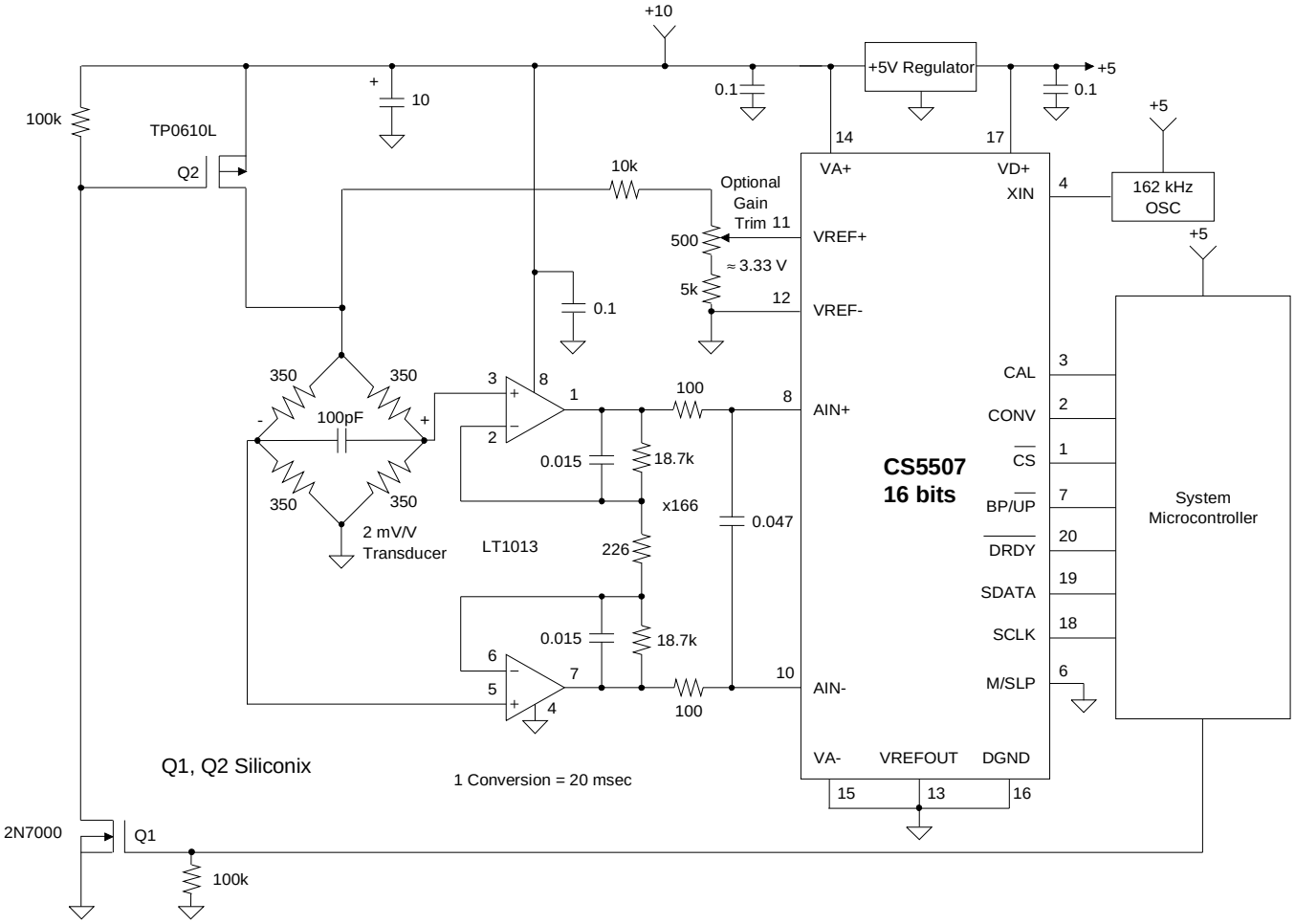



**Figure 6. CS5507 Switched-Bridge Low-power Digitizer with +10 Volt Excitation.**

measurement is required. Figure 6 illustrates an example circuit in which the power to the bridge transducer is switched on only when a measurement is desired.

The circuit as shown is optimized for a +10 V analog supply. The circuit can be modified (optimized) to operate from any analog supply from 11 V to 6.5 V (assuming the +5 V regulator needs 1.5 V of input/output differential) by changing the resistor values which determine the voltage reference to the converter and by changing the gain resistors in the amplifier to compensate for the change in the bridge output signal. The circuit shown illustrates a 2 mV/V transducer outputting 20 mV full-scale. A gain of 166 amplifies this to 3.32 V into the A/D. The full-scale of the A/D is set at 3.33 V by dividing down the excitation voltage.

In the power arrangement shown, the CS5507 A/D uses about 4 mW. The converter is clocked from an external gate oscillator clock (162 kHz) to yield a conversion time of 10 msec. When power is applied to the bridge, a delay must occur to allow the signal to settle before a valid conversion can be performed. Settling time to 16 bits after power is applied to the bridge takes about 3.3 msec. The microcontroller can use an internal timer to time about 4 msec. to allow for the delay or the microcontroller can perform a dummy conversion in the converter to allow for settling time. When the dummy conversion is finished (10 msec. later) the conversion data is discarded and a second conversion is then performed to make a valid measurement. After the second conversion is complete ($\overline{\text{DRDY}}$ falls the second time) power to the bridge is deactivated and the conversion word is clocked out of the converter's serial port.

Power consumed by the transducer dominates the power dissipated in the circuit. Average power consumption in the bridge can be reduced by a factor of at least fifty (<6 mW) if the bridge is powered for only 20 msec. for a reading each second. If even lower off power is desired, the supply to the LT1013 can also be switched along with the bridge excitation.

**CS5509 Switched-Bridge Low-power Digitizer with +5 V Excitation**

The circuit in Figure 7 is similar to the previous one, but operates from a single +5 V. The circuit shows a load cell with 3 mV/V sensitivity. A 2 mV/V transducer can be used if additional gain is added; or the voltage reference into the converter can be lowered to 1.67 V with some minor increase in noise. Average power consumption in the load cell is only 1.5 mW for one reading per second.

**CS5516/CS5520 Using DC Bridge Excitation**

The CS5516 (16-bit) and CS5520 (20-bit) A/D converters are designed for bridge measurement applications. They include an instrumentation amplifier with X25 gain, a PGA (programmable gain amplifier) with gains of 1, 2, 4, and 8, and a four bit DAC which can trim out offset up to ± 200% of the full scale signal magnitude. The input span can be adjusted by changing either the magnitude of the voltage at the VREF pins of the converter or by changing the PGA gain.

In the circuit shown in Figure 8, the bridge is excited with ± 5 volts. Resistors R1, R2, and R3 divide the excitation voltage to give a 2.5 V reference signal into the VREF pins. The input span at the AIN pins of the converter is determined by dividing the voltage at the VREF pins by the PGA gain and the X25 instrumentation amplifier gain. For example, with 2.5 V into the VREF pins, and the PGA set to a gain of 8, the input span at the AIN pins is 2.5/(8 X 25) = 12.5 mV in unipolar mode or ± 12.5 mV in bipolar mode. The converter offers several calibration features to remove offset and to calibrate the gain slope. The input span of

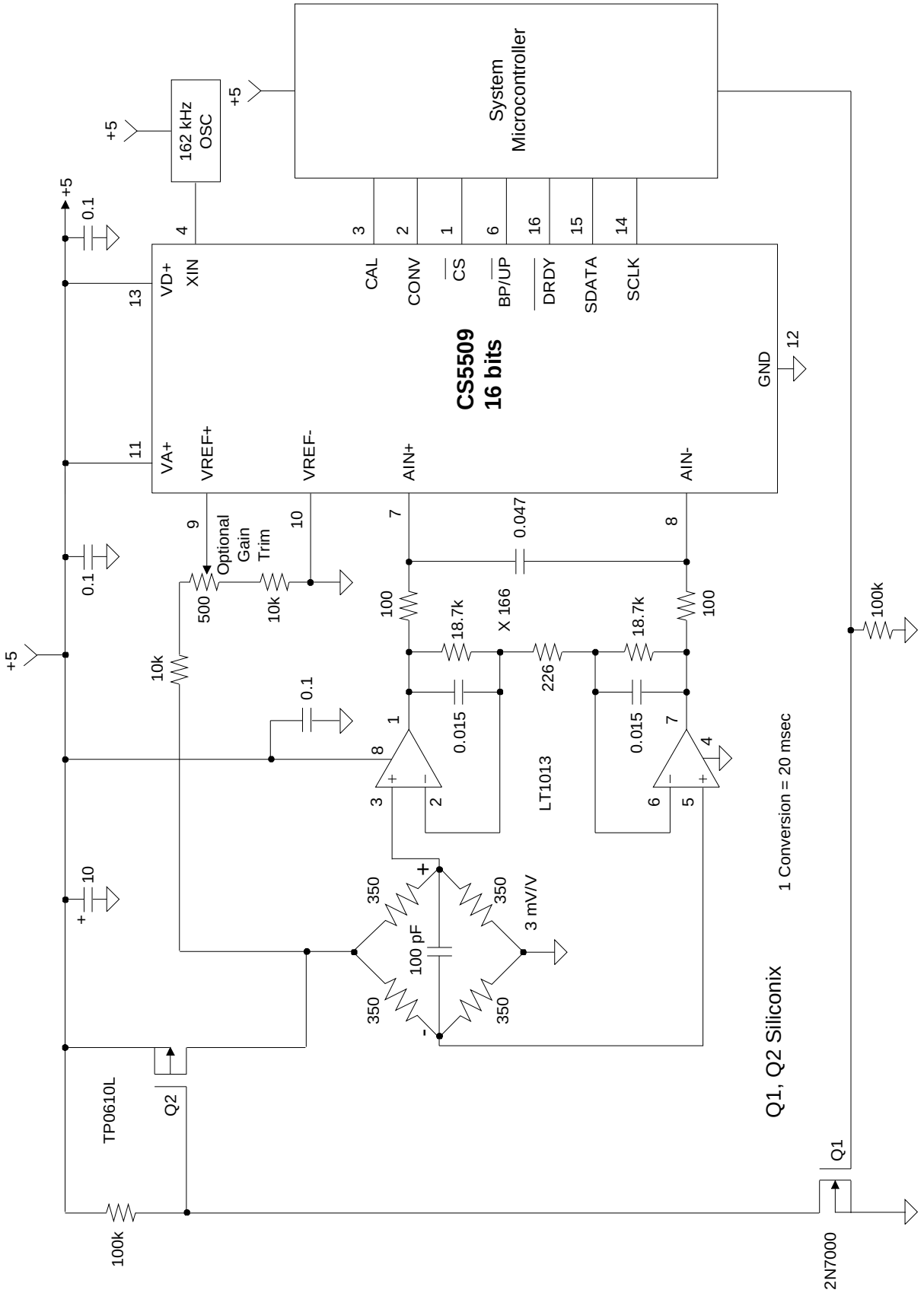



**Figure 7. CS5509 Switched-Bridge Low-power Digitizer with +5 Volt Excitation.**

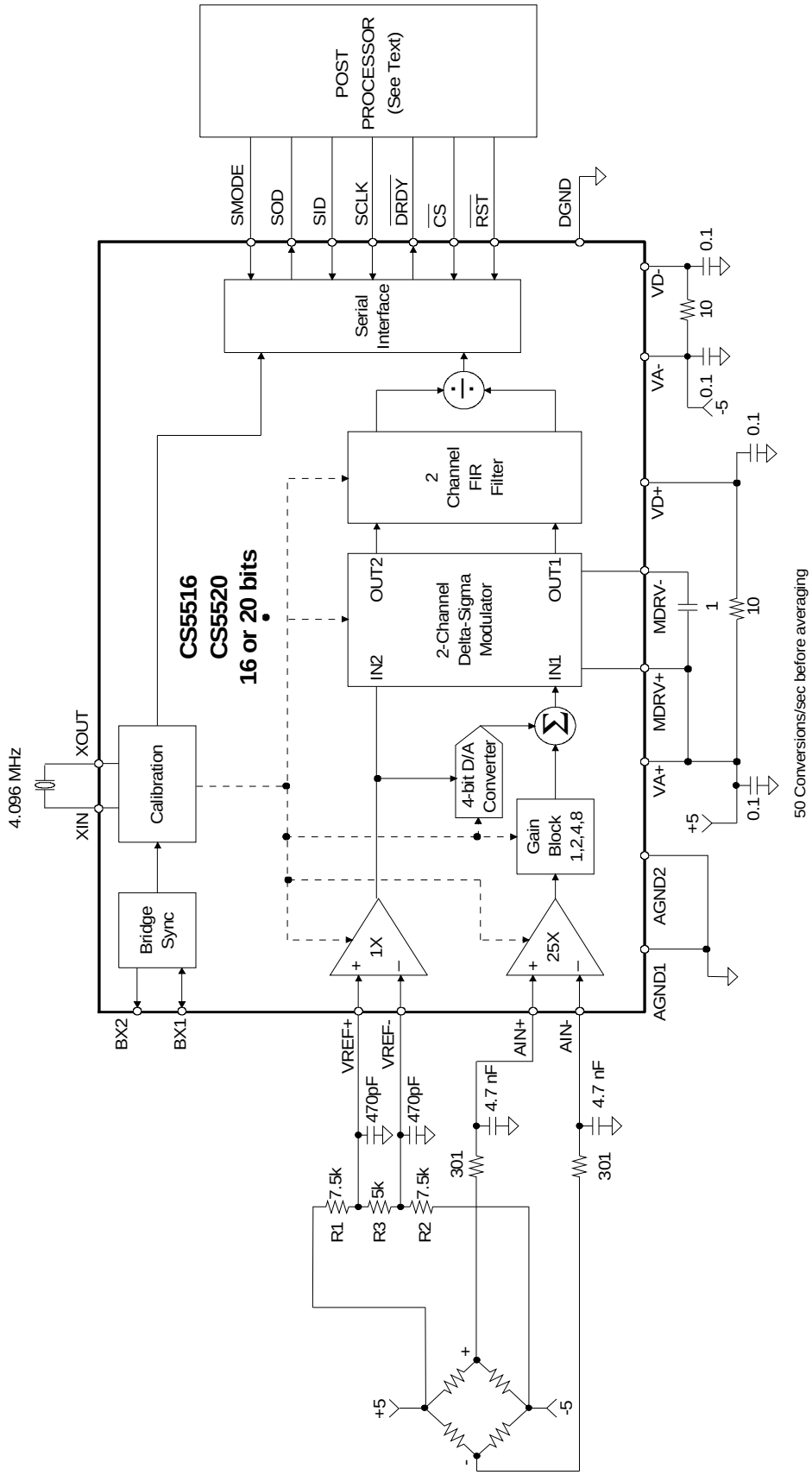



**Figure 8. CS5516/CS5520 Using dc Bridge Excitation.**

12.5 mV (considered the nominal value for this particular selection of PGA gain and VREF voltage) can be gain calibrated for input signals from 20 % less than or 20 % greater than the nominal 12.5 mV value. In other words, the gain can be calibrated with an input as low as 10 mV or as high as 15 mV when the nominal value is set for 12.5 mV. The nominal input can be changed by changing the PGA gain or by changing the divider resistors for the excitation voltage. The converter can accept a VREF input voltage of any value between 2.0 to 3.8 V.

The CS5516 and CS5520 can be operated on any clock frequency from 1.0 MHz to 5.0 MHz. the digital filter will give greater than 90 dB of attenuation to 50 and 60 Hz line interference if the input clock is 4.096 mHz or less. With a 4.096 MHz clock into the converter it will output conversion words at a 50 Hz rate. For optimal filtering it is desirable to average output words from the converter. If ten output words are averaged, the noise bandwidth is reduced to about 2.5 Hz.

The CS5516 and CS5520 support either dc or ac bridge excitation.

## AC-EXCITED OR CHOPPED SIGNAL BRIDGE CIRCUITS

When measuring low level signals, measurement performance can be enhanced if the signal is "chopped". Chopper amplifiers are commonly used to minimize amplifier offset drift. The disadvantage of chopper amplifiers is that they are generally manufactured using CMOS technology and have higher thermal noise than bipolar amplifiers. Chopper amplifiers have low offset drift and the 1/f noise of the amplifier tends to be averaged out due to chopping. Still, CMOS integrated circuit chopper amplifiers tend to have noise performance somewhere between 45 $nV/\sqrt{Hz}$ to 250 $nV/\sqrt{Hz}$. This noise limits the measurement performance when used in a high resolution bridge digitizer. Another limitation of a chopper amplifier is that it corrects only its own offset errors and does not correct offsets or parasitic thermocouples external to itself, including those created when its own package leads connect to the circuit card traces.

There are several other approaches to chopping the signal which can be used to enhance performance. Circuits will illustrate a number of these approaches. Some chop the signal after it is output from the bridge. Others actually switch the polarity to the bridge itself. Either method can be used to remove amplifier offsets and parasitic thermocouple effects. Switching the bridge has the advantage that it enables any nonratiometric offset of the bridge to be removed. But caution is advised; some silicon gages can be damaged if the excitation supply is reversed. Check with the gage manufacturer to determine if a silicon gage bridge can be used with AC excitation.

Switching the bridge may not be practical in applications which have very long cables due to the large cable capacitance.

### Bridge with Digital Offset Correction and Kelvin Reference Sensing.

One method of getting the lower noise of bipolar amplifiers and achieve good offset stability is to use digital offset correction. Figure 9 illustrates a circuit in which the input of the amplifier stage is periodically shorted and the offset measured with the A/D. The digital code is then used to correct readings from the converter when the signal is being measured. The schematic shows only the circuitry for one channel (the CS5504 has two input channels). Only one half of the DG303 is used per channel. LT1007 op amps are used for their low noise; but a dual LT1013 or quad LT1014 could be used if higher noise is acceptable. The LT1013 and LT1014 are capable of measuring signals with an input range which

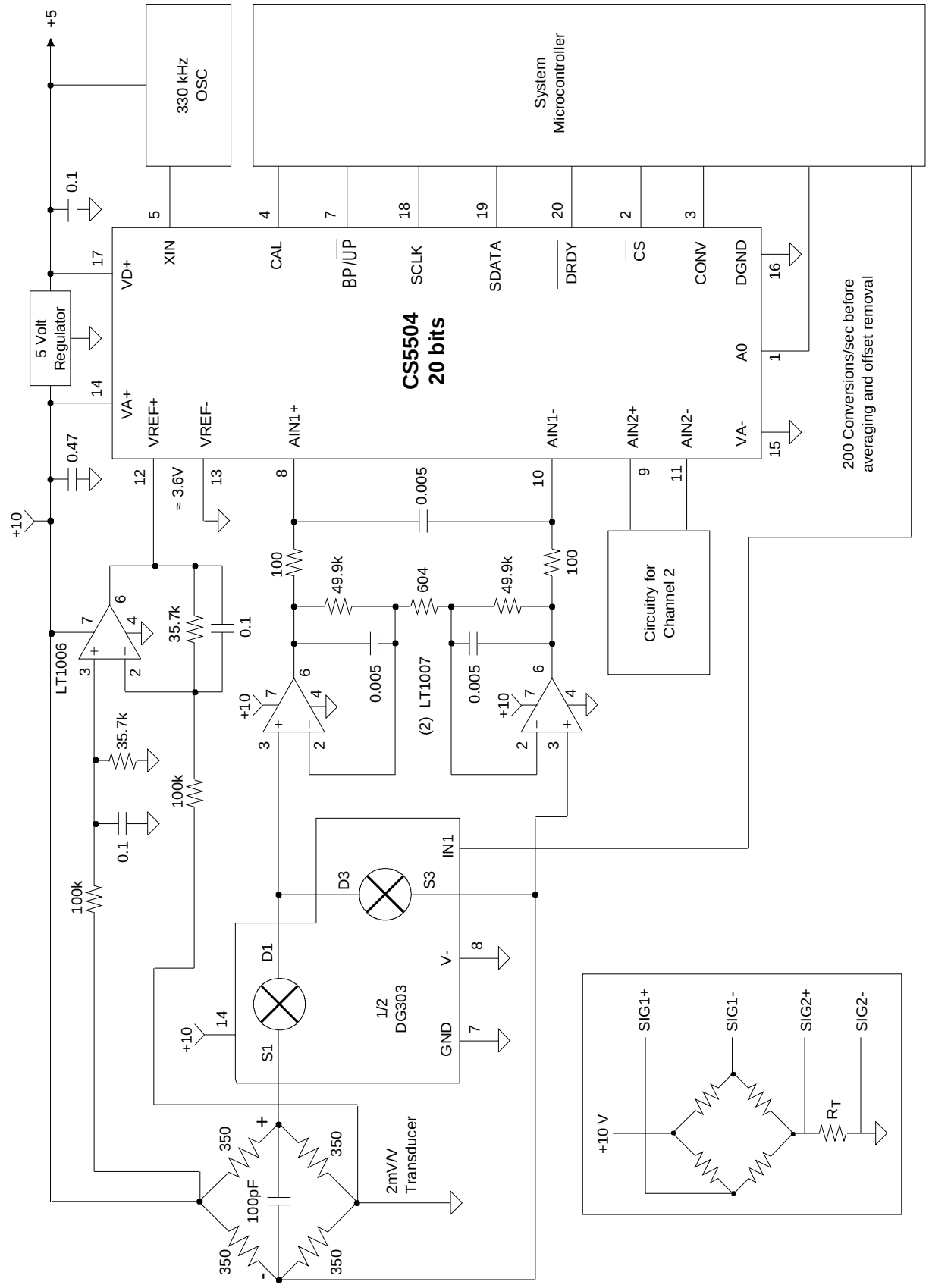



**Figure 9. Bridge with Digital Offset Correction and Kelvin Reference Sensing.**

includes the negative supply rail. One application for this may be for measuring a temperature compensating resistor in series with the bridge (see inset in Figure 9).

The converter in Figure 9 is set up in bipolar mode (use bipolar mode even if you want unipolar measurements as the bipolar setup provides less noise per code and allows for negative tempco drift of the zero reference point) and runs at 200 conversions a second. To correct offset and measurements on both channels, the following measurement sequence was used: Select the DG303 to short the inputs to both channel one and channel two. Use A0 on the converter to select channel one. Perform one conversion and discard the data to allow for settling. Perform a second conversion and keep the offset code for channel one. Change A0 to opposite state and measure the offset code for channel two. Switch the DG303 on both channels to measure the input signal and set A0 to measure channel one. Perform one dummy conversion and discard the data. Then perform a second conversion and keep the reading. Correct this reading with the offset reading taken for the same channel. Then change A0 and read channel two and correct it for offset. Each channel takes four conversions per result, so for two channels, outputs are available at 25 per second. A running average of 12 corrected words is recommended to improve noise performance. With 12 words averaged, the performance is greater than 150,000 noise-free counts with two updates per second for each channel.

If the circuit in Figure 9 is used at higher temperatures, one DG303 should be used for each amplifier stage with a switch (always on) included in the negative lead of the bridge circuit. With this configuration, the errors due to leakage currents and the on resistance of the switches will be more balanced on both the plus and minus leads of the bridge.

The voltage reference input to the A/D converter is buffered to reduce loading by the Kelvin sense leads. If the voltage reference Kelvin sensing lines are long, 50 and 60 Hz line interference may be picked up. The voltage reference input to the CS5504/5/6/7/8/9 should be filtered to prevent line interference if the devices are operated at a clock frequency other than 32.768 kHz.

**Bridge with Signal Chopping Using CS5504**

The load cell is often the dominant cost factor in many weighing systems. A lower cost load cell can be achieved by leaving out the temperature compensation gages and reducing testing during manufacturing. As long as the load cell temperature drift is repeatable, the entire system can be compensated with software in a microcontroller. In this type of system, a temperature sensor is usually embedded inside the load cell. The entire system is then characterized over temperature. A microcontroller reads the load cell and its temperature and uses a look-up table to correct the load cell output for drift over temperature. Figure 10 illustrates an example.

The circuit uses the CS5504 two channel fully differential A/D configured to convert at 200 samples per second. The analog portion of the A/D and the bridge are operated from +10 volts. The voltage reference for the A/D is developed from the bridge excitation. Channel two of the converter measures the output of a thermistor mounted in the load cell housing. The thermistor is excited with the same voltage as the bridge.

The output of the bridge is amplified by a buffer amplifier composed of two LT1007s. The CS5504 is operated in bipolar mode with ± 524,000 counts. A DG303 analog switch is used to reverse the polarity of the signal into the amplifier upon command from the microcontroller. A convert (CONV) command is

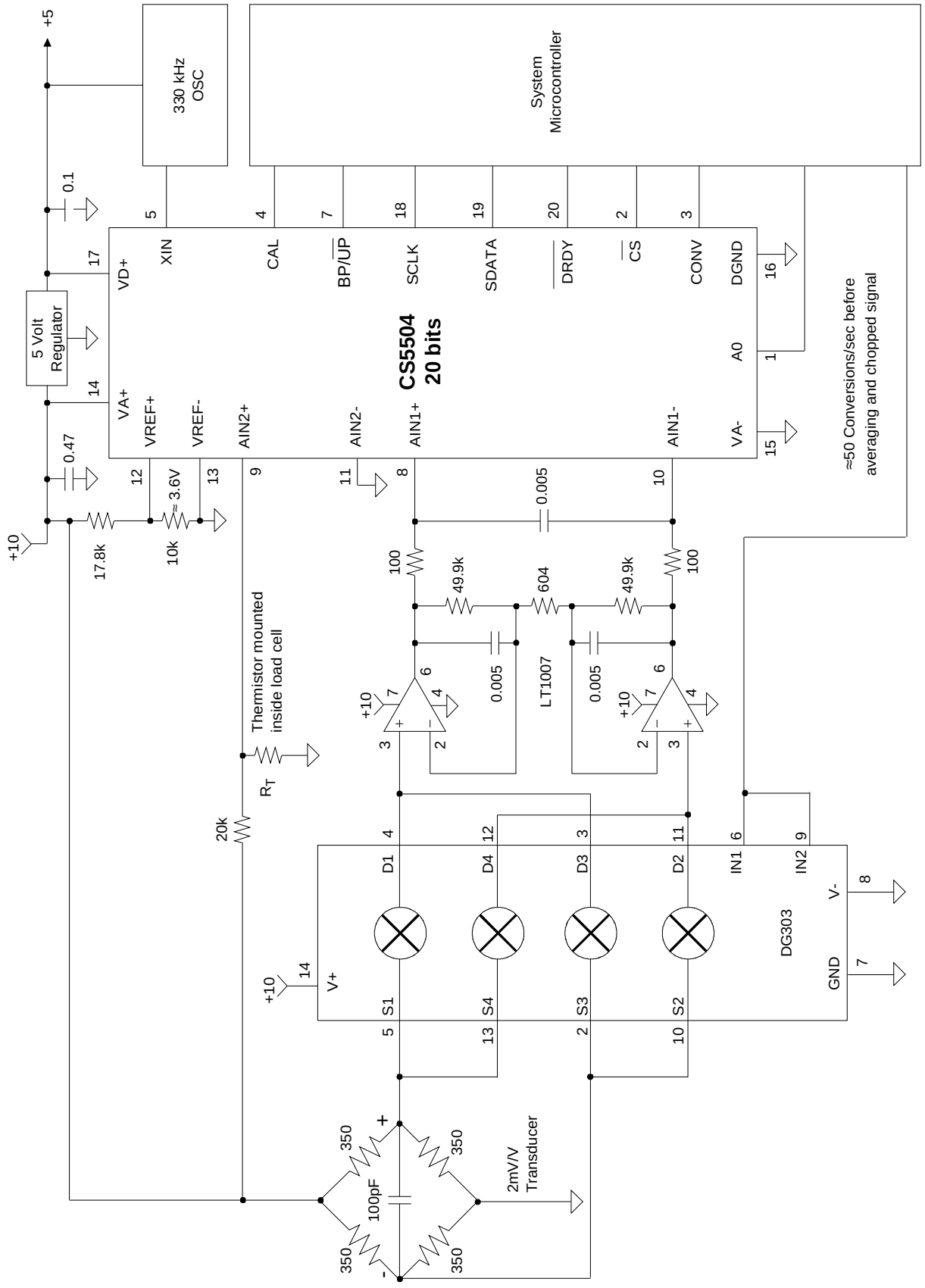



**Figure 10. Bridge with Signal Chopping Using CS5504.**

issued to the converter only after the DG303 switch has been switched to one position long enough for the buffer amplifier to have settled on the signal. With the DG303 in one position, the output of the amplifier will result in a positive voltage into the converter; when switched to the other position the output of the amplifier will be negative into the converter. The negative reading is then subtracted from the positive reading and then divided by two[(+answer - (-answer)]/2. The result will be a reading of the load cell signal with the offset of the amplifier removed. For example, let us assume the circuitry has +332 counts of offset and the signal from the bridge (the bridge itself has no offset for illustration purposes) should be 4700 counts. The reading from the converter with a positive input signal will be 5032 counts; the reading with the signal reversed will be -4368 counts. [5032 - (-4368)]/2 = 4700 counts, which is the answer with the offset averaged out. Note that dividing by two is really unnecessary as the number (9400) is representative of the signal magnitude. The converter can sample at 200 samples per second; performing a conversion every 5 msec. The converter has two channels but needs not to measure the temperature channel very often. The measurement sequence for channel one is follows: Switch the DG303 to condition one (switches 1 and 2 are on, switches 3 and 4 are off); perform a conversion but throw the data away as this conversion time is used to allow the amplifier to settle (the circuit shown takes less than 4 msec. to settle). Then perform a second conversion and keep the data. Switch the DG303 to condition two (switches 3 and 4 are on, 1 and 2 are off); perform a conversion but throw away the data to allow for settling. Then perform a second conversion, subtract the negative answer from the previous positive one (from switch condition one) and divide the answer by two (if you need the actual answer). Since it will take four conversion cycles to obtain one averaged answer, the converter will be able to update at a 50 Hz rate (assuming the temperature channel is not being read). The effects of noise in the output data can be reduced if words are averaged. An average of 20 of the final readings will result in a noise reduction of 4.4 times. Converting in this fashion will result in a converter with greater than 150,000 noise-free counts, and an update rate of about two and a half times per second. Chopping the signal lowers the input drift in the amplifier to about 125 nV peak-to-peak under slowly varying temperature conditions.

### Switched Bridge with CS5504 Using +10 V Analog Supply

The previous circuit achieved offset stability by chopping the bridge output. In the circuit in Figure 11 the polarity of the excitation voltage to the bridge is periodically reversed. Channel one of the CS5504 is used to measure the amplified signal from the bridge. The second channel of the converter is used to measure the magnitude of the bridge excitation. The bridge excitation is measured because the driver exhibits some change in drive output over temperature. The measurement sequence is as follows. For notation let the bridge excitation be in position one when the top of the bridge is +10 V (the actual voltage will be about 9.5 to 9.8 V depending upon the driver source impedance). When switched to this position, the microcontroller pauses for a short delay (1 msec or so) before performing a conversion on channel two to ensure that the circuit has settled. Once the conversion is performed on channel two, the data is saved. Then the A0 line to the converter is switched to select channel one. The amplifier has settled during the time the conversion was performed on channel two. A conversion is performed on channel one and the data is saved. Then the bridge excitation is flipped to position two ( the top of the bridge is grounded). After a 1 msec delay a conversion is performed on channel two; the negative answer is subtracted from the previously collected positive answer from channel two. Then A0 on

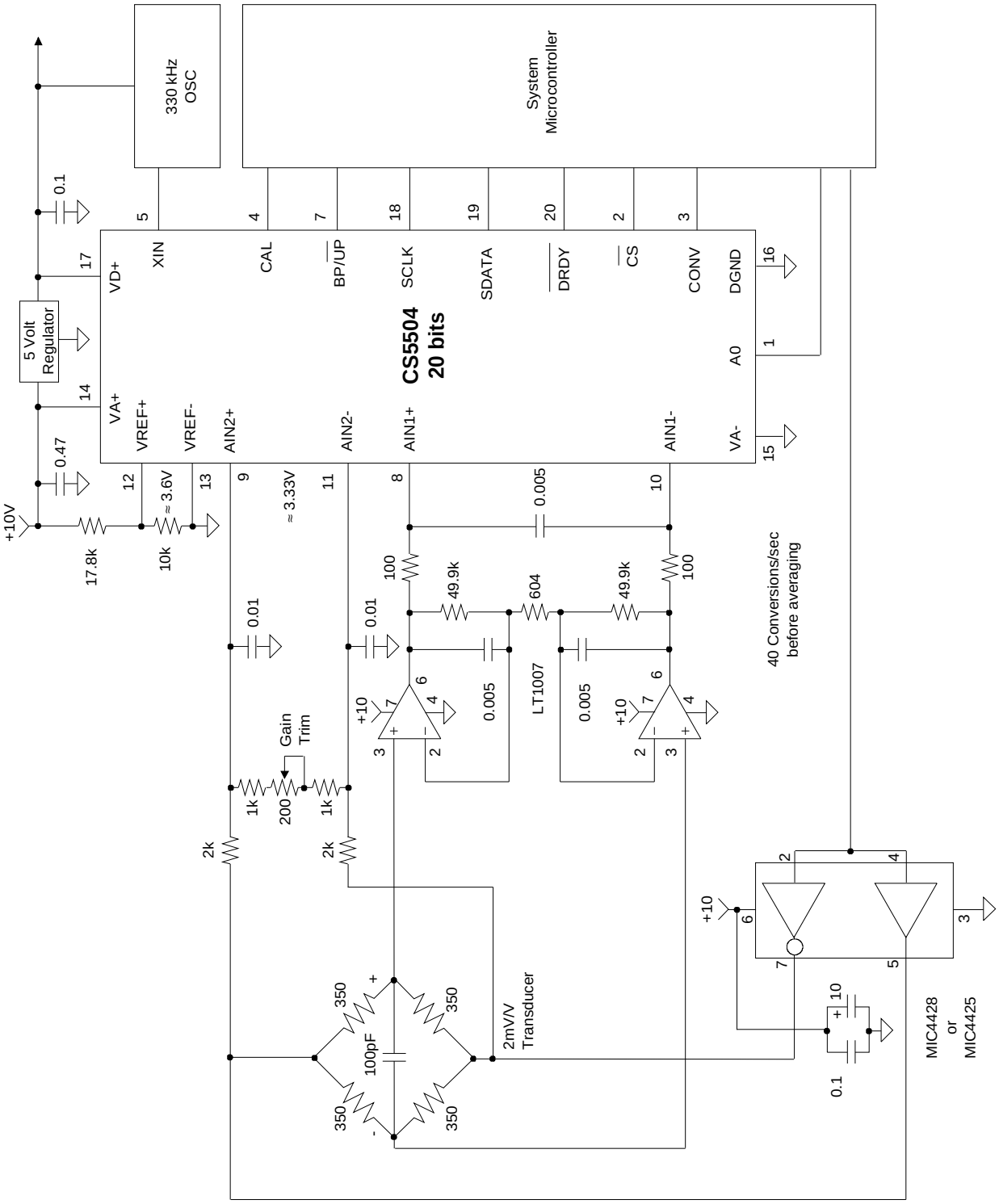



**Figure 11. Switched Bridge with CS5504 Using +10 Volt Analog Supply**

the converter is flipped and a conversion is performed on channel one of the converter. The negative answer for channel one is then subtracted from the previous positive reading from channel one.

The resultant readings from each channel can be averaged to reduce the effects of noise. Then the readings from the two channels are ratioed. The channel two data represents the value of the excitation on the bridge. Channel one data represents the output signal from the bridge as a proportion of the bridge voltage. By ratioing the data (AIN1/AIN2) any drift in the bridge excitation voltage (such as those caused by changes in the driver output impedance) is compensated.

The circuit can read both channels and calculate a final answer for the bridge signal in less than 25 msec.; which means an output word can be calculated at a rate of 40 times per second. If 20 output words are averaged the circuit will yield better than 100,000 noise-free counts with the offset drift of the digitizer being less than 50 nV over time.

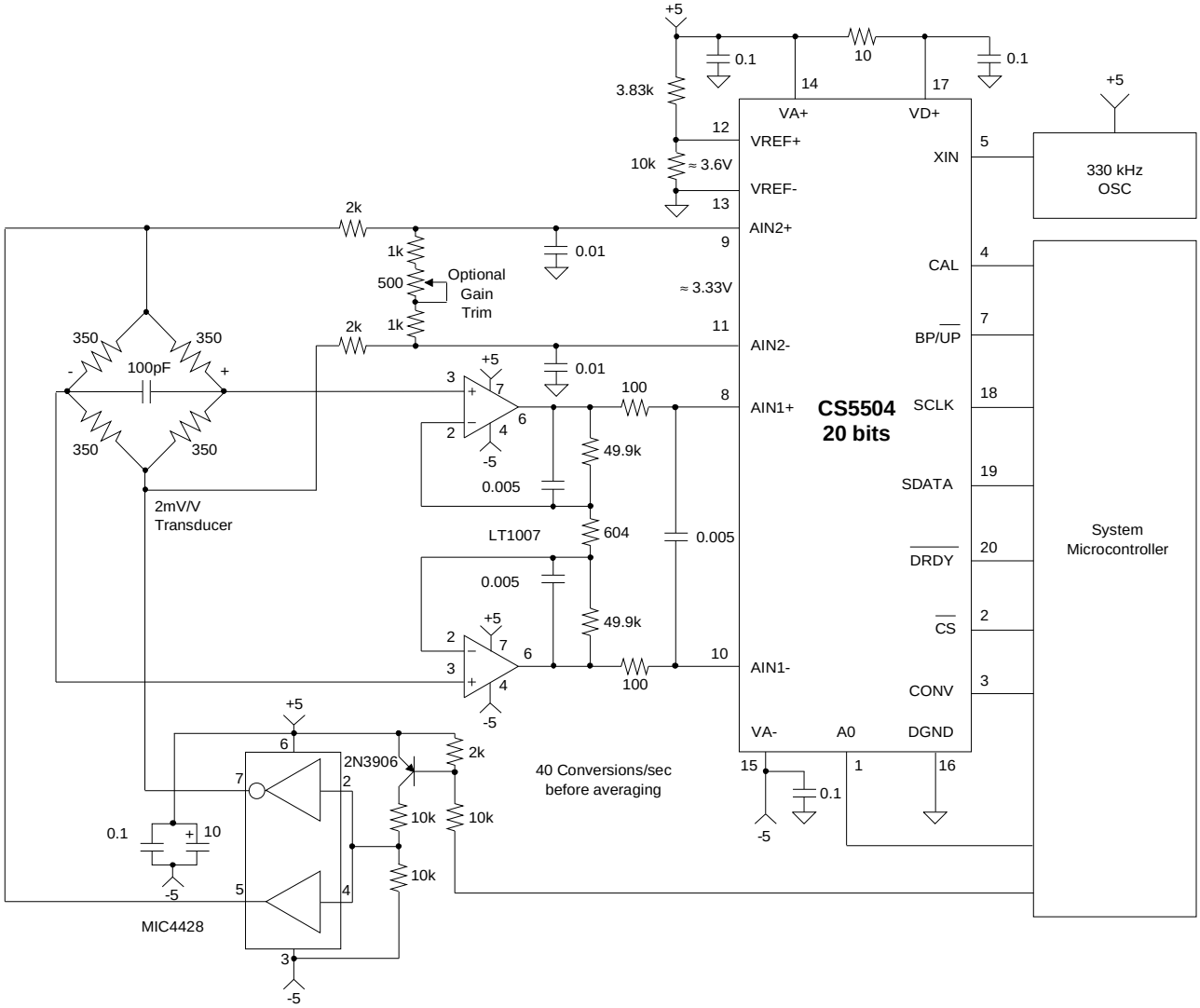



**Figure 12. Switched Bridge with CS5504 Using ± 5 Volt Analog Supplies.**

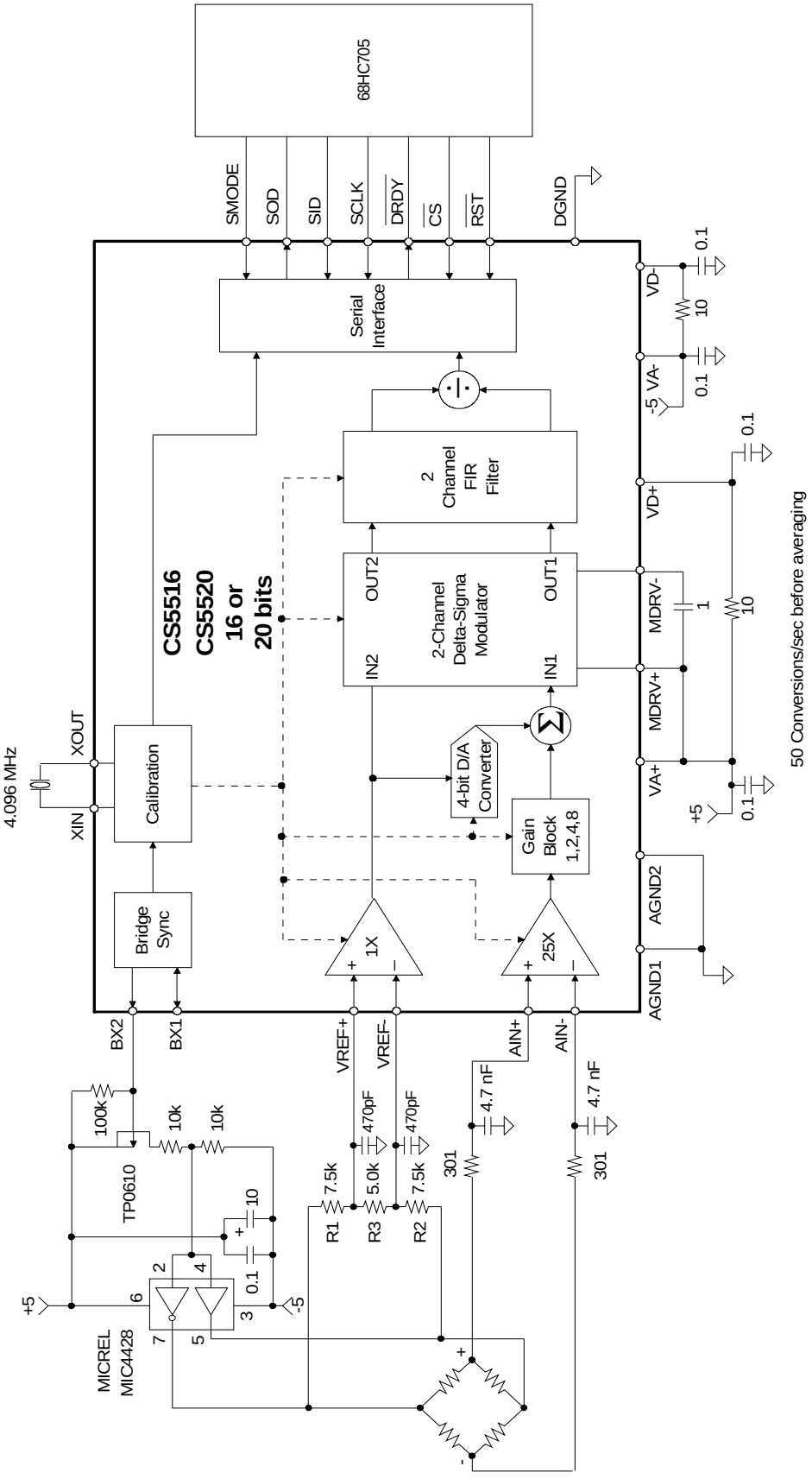



**Figure 13. CDB5516/20 Evaluation Board Circuit.**

### Switched Bridge with CS5504 Using ± 5 V Analog Supplies

This circuit in Figure 12 is basically identical to the previous circuit, but is configured to run from ± 5 V on the analog supplies.

### CDB5516/20 Evaluation Board Circuit

The CDB5516 and CDB5520 evaluation boards use the circuit in Figure 13. The CS5516 (16-bit) and CS5520 (20-bit) converters are optimized for bridge measurement applications. The evaluation board comes with software which runs on a PC-compatible computer. The evaluation board includes a microcontroller which communicates with the PC via the RS-232 serial port. The software allows the user to read and write all of the registers inside the CS5516/20 converter, perform conversions, save conversion data to a file, and perform some noise statistics on the captured data.

The CS5516 and CS5520 support both dc-excited bridges and ac-excited bridges. Figure 14 illustrates the benefit of AC excitation. In one of the plots in Figure 14, the CS5520 converter was set up for a bipolar input span of ± 12.5 mV and dc bridge excitation. Conversions were performed with a zero input signal from the bridge and data was collected for a one hour time interval. One LSB of the CS5520 was equivalent to about 25 nV. The data collected indicates that over the one hour period the average value of the data drifted as much as 1.25 µV, or about 50 counts. The drift is due to parasitic thermocouples in the components or wiring of the board. The evaluation board was open to the air. The data illustrates that the cycling of the air conditioner induced thermal gradients across the circuitry, changing the voltage effects of the parasitic thermocouples in the circuitry. The second plot in Figure 14 illustrates the stability of the data when the converter is set up for the same operating conditions, but with ac bridge excitation. The plot illustrates the normal thermal noise of the circuit but the average value remains stable over time.

The CS5516 (16-bit) and CS5520 (20-bit) A/D converters include an instrumentation amplifier with X25 gain, a PGA (programmable gain amplifier) with gains of 1, 2, 4, and 8, and a four bit DAC which can trim out offset up to ± 200% of the full scale signal magnitude. The input span can be adjusted by changing either the magnitude of the voltage at the VREF pins of the converter or by changing the PGA gain.

In the circuit shown in Figure 13, the bridge is excited with a 1 kHz square wave from the MIC4428 (or the Micrel MIC4425) driver. The driver outputs about ± 5 V. The 1 kHz drive signal is output from the BX2 pin of the CS5520. Control bits in a configuration register inside the chip have been set to select internal ac excitation with a frequency of 1 kHz (XIN = 4.096 MHz). The converter is designed to perform synchronous detection on the AIN and VREF input signals when operated in the ac excitation mode. This means that the converter measures the signal which is of the same frequency and phase as the excitation clock coming from the BX2 pin.

Resistors R1, R2, and R3 divide the excitation voltage to give a 2.5 V reference signal into the VREF pins. The input span at the AIN pins of the converter is determined by dividing the voltage at the VREF pins by the PGA gain and the X25 instrumentation amplifier gain. For example, with 2.5 V into the VREF pins, and the PGA set to a gain of 8, the input span at the AIN pins is 2.5/(8 X 25) = 12.5 mV in unipolar mode or ± 12.5 mV in bipolar mode. The converter offers several calibration features to remove offset and to adapt the gain. The nominal input span of 12.5 mV can be gain calibrated for input signals within ± 20% of

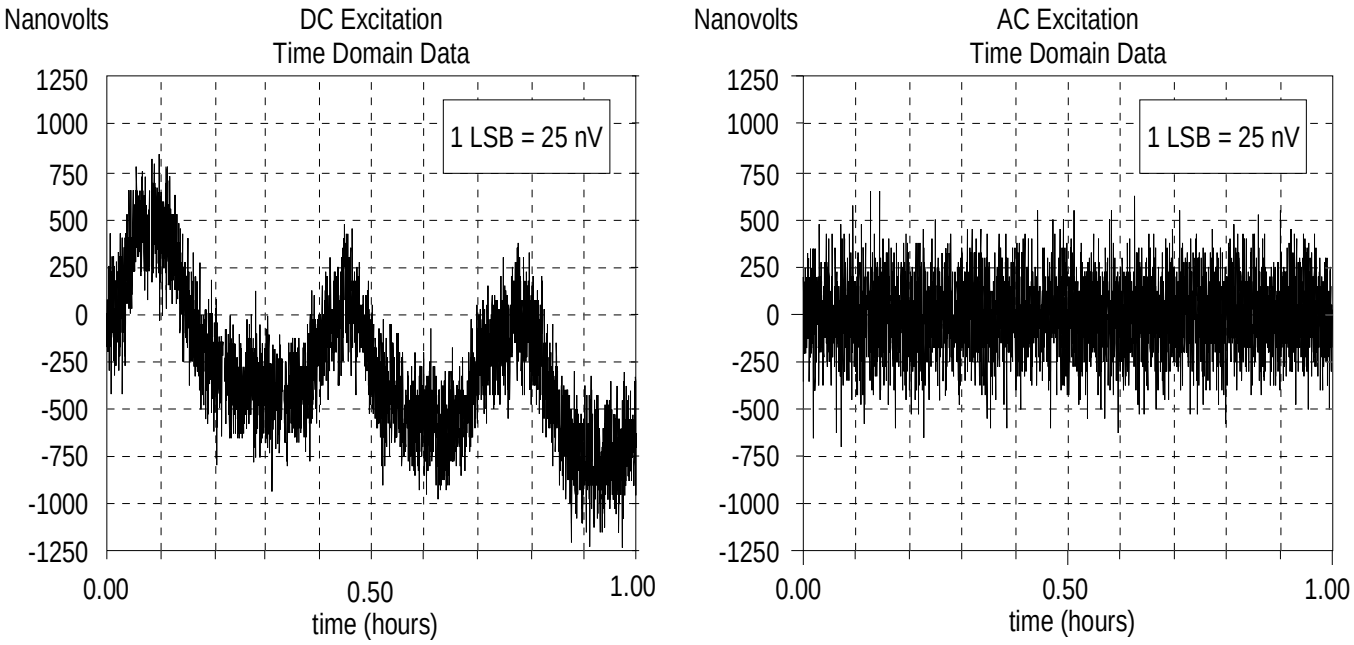



**Figure 14. DC Versus AC Excitation.**

nominal. In other words, the gain can be calibrated for an input as low as 10 mV or as high as 15 mV when the nominal value is set for 12.5 mV. The nominal input can be changed by changing the PGA gain or by changing the divider resistors for the excitation voltage. The converter can accept a VREF input voltage of any value between 2.0 to 3.8 V. The CS5516 and CS5520 can be operated on any clock frequency from 1.0 MHz to 5.0 MHz. The digital filter will give greater than 90 dB of attenuation to 50 and 60 Hz line interference if the input clock is 4.096 mHz or less. With a 4.096 MHz clock into the converter it will output conversion words at a 50 Hz rate. For optimal filtering it is desirable to average output words from the converter. If ten output words are averaged, the noise bandwidth is reduced to about 2.5 Hz.

### CS5516 with External 25 Hz AC Excitation

The CS5516 and CS5520 support two ac bridge excitation modes; internal and external. In the internal excitation mode, the excitation clock is derived internal to the converter from the oscillator frequency on the chip and is output from the BX1 and BX2 pins. In the external excitation mode (selected by setting a bit in the configuration register of the converter), a square wave whose frequency is a sub-multiple of the XIN frequency to the converter (see the CS5516/20 data sheet for details) is input into the BX1 pin of the converter.

When using the CS5516 or CS5520 in the ac excitation mode, the AIN and VREF signals into the converter are sampled 64 XIN clock cycles after the excitation signal is switched. When the square wave excitation changes polarity, the circuitry, including the bridge, the load cell cable, and any filtering components must settle to at least 5 per cent accuracy within the 64 XIN clock cycles after the switching edge. This can be a limiting factor in using square wave ac excitation, especially with long cables which have a large capacitance.

The excitation frequency can be lowered to XIN/(10 X $2^{14}$) if output words from the converter are averaged over several conversion cycles. For example, with a 4.096 MHz clock, a

decade divider (74HC4017) can be followed by a binary $2^{14}$ divider (74HC4020) to yield a 25 Hz excitation frequency. The converter will output conversion words at a 50 Hz rate, or two output words for each one cycle of the bridge excitation. The 25 Hz excitation reduces the switching frequency of the bridge so the circuit spends more time measuring and less time settling. This will improve measurement performance, but multiple output words (an even number of them) must be averaged to ensure equal samples for both polarities of the excitation clock. Figure 15 illustrates this circuit. Note that the details on connecting the clock divider chips have not been shown to simplify the schematic.

### CS5516/CS5520 with AC-Excitation Controlled by a Microcontroller

If the load cell cables are very long, the capacitance may be so large that the circuit cannot settle and yield an accurate result with the 25 Hz circuit. Another option exist. Rather than use the counters in Figure 15 to control the BX1 signal and the drive polarity, one can use a microcontroller output line. With the converter set up in the external excitation mode, the microcontroller can control the polarity of the

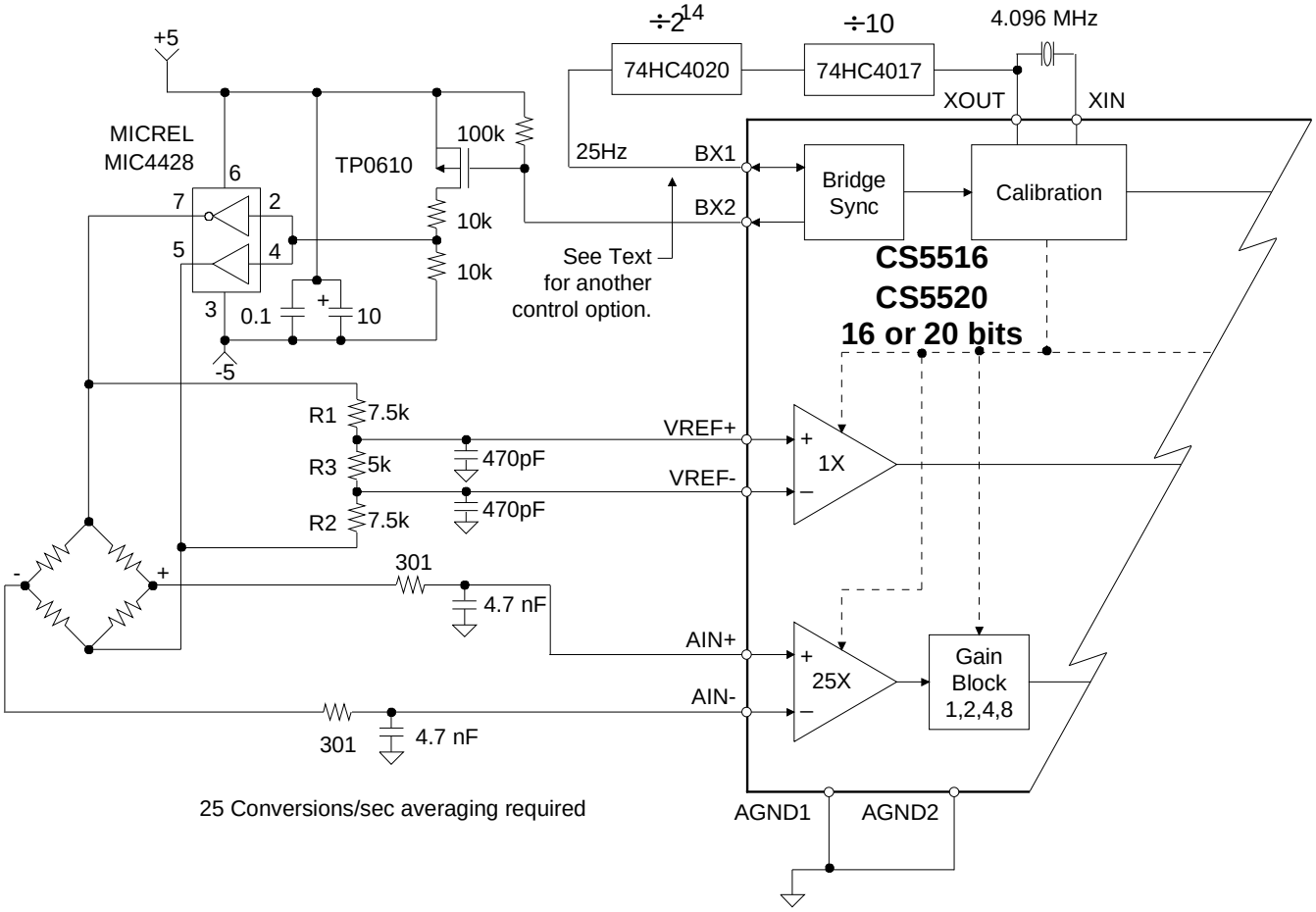



**Figure 15. CS5516 with External 25 Hz AC Excitation.**

excitation. In external excitation mode, the BX1 pin of the converter is an input and is used to determine the polarity of the excitation. The phase of the signal at BX1 controls the phase of the internal detection circuitry. Each time the polarity of the excitation is changed, the converter needs six conversion word periods for the internal digital filter to accurately settle on the input signal. To yield a proper result, the sixth conversion word for each of the excitation phases will need to be averaged together. For optimum throughput, the excitation polarity should be changed when the $\overline{\text{DRDY}}$ signal falls. The on-chip calibration features may not be usable directly when operating in this manner, but the user microcontroller can manipulate the gain and offset registers in the converter to optimize the the offset and gain adjustments for optimum operation. If the bridge polarity is reversed every six conversion words, an output result can be computed every twelve filter cycles. This will yield an effective conversion update rate of about four updates per second (XIN = 4.096 MHz).

### CS5516 or CS5520 and a 1 mV/V AC-Excited Load Cell

Metal film or metal foil strain gages are generally configured to yield a sensitivity of 2 mV/V or 3 mV/V from a load cell. A load cell may be used at 1/2 or 1/3 its rated capacity to allow it to have greater overload capacity. A designer may trade sensitivity for overload capability. For example, using a 2 mV/V load cell at 1/2 capacity yields a 1 mV/V sensitivity, but with greater ruggedness. The lower sensitivity results in less output signal for a given excitation. The usable portion of the output signal may be further reduced because the load cell may be part of a system where the pan weight consumes a good portion of the signal span of the load cell output. For example, a scale designed to weigh 10 Kg (22 lbs.) may have a pan weight which weighs 5 Kg. (11 lbs.) and therefore the pan weight consumes half of the signal span out of the load cell. The application may require protection against high impact, such as when the items being weighed are dropped on the scale. A 2 mV/V load cell may be derated which results in lower output sensitivity (1 mV/V or so) to allow greater impact capacity for the load cell.

Figure 16 illustrates such an application. The signal to measured from the bridge is only 5 mV over the measurement range (the pan weight consumes 5 mV of the load cell span). The offset calibration capability of the CS5516/CS5520 converter can readily remove the offset due to the pan weight. If the converter was configured to measure the 5 mV signal without the additional buffer amplifier, the 5 mV signal would only use part of the converter's span. For example, if the VREF voltage is reduced to 2.0 V and the PGA gain inside the converter is set to 8, the input span expected by the converter would be 2.0/(25 X 8) = 10 mV. To calibrate the converter with only a 5 mV signal would force the gain register to a value outside the recommended range (1.2 to 0.8). This situation can be overcome by using an external buffer amplifier made up of two OP-27 op amps. The VREF voltage for the converter is set to 3.33 V by using three equal resistors for R1, R2, and R3. The PGA gain is set to 1 which makes the input sensitivity at the AIN pins of the converter to be 3.33/(25 X 1) = 133 mV. The buffer amplifies the usable portion of the load cell output signal (5 mV) by a gain of 26 to yield an input to the converter of 130 mV. Stability of the gain resistors is important but tight initial tolerance is not needed as the gain calibration feature of the CS5516/CS5520 can accommodate up to ± 20% gain scaling. AC excitation removes the offset of the OP-27s.

The circuit is operated with the load cell excited with a 1 kHz bridge drive frequency. When operating in bipolar mode, the CS5516 converter will yield about 27,000 noise-free counts over

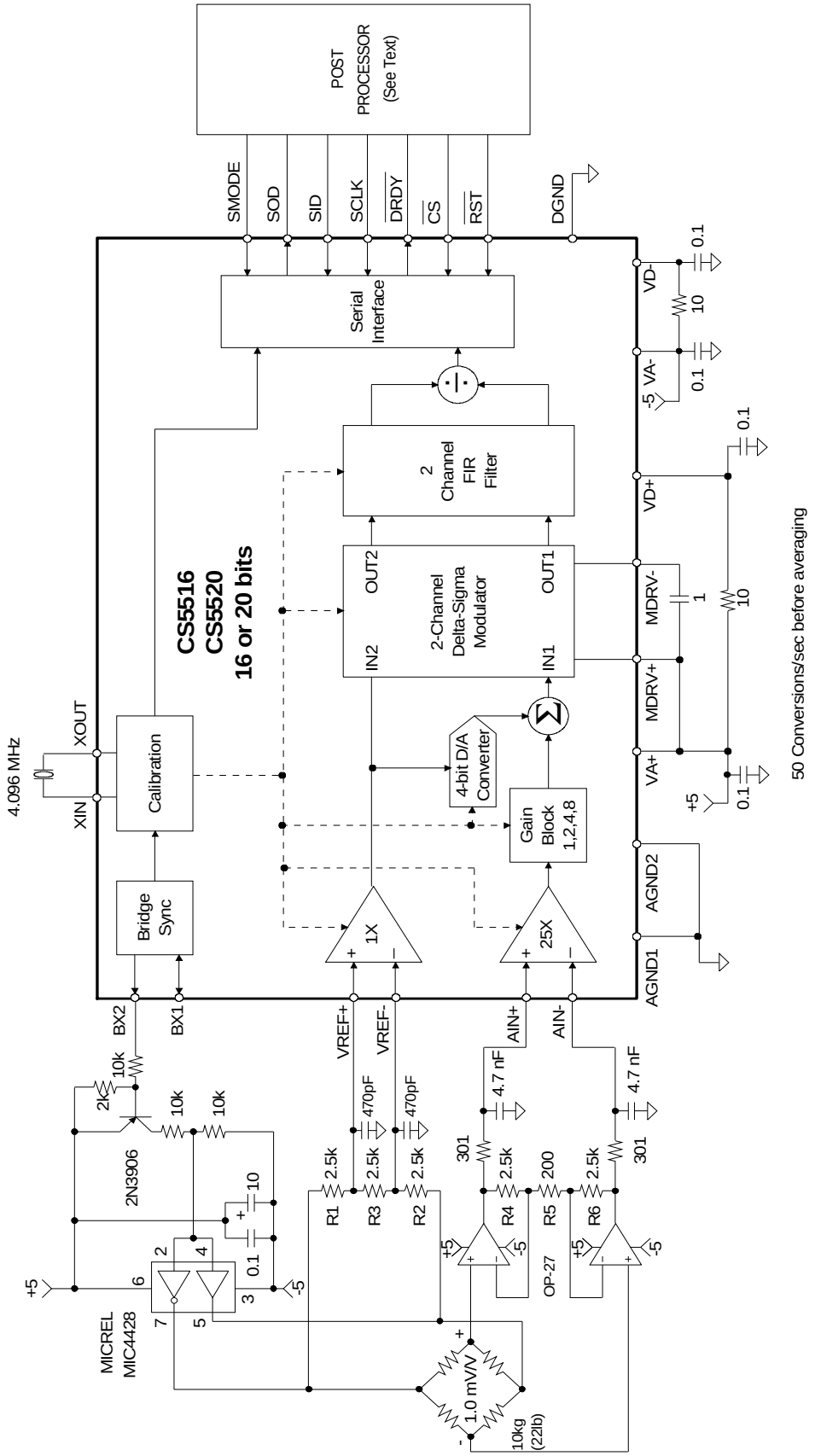



**Figure 16. CS5516 or CS5520 and a 1 mV/V AC-Excited Load Cell.**

the 5 mV span at a fifty samples per second update rate. The CS5520 should be used if higher resolution is desired at the 50 Hz update rate. Averaging 25 samples will yield an output with an effective 135,000 noise-free counts at two updates per second; this on a 5 mV signal span. The AIN ratiometric calibration register inside the converter can be used to add or subtract offset from the signal and give some counts for zero weight underflow (if used in unipolar mode) or some counts for full scale overrange (if bipolar mode is used). Averaging as many as fifty output words may be desirable in some applications where mechanical vibration is a problem.

### CS5520 and an AC-Excited 1.9 mV/V Weigh Platform

Figure 17 illustrates another very high resolution digitizer. A GSE model 4444 "floating beam" platform is used as the weigh bridge. The model 4444 has a full scale capacity of 100 pounds and a sensitivity of 1.9 mV/V. The full-scale output signal from the bridge is (1.9 mV/V) X 9.5 volts excitation or about 18 mV. The 18 mV output signal is amplified by two LT1115 amplifiers configured as a high input impedance buffer amplifier with a fixed gain of 8. When the 18 mV signal is amplified by 8 it yields an input signal to the converter slightly above the nominal value determined by the voltage reference. The calibration features of the CS5520 enable it to accommodate input spans which are as much as 20 % above or 20 % below the nominal value set by the reference voltage. Vishay resistors (R4-R6) are used in the buffer amplifier to maintain a stable gain over temperature. The LT1115 was chosen for its low noise while sustaining a loop gain greater than one million. With a X8 closed loop gain, an open loop gain of 138 dB must be maintained. The operational amplifier must maintain its high open loop gain with reduced supply voltages (±5 V) and with environmental temperature changes. A loop gain greater than one million ensures that gain stability will be dictated by the gain-setting resistors and not by limited loop gain. Offset voltage, offset drift, bias current, and bias current drift are unimportant when ac excitation is used as these errors are modulated out-of-band and filtered out by the digital filter inside the CS5520. Thermal noise at the excitation frequency remains as the limitation to achieving high dynamic range. Although the LT1115 is a very low noise amplifier, the noise in the digitizer circuit is actually dominated by noise referred to the buffer amplifier's input from the A/D. (Note that a lower cost amplifier such as the LT1007 can be used with only a minor increase (5%) in peak-to-peak noise). The effects of the thermal noise can be reduced by averaging output conversion words. With the digitizer using the LT1115s for optimum performance, you can capture output conversion words from the digitizer and examine the noise content in the 50 Hz conversion words. You should capture at least 1000 conversion words from the CS5520 to have a large enough sample to minimize statistical uncertainty. The input to the digitizer should be held at a stable value while the conversion words are captured. Once the samples are captured, a frequency distribution of the samples is computed and plotted. Spreadsheets such as Lotus or Quattro can be used to compute and plot the frequency distribution of the data. Figure 18 illustrates the histogram of 1000 50 Hz output samples from the digitizer of Figure 17. The histogram illustrates that the 50 Hz output words from the converter have a peak-to-peak noise amplitude which is less than 6 LSBs (least significant bits) 99% of the time. The noise in the output codes has a Gaussian characteristic and therefore averaging can be used to reduce its value. Averaging samples which include Gaussian noise will reduce the noise amplitude in proportion to the square root of the number of samples which are averaged together. The post processor computes an average of 50 CS5520 output words to yield a post-filtered output word

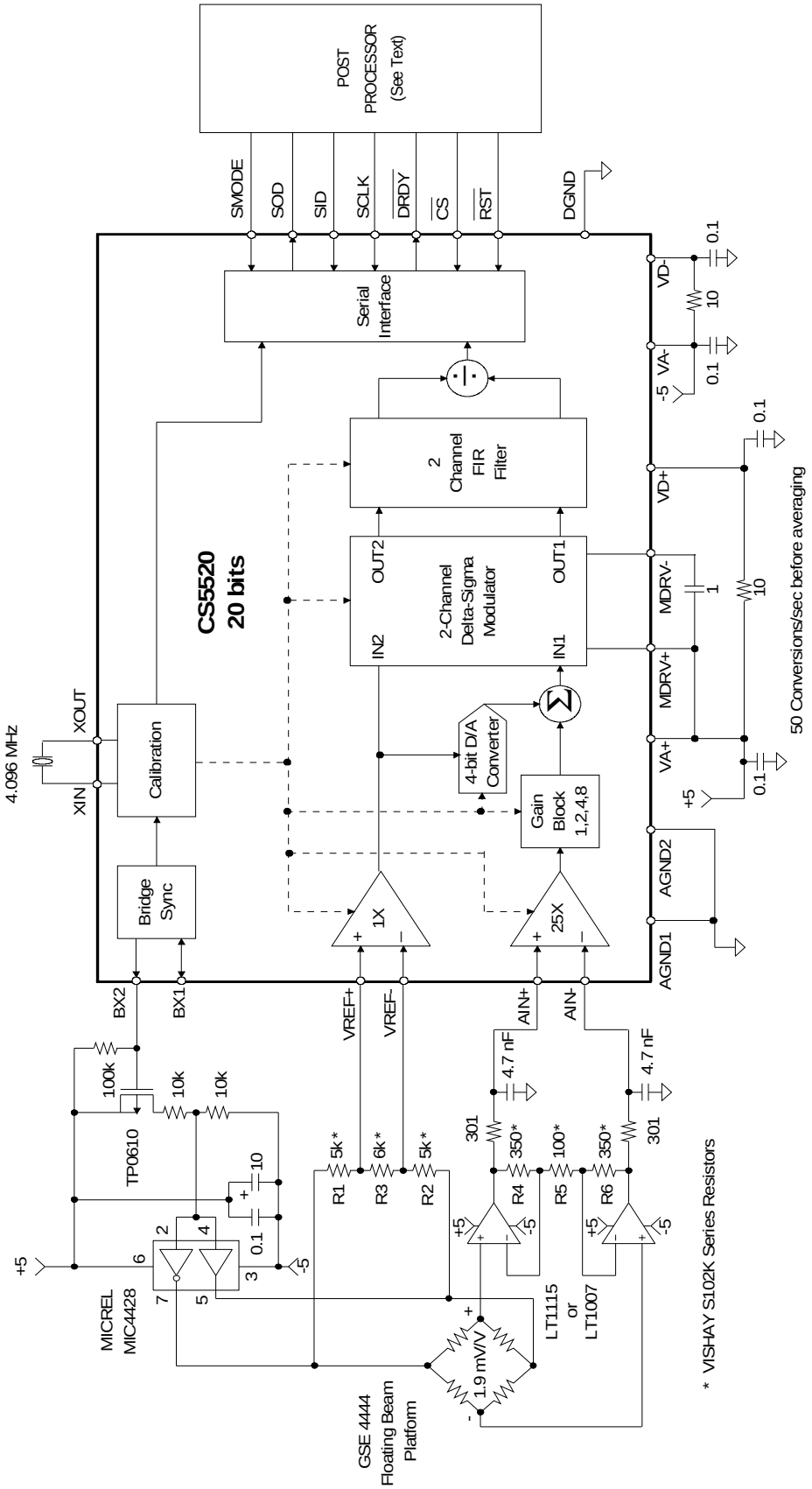



**Figure 17. CS5520 and an AC-Excited 1.9 mV/V Weigh Platform.**

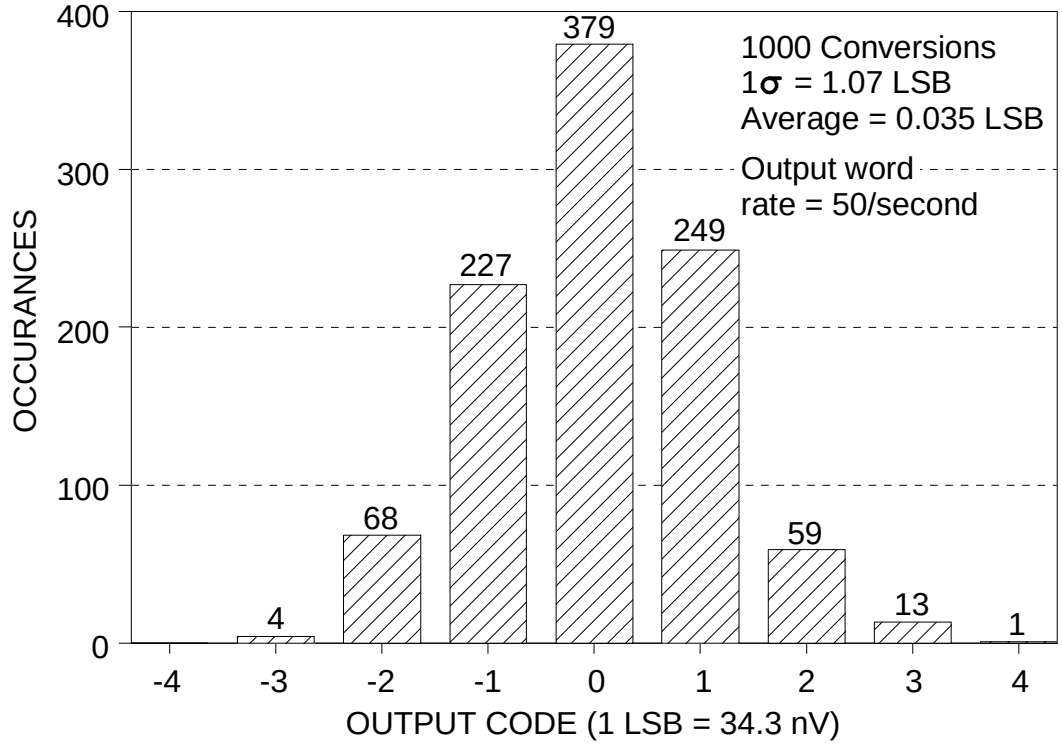



**Figure 18. Noise Histogram of 1000 Conversions.**

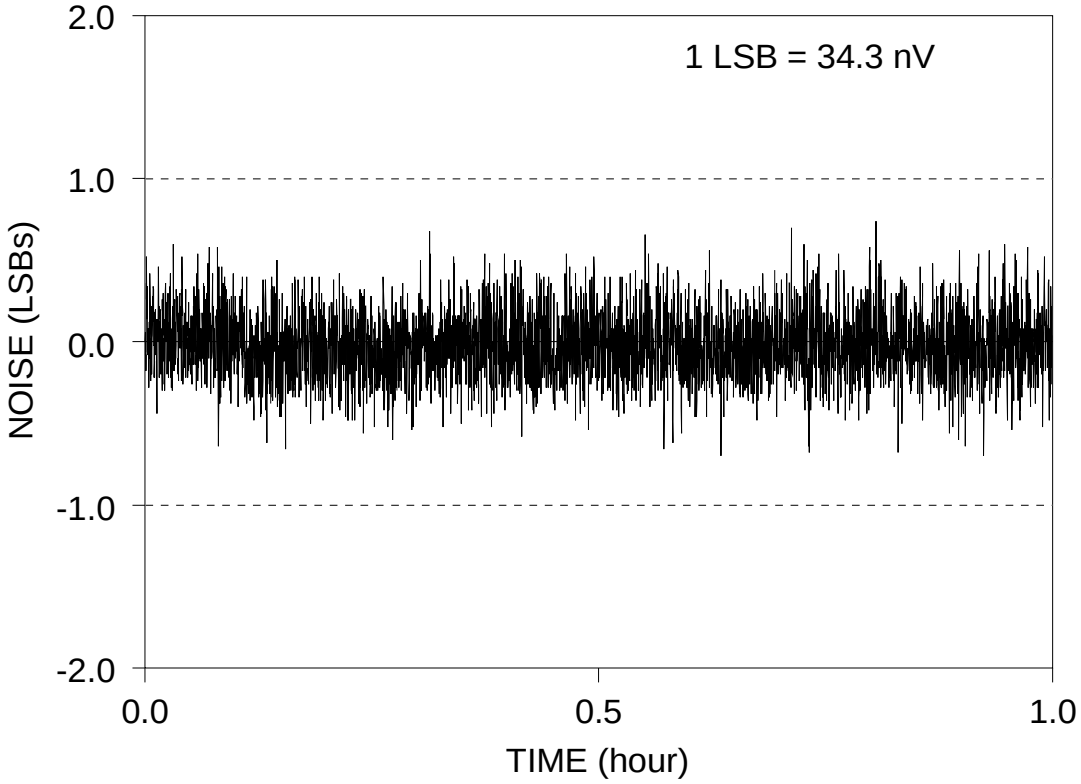



**Figure 19. Digitizer Stability Over One Hour.**

rate of 1/second. Averaging 50 words reduces the noise by $\sqrt{50}$, or by a factor of 7.07. Since the standard deviation, or rms value of the noise illustrated in Figure 18 is 1.07 LSB, the rms output noise in the post-filtered samples will be 1.07/7.07 = 0.151 LSB rms. You can use the rule of thumb that peak to peak noise is approximately 6 to 6.6 times greater than the rms value to predict the peak-to-peak noise in the post-processed output words. This results in a peak- to-peak noise in the post-filtered output words of less than ±1 LSB for greater than 99.9% of the post-filtered output words.

To illustrate the dc stability and noise of the post-filtered output words over time, the 1 Hz post-filtered output words were collected for a period of one hour. Note that for this test the input to the bridge amplifier was removed from the load cell and tied to ground through two 350 ohm resistors. This eliminates the load cell's sensitivity to vibration when studying the digitizer input noise characteristics.

Figure 19 illustrates the peak-to-peak noise of the digitizer over a one hour period. The plot indicates that the drift and noise are less than ±1 LSB for more than 99.9% of the output samples over the hour long period. This is superb performance and illustrates the benefit of synchronous detection. Figure 18 and Figure 19 indicate that the 50 Hz output data from the converter can averaged to yield a 1 Hz update rate which is stable to 1 count in ±524,000 when the converter is set up for bipolar mode. The CS5520 includes a DAC and a ratiometric offset register which can be used to offset the span in a negative direction by 500,000 counts. This allows the weigh scale to have 24,000 counts of underrange to accommodate any zero drift or creep in the load cell. The measurement span for the 18 mV load cell output would be over 524,287 counts, but above this would be another 500,000 counts which would allow the digitizer to accurately measure overranged weights. In this configuration the digitizer can accurately digitize an overrange signal, even up to 195% of full scale.

The GSE 4444 platform has mechanical stops which activate at approximately 120% of capacity, so the synchronous detection weigher will yield a noise-free 19-bit measurement, with a 20% overrange capacity. If the digitizer was used with a tension-compression load cell such as the BLH Electronics model LPT, the digitizer would yield better than ±500,000 noise-free counts.

**Digitizer Noise And Averaging**

As illustrated in the previous example circuit, it is good practice to evaluate the performance of a prototype digitizer. While many measures of performance should be investigated (linearity, stability over temperature, etc.), one of the primary factors which limits measurement resolution is noise in the digitizer circuit itself.

Investigating the noise performance of the digitizer should begin in the design phase. Analysis should yield an estimate of the amount of noise in the circuit. This discussion will not focus on the analysis but will instead be limited to evaluating the noise in the digitizer circuit.

One simple method of evaluating digitizer noise is to "ground" the input and collect enough samples to evaluate the noise statistically. "Grounding" the input involves connecting the signal + and signal - leads of the digitizer input amplifier to a quiet node which has a voltage equivalent to the common mode output of the bridge to be measured. In a system with load cell excitation of +5 V and -5 V the inputs can be tied to ground. If the load cell is excited with a single supply ( for example, +5 V or +10 V), a quiet source with a common mode voltage compatible with the input of the amplifier should be generated. For example, if the circuit runs on

a single +5 V supply, use two 100 ohm resistors connected in series between +5 V and ground. Then connect the input of the digitizer circuit to the 2.5 V node of the resistor pair. While a load cell simulator may be used in many circumstances, this can be a source of some problems. Some simulators exhibit 1/f noise which can adversely affect the data output from a high resolution digitizer. And some simulators may not work well with the circuits which use ac-excitation. This is because some simulators use switches which rectify the ac excitation signal; therefore the actual signal to be measured is corrupted. This can result in greater noise than expected as well as a dc offset error.

The biggest difficulty in evaluating the noise performance of a circuit is that some means of getting the data out of the digitizer and into a computer must be designed into the circuit. For the CS5504/5/6/7/8/9 devices this can be accomplished by making the SCLK, SDATA and $\overline{\text{DRDY}}$ signals available on a header. The CDBCAPTURE system from Crystal has a standard 10 pin (two rows of 5 pins) stake header which can interface to the CS5504/5/6/7/8/9 products and capture data from these converters. Alternatively, a designer may include some other type of interface in his system to port data to a PC-compatible computer via the serial or parallel port.

Once an interface is available, it is a matter collecting enough conversion words to perform meaningful statistical analysis on the data. The CDBCAPTURE system enables the user to capture data from the CS5504/5/6/7/8/9 and to produce noise histograms. The CS5516 and CS5520 are not supported with the CDBCAPTURE system, but the CDB5516 or CDB5520 evaluation boards can be configured to collect data from these chips. Once data has been collected into a file on a computer, spreadsheets such as Quattro, Lotus, or Excel can be used to analyze the data using a frequency distribution function and statistical functions. The data should also be plotted as shown in Figure 18 to give the user an indication that the data actually follows a Gaussian (Normal) distribution. Thermal noise will have a "bell-shaped" histogram. If the data words represent thermal noise, one standard deviation is equivalent to the rms noise; while 99.9% of all the data should fall within ± 3.3 standard deviations of the mean. Therefore the peak-to-peak noise is approximately 6.6 times the rms noise. When performing statistical analysis on a digitizer's output, at least 500 to 1000 conversion words should be included to lower statistical uncertainty to an acceptable level.

Once the rms noise is known (by calculating the standard deviation of the data set), averaging can be used to improve system resolution if it has been confirmed that the noise follows a Gaussian distribution. Data may not follow a Gaussian distribution because it includes interference due to dc-dc converters or to clock coupling which is picked-up by the sensitive analog circuitry. In this case averaging output words may be deceptive. Averaging will reduce the peak-to-peak noise but the mean can be adversely affected by the interference which is included with the signal.

One additional noise test is to measure noise over the entire input span of the converter. If noise increases with higher signal amplitudes, it suggests the voltage reference input to the converter is excessively noisy.

**Conclusion**

The circuits in this application note were designed, constructed, and tested with the intent of illustrating a wide variety of bridge digitizer solutions. The circuits demonstrate various power supply arrangements and various levels of measurement resolution; all with the intent of helping designers understand the flexibility of the A/D converters which have been used.

# • Notes •