Application Note

Clock Options for A/D Converters

by
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Most A/D converters require a clock source for operation. Some converters, such as the CS5101A, CS5102A, CS5501/3, and the CS5504/5/6/7/8/9 include an on-chip gate oscillator as shown in Figure 1. A Pierce-oscillator architecture is commonly used. It is constructed with either on-chip loading capacitors (C2 and C3 in Figure 1) or it may require off-chip loading capacitors (C4 and C5) depending upon the crystal frequency. The data sheet for the particular A/D converter should give instructions regarding the size of any external loading capacitors.

System applications may require the A/D converter clock to drive other circuits; or the measurement system may require two or or more A/D converters to be driven from the same clock. It is always preferable for one common clock to be used for the entire system. With one system clock, any interference will be synchronous and will generally be less severe.

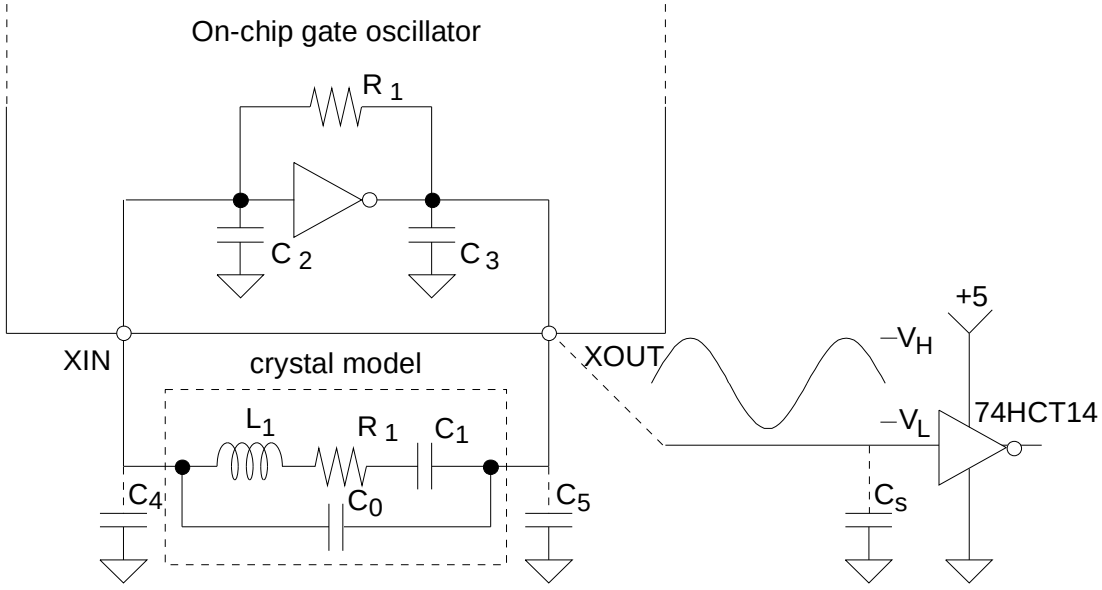

Figure 1. Using 74HCT14 Gate to Buffer Oscillator Output

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To drive external circuitry from the on-chip oscillator of an A/D converter use the XOUT or CLKOUT pin. Although the on-chip oscillator is shown as an inverter gate, this does not mean that it can drive external circuitry very well. The gate oscillator circuit is optimized for low gain to facilitate building a stable oscillator; and the circuit may be optimized to minimize power dissipation in the oscillator. For example, the on-chip oscillator of the CS5504/5/6/7/8/9 devices uses only 10 µA of supply current. It is therefore necessary to buffer the oscillator output with a high impedance gate input such as CMOS logic. The CS5504/5/6/7/8/9 devices work well with a 74HCT14-type gate. The HCT threshold is required as the oscillator output oscillates between 0 - 2.5 volts. The external gate should be located very near to the XOUT pin of the converter to minimize stray capacitance. The same technique can be used with the CS5101A/02A and CS5501/03 converters. When using external loading capacitors (C4 and C5 in Figure 1) and an external gate to buffer the oscillator output, the value of C5 should be lowered by the estimated input capacitance of the CMOS gate input and any additional stray capacitance. For example, the oscillator by itself may call for C5 to be 30 pF. But if the oscillator output is driving an external CMOS gate, the gate input may have 5-10 pF of input capacitance and there may be 1-4 pF of stray capacitance. Under these conditions the value of C5 should be lowered, say to 22 pF, so that the total capacitance seen at the output of the on-chip gate oscillator is maintained near 30 pF.

Some applications may use a central oscillator which is then distributed as shown in Figure 2. The oscillator may use a logic gate, a clock module, or an oscillator chip such as the Harris HA7210. Buffers are then used to drive the system circuitry. To minimize clock jitter, the power supply to the oscillator, whether it be a gate or a module, should be decoupled with an RC filter to keep any noise on the power supply from reaching the oscillator.

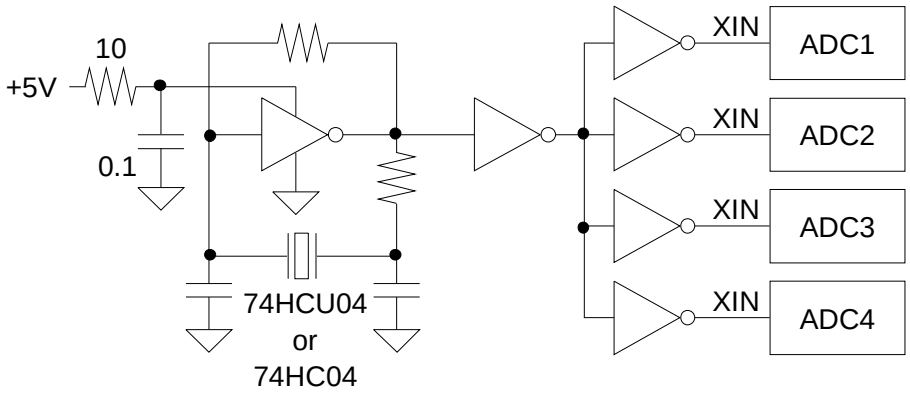


Figure 2. External Oscillator using Buffers for Distributed Clock

Working with gate oscillators can present some difficulties. For example, just looking at the output with a scope probe loads the oscillator with the probe capacitance. This can change the oscillator frequency, the signal amplitude, or even cause the oscillator to quit oscillating. Use a low capacitance or active probe if possible. A series resistance can be added between the circuit and a standard probe to minimize the effects of the scope capacitance as shown in figure 3. Choose R to be 5-10 times greater than the impedance of the output loading capacitor (at the frequency of oscillation).

Customers have asked whether the on-chip gate oscillators used in Crystal A/Ds call for series or parallel-type crystals. The only difference between series and parallel-type crystals is the method by which their fundamental frequency is calibrated. The frequency at which series crystals are calibrated to oscillate is a function of the crystal's internal inductance (L_1) and its internal series capacitance (C_1) of figure 4. These resonate in series to produce zero phase shift through the crystal network. Series-mode oscillators use non-inverting amplifiers.

Parallel-mode crystals are calibrated using the crystal's internal inductance and its internal parallel capacitance in parallel with external loading capacitors. Parallel-mode oscillators require an inverting amplifier which contributes 180 degrees phase shift along with the 180 degrees phase shift contributed by the network composed of the crystal and the loading capacitors.

All of the converter chips mentioned in this application note use parallel-mode oscillators, but either series or parallel mode crystals will

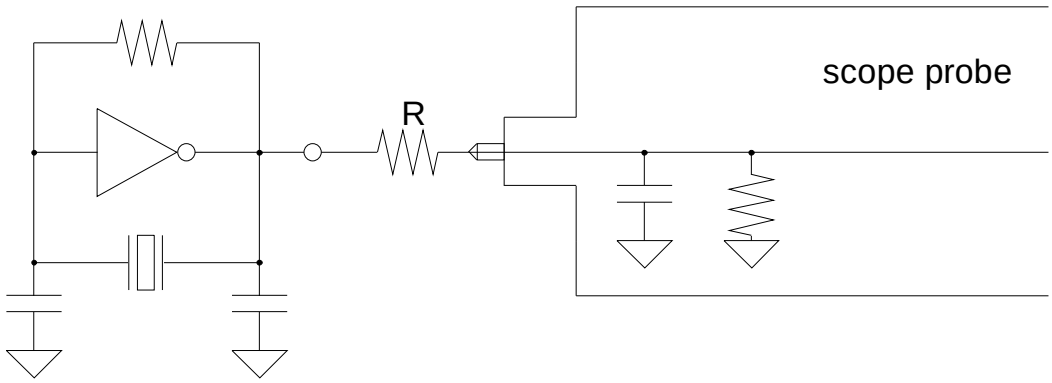
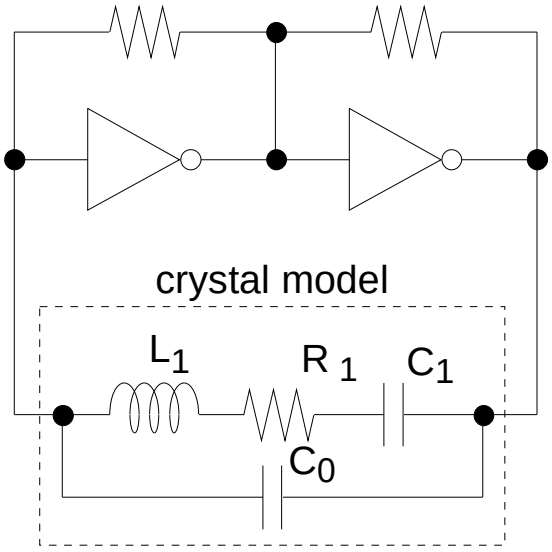


Figure 3. Isolate Scope Probe Capacitance to prevent Oscillator Loading.

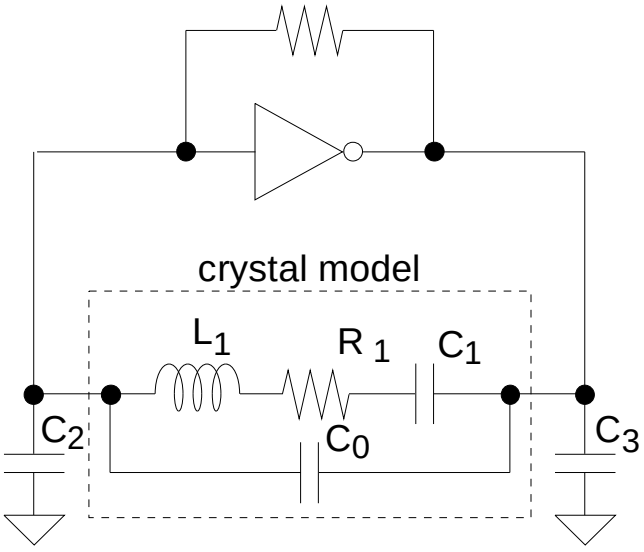
oscillate. When using a series-mode crystal in parallel mode, its oscillation frequency may be off a small percentage, never more than 0.5%. This will not cause problems unless the clock is used for time-keeping purposes.

Parallel resonant crystals always require a specified load capacitance. For example, a parallel crystal may be specified as 8.000 MHz (20 pF); meaning that the crystal will oscillate at exactly 8.000 MHz if loaded with exactly 20 pF. This would require C_2 and C_3 of figure 5 to be 2 X 20 pF (39 pF typical). This is because the capacitors are series-connected, which divides the effective capacitance.



$$f = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

Figure 4. Series Resonant Crystal Oscillator.



$$f = \frac{1}{2\pi}\sqrt{\frac{1}{L_1 C_1} + \frac{1}{L_1 C_T}}$$

$$C_T = C_0 + \frac{C_2 \times C_3}{C_2 + C_3}$$

Figure 5. Parallel Resonant Crystal Oscillator.