Application Note

CS5516 and CS5520: Overcoming Errors in Bridge Transducer Measurement

The CS5516 and CS5520 Bridge Transducer A/D converters address many of the common error sources encountered when digitizing bridge transducers. This application note describes many of these error sources and explains how to minimize their effects. Many of the features of the CS5516 and CS5520 which allow for the control of these error sources are also discussed. Some of the content of this application note was originally a portion of the CS5516 and CS5520 data sheet and was titled" Enemies of the Strain Gauge".

Strain gages are sensing devices which change resistance when subjected to mechanical stress. The amount of stress to which the gage is exposed is usually limited to minimize possible damage to the gage due to overstress. A strain gage is a passive electrical device. Most often gages are configured in a Wheatstone bridge configuration to enhance their sensitivity while minimizing the effects of drift. The bridge may be excited with either a voltage or a current. Excitation is supplied through connecting leads to the bridge. The connecting leads will include resistances (R_{p1} and R_{p2}) as shown in Figure 1. These resistances will affect the gain of the bridge:

$$A_V = \frac{AIN+ - AIN-}{VEXC+ - VEXC-}$$

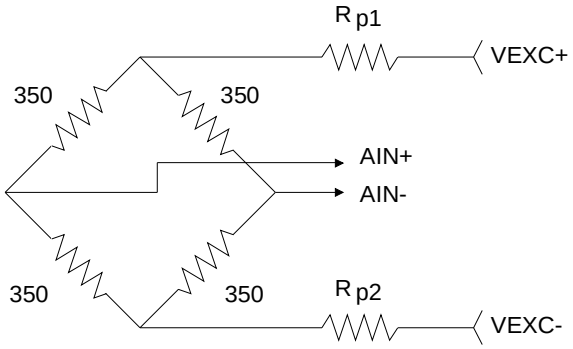

Figure 1. Four-Wire Bridge

When a bridge connected gage set is included as part of a mechanical assembly (often called a load cell), a connecting cable is often included. Manufacturers will include the errors due to R_{p1} and R_{p2} in the specification for the load cell assembly.

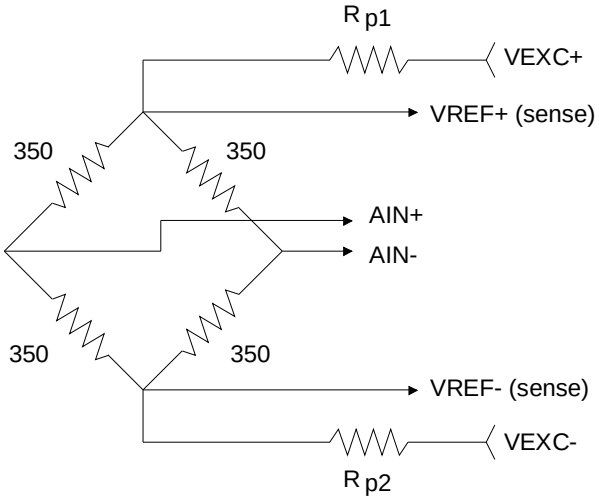

Figure 2. Six-Wire Bridge

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581
http://www.crystal.com

A six-wire bridge, as shown in Figure 2, allows for force and sense (Kelvin connection) leads to measure the excitation directly at the bridge. This allows all errors due to R_{p1} and R_{p2} to be removed if a ratiometric measurement system (as provided by the CS5516 and CS5520) is employed.

Bridge Offsets

It is common for bridge configured load cells to have a zero offset specified to be as great as ±10% of the full scale output signal. In a typical digitizer this offset must be "trimmed out" by adjusting a potentiometer. This may be necessary to reduce the portion of the dynamic range of the measurement system which is consumed by the offset of the load cell. In some weighing systems, another source of offset which may consume dynamic range is the pan weight; sometimes called the tare weight. Prior to making a weighing, an empty pan is placed on the scale. Then a zero or tare button is activated and signals the digitizer to remove the offset produced by the empty container. After the offset due to the pan weight is removed, the actual item to be measured is then added to the pan. Pan weight can consume a large portion of the dynamic range of the digitizer depending upon the method by which it is removed from the measurement.

The CS5516 and CS5520 converters include a 4-bit offset trim DAC. The DAC allows the removal of up to ±200% of the selected range's full scale before the signal is digitized. This avoids the loss of resolution in the digitizer caused by load cell or pan weight offsets. The converters also include a ratiometric offset calibration register which can be calibrated or manipulated to add or subtract offsets from the digital output words after conversion has been performed. This allows the transfer function of the converter to be offset (either plus or minus) to accommodate load cell zero drift or load cell creep.

Of critical importance when removing offset is for the DAC output to remain ratiometric to the voltage reference if the voltage reference should change. The CS5516 and CS5520 converters are designed to perform ratiometric, non-reference sensitive offset removal.

50/60 Hz Pickup

It is common in some weighing applications for the load cell to be located some distance from the digitizer. The load cell leads can become exposed to radiated noise caused by line interference at 50 or 60 Hz. Twisted pair interconnections should always be used on the AIN+, AIN- and VREF+, VREF- pairs to minimize 50/60 Hz pickup. Nonetheless, some amount of line interference is inevitable.

The line interference may enter into the A/D converter circuitry by either the AIN signal input or the VREF input (Line interference may also appear on the power supply leads, in which the power supply rejection of the A/D converter is an important issue, but in this discussion the focus is on the interference picked up by the transducer leads).

When line interference enters the AIN and VREF inputs of a traditional A/D converter, the interference will most likely introduce errors into the output words of the converter. To understand why, assume that 60 Hz interference enters into the converter by means of both the AIN and VREF inputs. The AIN signal is:

$$AIN+ - AIN- = V_{IN} + b\cos(2\pi 60t)$$

Assuming the input and reference paths are well matched, the VREF input would be:

$$VREF+ - VREF- = V_{REF} + b\cos(2\pi 60t)$$

The A/D converter computes the ratio:

$$\frac{AIN}{VREF}$$

The dc component of the A/D output is obtained by averaging the ratio of AIN/VREF over a 60 Hz period of T = 16.7 msec. The AIN and VREF inputs include the interference component $b\cos(2\pi 60t)$ as shown in the previous equations:

$$\frac{1}{T}\int_0^T \frac{AIN+ - AIN-}{VREF+ - VREF-}\,dt = 1 + \frac{V_{IN} - V_{REF}}{\sqrt{V_{REF}^2 - b^2}}$$

To develop a feel for this result, let's define some real input conditions as an example. Assume a typical converter has a full scale span of 2.5 volts (VREF = 2.5) and the input signal AIN is 0.6 volts. The converter would output a digital code which states that the input is a ratio of 0.6/2.5 or 0.240 of full scale. If there is no line interference on the AIN and VREF inputs, that is b = 0, (no interference pickup), the output result from the equation above is AIN/VREF= 0.6/2.5, or 0.240 as desired. If the interference is not zero, that is, b0, (let's say the line interference has a magnitude of 10 mV, that is 0.010) the output result will include an error caused by the interference. The result will be:

$$1 + \frac{V_{IN} - V_{REF}}{\sqrt{V_{REF}^2 - b^2}} = 1 + \frac{0.6 - 2.5}{\sqrt{2.5^2 - 0.010^2}}$$

or

$$1 + \frac{0.6 - 2.5}{2.499980} = 0.2399939$$

If we take the ratio 0.2399939/0.240 = 0.9999745

The result is 25.5 ppm less than it would have been, had the measurement not included the interference. 25.5 ppm is equivalent to about 26-27 counts error in a 20-bit A/D converter; or 1.66 counts error in a 16 bit A/D converter.

Note that the error when interference is present will be zero only if AIN = VREF, that is only if the AIN signal is a full scale input with the same magnitude (including line interference) as on the VREF input. This measurement condition is unlikely to occur.

We see that line interference can cause measurement errors. Interference into only the voltage reference input can introduce similar errors into the converter.

The CS5516 and CS5520 converters minimize errors due to line interference because the AIN and VREF inputs to the converter are actual independent A/D converters which use a common voltage reference which is internal to the converter chip. Each of the two signals (AIN and VREF) are converted and processed by independent digital filters before the AIN/VREF ratio is computed. With an appropriate choice of operating clock frequency for the converter, the digital filters remove 50 and 60 Hz (and their harmonics). The robustness of the conversion output is significantly enhanced when operating in harsh 50/60 Hz environments.

Non-Ratiometric Errors

A variety of offset sources can introduce errors into the measurement which do not scale with the excitation voltage; hence the name non-ratiometric errors. Amplifier offset voltages and parasitic thermocouples are two common non-ratiometric offsets. The measurement errors which can be caused by non-ratiometric offsets will be examined more closely and then parasitic thermocouples will be discussed more thoroughly.

The first offset to be considered is shown as V_{OS} in Figure 3. The ADC output is given by:

$$D_{OUT} = \frac{V_{IN}}{V_{REF}} = A_V + \frac{V_{OS}}{V_{REF}}$$

The sensitivity of D_{OUT} to changes in the excitation voltage will be termed S_1:

$$S_1 = \frac{\delta D_{OUT}}{\delta V_{REF}} \frac{V_{REF}}{D_{OUT}} = \frac{-V_{OS}}{A_V V_{REF} + V_{OS}}$$

Some practical values illustrate the significance of this equation. Suppose the sensitivity of the load cell is 2 mV/V (A_V = 0.002) and the excitation supply (VREF) is 10 V. Assume that V_{OS} = 20 µV and that it is a non-ratiometric offset generated by a parasitic thermocouple or by the offset of a precision amplifier. This yields a sensitivity S_1 = 0.001. Sensitivity factor S_1 is a measure of the sensitivity of the converter output code D_{OUT} to changes in the excitation supply. The excitation supply may drift due to temperature changes or due to limited line and load regulation. A typical regulator may change 1% over changing line, load, and temperature changes. With S_1 = 0.001 a typical 1% change in the excitation supply will cause a 0.0001% change, or a 10 ppm change in D_{OUT}. This 10ppm error is in addition to the error introduced by the 20 µV offset itself. This 10 ppm error is significant, being 10 counts in a 20-bit converter or 2/3 count in a 16-bit converter.

The above equation suggest three methods of reducing V_{OS}-induced errors:

1) Buy a gauge with a large A_V.
2) Use a large excitation voltage (VREF).
3) Measure V_{OS} and calibrate it out.

The CS5516 and CS5520 converters include the features necessary to calibrate out non-ratiometric offsets. Calibration is only effective if the non-ratiometric offsets are stable after being calibrated. The converters also support ac

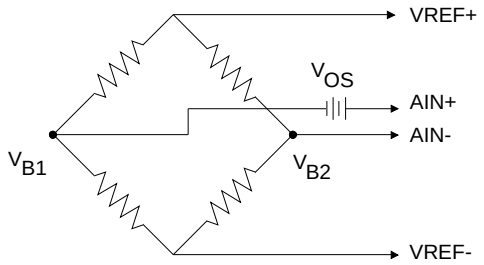

Figure 3. V_{OS} Offset

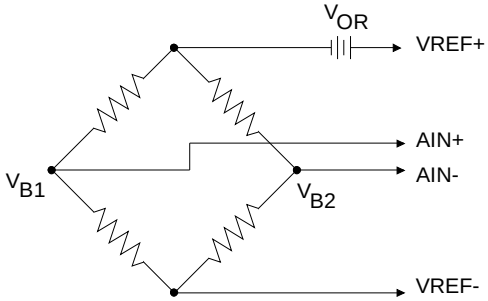

Figure 4. V_{OR} Offset

bridge excitation which removes the effects of non-ratiometric offsets (more on this later).

A second non-ratiometric error is shown as V_{OR} in Figure 4. Its sensitivity is given by:

$$S_2 = \frac{\delta D_{OUT}}{\delta V_{REF}} \frac{V_{REF}}{D_{OUT}} = \frac{-V_{OR}}{V_{REF} - V_{OR}}$$

Not surprisingly, in this case increasing A_V doesn't help.

Sensitivities S_1 and S_2 simply confirm that, when non-ratiometric errors are present, the A/D converter output will vary as the excitation voltage changes. A zero tempco, zero aging, excitation supply with perfect line and load regulation can reduce this variation, but one major advantage of a ratiometric measurement system should be that a precise, stable reference is not necessary.

Again the non-ratiometric calibration capabilities of the CS5516 and CS5520 can remove the adverse effect of V_{OR}.

Thermocouples

A common source of non-ratiometric error is the parasitic thermocouple. Thermocouples result any time that two dissimilar metals are joined. Common tin-lead solder and copper traces of a PC board create a thermocouple junction with a thermal EMF (electro-motive force) of 3.1-3.4 µV/°C. It is common for components such as resistors to have wire leads composed of different metal alloys than the resistor element itself. Therefore each end of the resistor has a thermocouple junction as an integral part of the resistor. Soldering the leads to the circuit board traces creates more thermocouple junctions. It is imperative that low level measurement circuits have an identical number of junctions in the differential signal path and that differential inputs be routed next to each other. Interconnecting devices (connectors and IC sockets) and relays should be chosen to minimize thermocouple effects. A circuit board layout should optimize trace and junction placement, and component placement and orientation, to match the thermocouple effects of a differential signal path. While perfectly matched thermocouple chains produce zero differential inputs, thermal gradients exist in any "real world" measurement system. Temperature dependent non-ratiometric offsets result.

The use of non-ratiometric offset calibrations can substantially reduce thermocouple errors. Nonetheless, temperature gradient fluctuations are difficult to eliminate. In addition to non-ratiometric offset calibration of the AIN and VREF channels the CS5516 and CS5520 converters also support ac bridge excitation. AC bridge excitation can help minimize the errors caused by parasitic thermocouples.

AC excitation, as shown in Figure 5, alternately flips the excitation voltages at the top and bottom of the bridge.

With ac excitation, the desired signal flips in polarity as the excitation voltage flips. The analog input becomes a square wave at the excitation frequency as the excitation voltage flips. V_{OS} doesn't flip. When the CS5516/20 synchronously demodulates the square wave in ac excitation mode, V_{OS} is modulated up into the digital filter's rejection band. V_{OS} problems are just filtered away.

Any systems design that can exploit the benefits of ac excitation probably should. Accuracy fluctuations with temperature can be virtually eliminated. Any remaining non-ratiometric errors can still be attacked with non-ratiometric calibrations when ac excitation is used. The CS5516/20's BX1 and BX2 pins provide for both internally and externally controlled excitation signals.

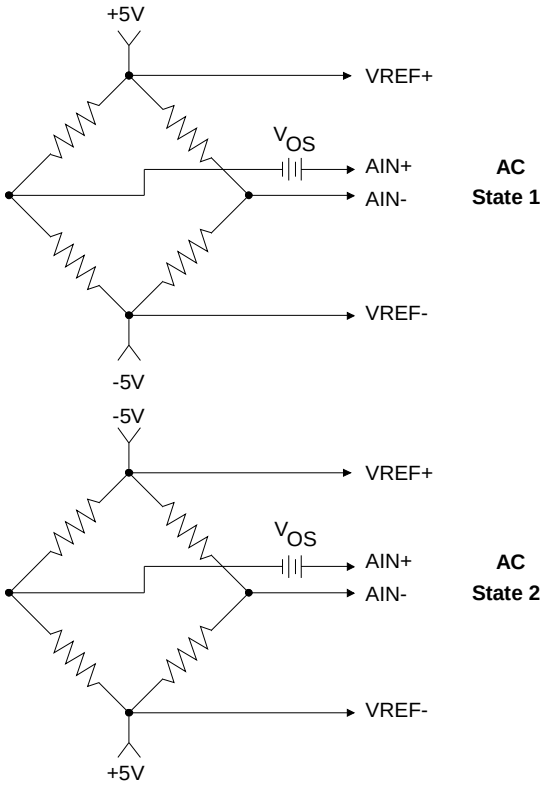

Figure 5. AC Excitation

Offsets due to leakages

Moisture or other contaminants in load cell cables or on the printed circuit board can cause current leakage paths, one of which is illustrated in Figure 6.

The current source model is appropriate since the resistance of the leakage path is often much larger than that of the gage. Comparison with Figure 5 reveals that both ac excitation and non-ratiometric calibration serve to reduce measurement errors due to these leakage current paths.

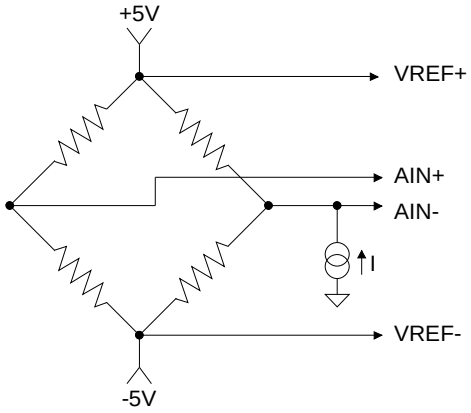

Figure 6. Leakage Effects Offset

Conclusion

This application note has presented some of the errors encountered in bridge transducer digitizers, and has indicated how the CS5516 and CS5520 A/D converters can overcome these errors.