CRYSTAL ®

24-Bit 105 dB Audio Codec with Volume Control

Features

- 105 dB Dynamic Range A/D Converters
- 105 dB Dynamic Range D/A Converters
- 110 dB DAC Signal-to-Noise Ratio (EIAJ)
- Analog Volume Control (CS4224 only)
- Differential Inputs / Outputs
- On-chip Anti-aliasing and Output Smoothing Filters
- De-emphasis for 32, 44.1 and 48 kHz
- Supports Master and Slave Modes
- Single +5 V power supply
- On-Chip Crystal Oscillator
- 3 - 5 V Digital Interface

Description

The CS4223/4 is a highly integrated, high performance, 24-bit, audio codec providing stereo analog-to-digital and stereo digital-to-analog converters using delta-sigma conversion techniques. The device operates from a single +5 V power supply, and features low power consumption. Selectable de-emphasis filter for 32, 44.1, and 48 kHz sample rates is also included.

The CS4224 includes an analog volume control capable of 113.5 dB attenuation in 0.5 dB steps. The analog volume control architecture preserves dynamic range during attenuation. Volume control changes are implemented using a "soft" ramping or zero crossing technique.

Applications include digital effects processors, DAT, and multitrack recorders.

ORDERING INFORMATION

CS4223-KS	-10 to +70 °C	28-pin SSOP
CS4223-BS	-40 to +85 °C	28-pin SSOP
CS4224-KS	-10 to +70 °C	28-pin SSOP
CS4224-BS	-40 to +85 °C	28-pin SSOP
CDB4223/4		Evaluation Board
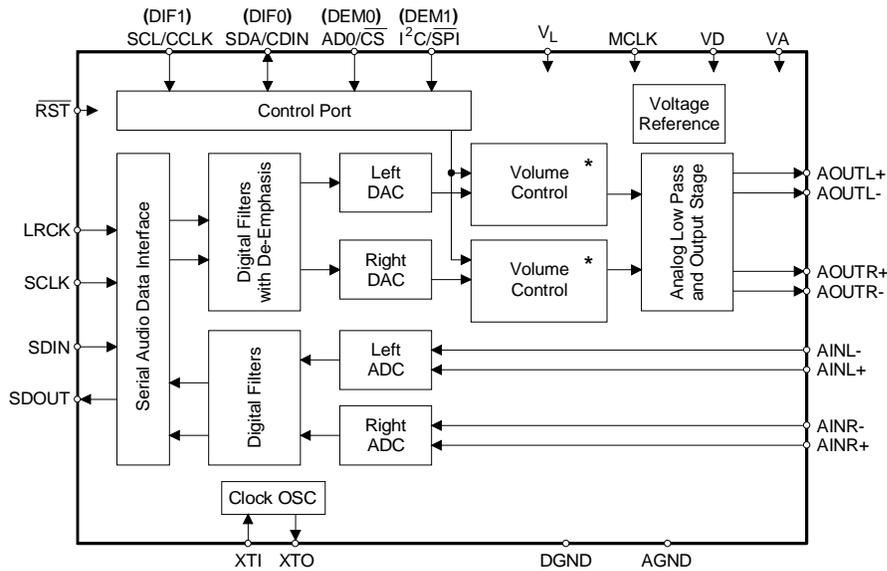
( ) = CS4223   * = CS4224

Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support
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http://www.cirrus.com/corporate/contacts/

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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25° C; VA, VD = +5 V; Full Scale Input Sine wave, 997 Hz;

Fs = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Local components as shown in Figures 4 and 5; SPI® mode, Format 0, unless otherwise specified.)

Parameter	Symbol	CS4223/4 - KS			CS4223/4 - BS			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Input Characteristics								
ADC Resolution		-	-	24	-	-	24	Bits
Total Harmonic Distortion	THD	-	0.0014	-	-	0.0014	-	%
Dynamic Range A-weighted		100	105	-	95	105	-	dB
unweighted		97	102	-	92	102	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N	-	-97	-92	-	-97	-87	dB
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	-	0.1	-	-	0.1	dB
Offset Error with High Pass Filter		-	-	0	-	-	0	LSB
Full Scale Input Voltage (Differential)		1.9	2.0	2.1	1.9	2.0	2.1	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Input Resistance		10	-	-	10	-	-	kΩ
Input Capacitance		-	-	15	-	-	15	pF
Common Mode Input Voltage		-	2.3	-	-	2.3	-	V
A/D Decimation Filter Characteristics								
Passband (Note 2)		0	-	21.8	0	-	21.8	kHz
Passband Ripple		-	-	±0.01	-	-	±0.01	dB
Stopband (Note 2)		30	-	6114	30	-	6114	kHz
Stopband Attenuation (Note 3)		80	-	-	80	-	-	dB
Group Delay (Fs = Output Sample Rate) (Note 4)	t_{gd}	-	15/Fs	-	-	15/Fs	-	s
Group Delay Variation vs. Frequency	Δt_{gd}	-	-	0	-	-	0	µs
High Pass Filter Characteristics								
Frequency Response -3 dB (Note 2)		-	3.7	-	-	3.7	-	Hz
-0.1 dB		-	20	-	-	20	-	Hz
Phase Deviation @ 20 Hz (Note 2)		-	10	-	-	10	-	Degree
Passband Ripple		-	-	0	-	-	0	dB

Notes: 1. Referenced to typical full-scale differential input voltage (2 Vrms).

2. Filter characteristics scale with output sample rate. For output sample rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.625x Fs.

3. The analog modulator samples the input at 6.144 MHz for an Fs equal to 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.8 kHz where n = 0,1,2,3...).

4. Group delay for Fs = 48 kHz, t_{gd} = 15/48 kHz = 312 µs.

ANALOG CHARACTERISTICS (CONTINUED)

Parameter	Symbol	CS4223/4 - KS			CS4223/4 - BS			Unit
		Min	Typ	Max	Min	Typ	Max	
Analog Output Characteristics - Minimum Attenuation, 10 kΩ, 100 pF load; unless otherwise specified.								
DAC Resolution		-	-	24	-	-	24	Bits
Signal-to-Noise, Idle-Channel Noise (CS4224 only) DAC muted, A-weighted		102	110	-	97	110	-	dB
Dynamic Range DAC not muted, A-weighted		100	105	-	95	105	-	dB
DAC not muted, unweighted		97	102	-	92	102	-	dB
Total Harmonic Distortion	THD	-	0.0014	-	-	0.0014	-	%
Total Harmonic Distortion + Noise	THD+N	-	-97	-92	-	-97	-87	dB
Interchannel Isolation (1 kHz)		-	90	-	-	90	-	dB
Interchannel Gain Mismatch		-	-	0.1	-	-	0.1	dB
Attenuation Step Size All Outputs		0.35	0.5	0.65	0.35	0.5	0.65	dB
Programmable Output Attenuation Span		110	113.5	-	110	113.5	-	dB
Differential Offset Voltage		-	±10	-	-	±10	-	mV
Common Mode Output Voltage		-	2.4	-	-	2.4	-	V
Full Scale Output Voltage		1.8	1.9	2.0	1.8	1.9	2.0	Vrms
Gain Drift		-	100	-	-	100	-	ppm/°C
Out-of-Band Energy Fs/2 to 2 Fs		-	-60	-	-	-60	-	dBFs
Analog Output Load Resistance		10	-	-	10	-	-	kΩ
Capacitance		-	-	100	-	-	100	pF
Combined Digital and Analog Filter Characteristics								
Frequency Response 10 Hz to 20 kHz		-	±0.1	-	-	±0.1	-	dB
Deviation from Linear Phase		-	±0.5	-	-	±0.5	-	Degree
Passband: to 0.01 dB corner (Notes 5 and 6)		0	-	21.8	0	-	21.8	kHz
Passband Ripple (Note 6)		-	-	±0.01	-	-	±0.01	dB
Stopband (Notes 5 and 6)		26.2	-	-	26.2	-	-	kHz
Stopband Attenuation (Note 7)		70	-	-	70	-	-	dB
Group Delay (Fs = Input Word Rate)	t_gd	-	16/Fs	-	-	16/Fs	-	s
Power Supply								
Power Supply Current VA		-	46	60	-	46	60	mA
VD		-	9	20	-	9	20	mA
VL		-	3	5	-	3	5	mA
Total Power Down		-	0.4	-	-	0.4	-	mA
Power Supply Rejection Ratio 1 kHz		-	65	-	-	65	-	dB

Notes: 5. The passband and stopband edges scale with frequency. For input word rates, Fs, other than 48 kHz, the 0.01 dB passband edge is 0.4535x Fs and the stopband edge is 0.5465x Fs.

6. Digital filter characteristics.

7. Measurement bandwidth is 10 Hz to 3 Fs.

DIGITAL CHARACTERISTICS (T_A = 25° C; VA, VD = 4.75V - 5.25V)

Parameter		Symbol	Min	Max	Unit
High-level Input Voltage	VL = 5V	V_{IH}	2.8	VL + 0.3	V
	VL = 3V	V_{IH}	2.0	VL + 0.3	V
Low-level Input Voltage		V_{IL}	-0.3	0.8	V
High-level Output Voltage at I_O = -2.0 mA		V_{OH}	VL - 1.0	-	V
Low-level Output Voltage at I_O = 2.0 mA		V_{OL}	-	0.5	V
Input Leakage Current	Digital Inputs		-	10	µA
Output Leakage Current	High Impedance Digital Outputs		-	10	µA

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Max	Unit
Power Supplies	Digital	VD	-0.3	6.0	V
	Analog	VA	-0.3	6.0	V
Input Current	(Note 8)		-	±10	mA
Analog Input Voltage	(Note 9)		-0.7	VA + 0.7	V
Digital Input Voltage	(Note 9)		-0.7	VD + 0.7	V
Ambient Temperature	Power Applied		-55	+125	°C
Storage Temperature			-65	+150	°C

RECOMMENDED OPERATING CONDITIONS

(AGND, DGND = 0 V, all voltages with respect to 0 V.)

Parameter		Symbol	Min	Typ	Max	Unit
Power Supplies	Digital	VD	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
	Digital	VL	2.7	5.0	5.25	V
	| VA - VD |		-	-	0.4	V
Ambient Operating Temperature	Commercial (KS)	T_{AC}	-10	25	70	°C
	Industrial (BS)	T_{AI}	-40	25	85	°C

Notes: 8. Any pin except supplies. Transient currents of up to 100 mA on the analog input pins will not cause SCR latch-up.

   9. The maximum over or under voltage is limited by the input current.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
   Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS (T_A = 25° C; VA, VD = 4.75 V - 5.25 V; outputs loaded with 30 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Audio ADC's and DAC's Sample Rate		Fs	4	-	50	kHz
XTI Frequency	XTI = 256, 384, or 512 Fs		1.024	-	26	MHz
XTI Pulse Width High	XTI = 512 Fs		13	-	-	ns
	XTI = 384 Fs		21	-	-	ns
	XTI = 256 Fs		31	-	-	ns
XTI Pulse Width Low	XTI = 512 Fs		13	-	-	ns
	XTI = 384 Fs		21	-	-	ns
	XTI = 256 Fs		31	-	-	ns
XTI Jitter Tolerance			-	500	-	psRMS
RST Low Time	(Note 10)		10	-	-	ms
SCLK falling edge to SDOUT output valid	DSCK = 0	t_{dpd}	-	-	$\frac{1}{(384)\,Fs} + 20$	ns
LRCK edge to MSB valid		t_{lrpd}	-	-	45	ns
SDIN setup time before SCLK rising edge	DSCK = 0	t_{ds}	25	-	-	ns
SDIN hold time after SCLK rising edge	DSCK = 0	t_{dh}	25	-	-	ns
SCLK Period		t_{sckw}	$\frac{1}{(128)\,Fs}$	-	-	ns
SCLK High Time		t_{sckh}	40	-	-	ns
SCLK Low Time		t_{sckl}	40	-	-	ns
SCLK rising to LRCK edge	DSCK = 0	t_{lrckd}	35	-	-	ns
LRCK edge to SCLK rising	DSCK = 0	t_{lrcks}	40	-	-	ns

Notes: 10. After powering up the CS4223/4, PDN should be held low for 10 ms to allow the power supply to settle.
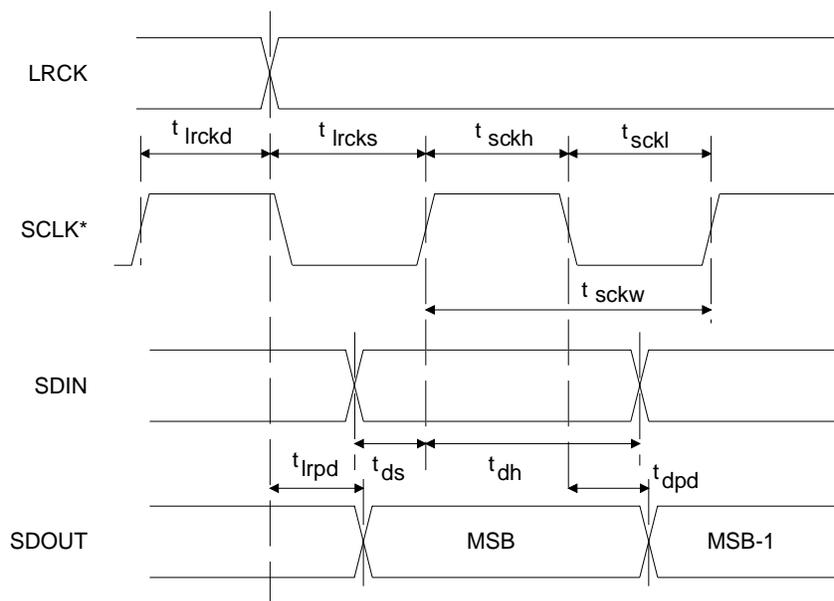
*SCLK shown for DSCK = 0, SCLK inverted for DSCK = 1.

Figure 1. Serial Audio Port Data I/O Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE (CS4224)

$(T_A = 25°\ C;\ VA,\ VD = 4.75\ V - 5.25\ V;\ Inputs:\ Logic\ 0 = DGND,\ Logic\ 1 = VD;\ C_L = 30\ pF)$

Parameter		Symbol	Min	Max	Unit
SPI Mode (SPI/I2C = 0)					
CCLK Clock Frequency		f_{sck}	-	6	MHz
RST rising edge to CS falling	(Note 11)	t_{srs}	41	-	µs
CCLK edge to CS falling	(Note 12)	t_{spi}	500	-	ns
CS High Time between transmissions		t_{csh}	1.0	-	µs
CS falling to CCLK edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK rising setup time		t_{dsu}	40	-	ns
CCLK rising to DATA hold time	(Note 13)	t_{dh}	15	-	ns
Rise time of CCLK and CDIN	(Note 14)	t_{r2}	-	100	ns
Fall time of CCLK and CDIN	(Note 14)	t_{f2}	-	100	ns

Notes: 11. Not tested but guaranteed by design.

    12. t_{spi} only needed before first falling edge of CS after RST rising edge. $t_{spi} = 0$ at all other times.

    13. Data must be held for sufficient time to bridge the transition time of CCLK.

    14. For $F_{SCK} < 1$ MHz.
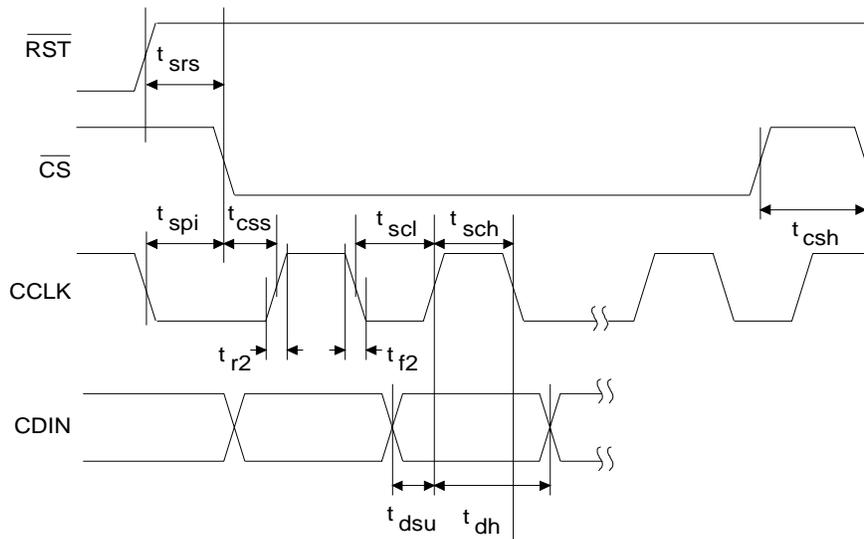
Figure 2. SPI Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - I²C MODE (CS4224)

(T_A = 25° C; VA, VD = 4.75 V - 5.25 V; Inputs: Logic 0 = DGND, Logic 1 = VD; C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
I²C® Mode (SPI/I2C = 1)				
SCL Clock Frequency	f_{scl}	-	100	kHz
RST rising edge to Start (Note 15)	t_{irs}	50	-	µs
Bus Free Time between transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low Time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup time for repeated Start Condition	t_{sust}	4.7	-	µs
SDA hold time for SCL falling (Note 16)	t_{hdd}	0	-	µs
SDA setup time to SCL rising	t_{sud}	250	-	ns
Rise time of SCL	t_{rc}	-	25	ns
Fall time of SCL	t_{fc}	-	25	ns
Rise time of SDA	t_{rd}	-	1	µs
Fall time of SDA	t_{fd}	-	300	ns
Setup time for Stop Condition	t_{susp}	4.7	-	µs

Notes: 15. Not tested but guaranteed by design.

16. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
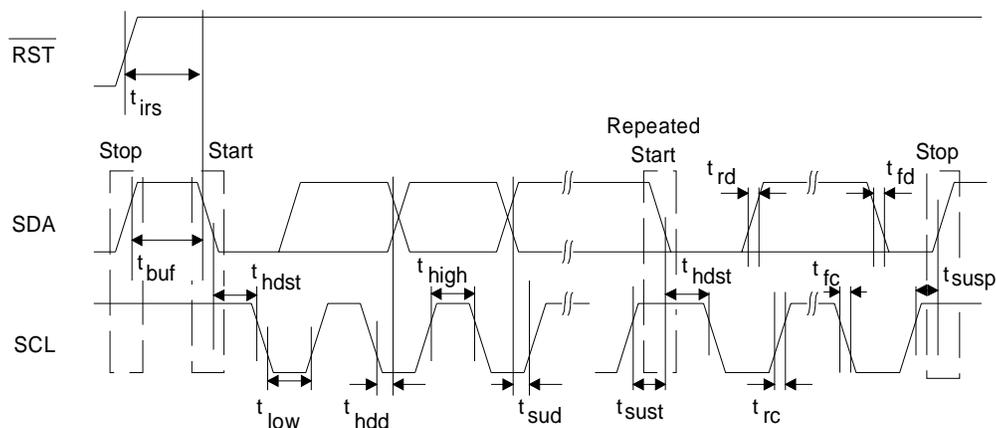
Figure 3. I²C Control Port Timing

2. TYPICAL CONNECTION DIAGRAM — CS4223
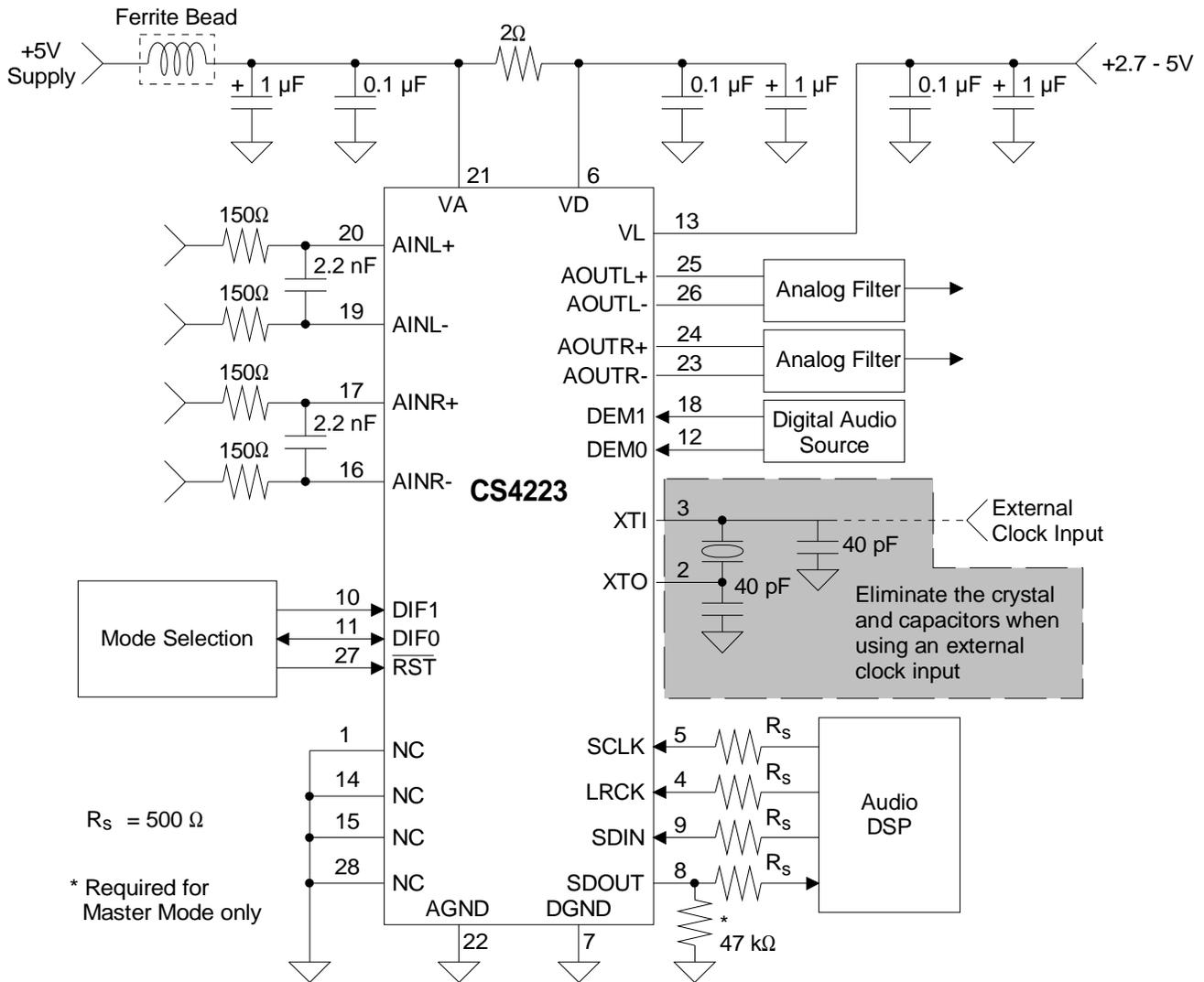
Figure 4. CS4223 Recommended Connection Diagram
(Also see *Recommended Layout Diagram*)

3. TYPICAL CONNECTION DIAGRAM — CS4224
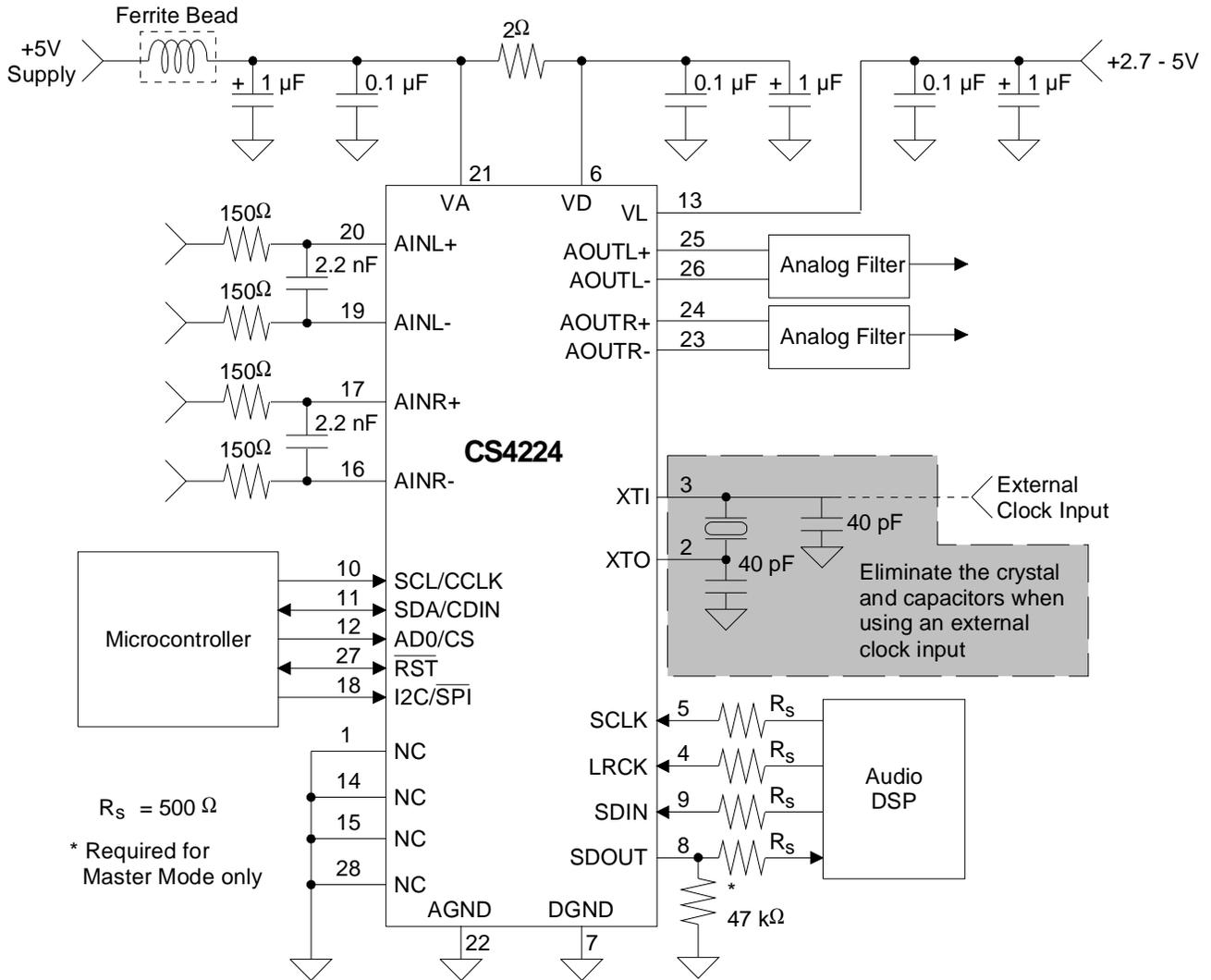
Figure 5. CS4224 Recommended Connection Diagram
(Also see *Recommended Layout Diagram*)

4. REGISTER QUICK REFERENCE - CS4224

Addr	Function	7	6	5	4	3	2	1	0
0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
1h	ADC Control	PDN	HPDR	HPDL	ADMR	ADML	CAL	CALP	CLKE
	default	0	0	0	0	0	0	0	0
2h	DAC Control	Reserved	MUTC	MUTR	MUTL	SOFT	Reserved	RMP1	RMP0
	default	0	0	0	0	0	0	0	0
3h-4h	Output Attenuator Level	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
	default	0	0	0	0	0	0	0	0
5h	DSP Port Mode	Reserved	DEM1	DEM0	DSCK	DOF1	DOF0	DIF1	DIF0
	default	0	0	0	0	0	0	0	0
6h	Converter Status Report	ACCR	ACCL	LVR2	LVR1	LVR0	LVL2	LVL1	LVL0
	default	0	0	0	0	0	0	0	0
7h	Master Clock Control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCK1	MCK0
	default	0	0	0	0	0	0	0	0

5. REGISTER DESCRIPTIONS - CS4224

Note: All registers are read/write in I²C mode and write-only in SPI mode, unless otherwise noted.

5.1 ADC Control (address 01h)

7	6	5	4	3	2	1	0
PDN	HPDR	HPDL	ADMR	ADML	CAL	CALP	CLKE
0	0	0	0	0	0	0	0

5.1.1 POWER DOWN ADC (PDN)

> Default = 0
> 0 - Disabled
> 1 - Enabled

Function:

> The ADC will enter a low-power state when this function is enabled.

5.1.2 LEFT AND RIGHT CHANNEL HIGH PASS FILTER DEFEAT (HPDR-HPDL)

> Default = 0
> 0 - Disabled
> 1 - Enabled

Function:

> The internal high-pass filter is defeated when this function is enabled. Control of the internal high-pass filter is independent for the left and right channel.

5.1.3 LEFT AND RIGHT CHANNEL ADC MUTING (ADMR-ADML)

> Default = 0
> 0 - Disabled
> 1 - Enabled

Function:

> The output for the selected ADC channel will be muted when this function is enabled.

5.1.4 CALIBRATION CONTROL (CAL)

> Default = 0
> 0 - Disabled
> 1 - Enabled

Function:

> The device will automatically perform an offset calibration when brought out of reset, which last approximately 50 ms. When this function is enabled, a rising edge on the reset line will initiate an offset calibration.

5.1.5 CALIBRATION STATUS (CALP) (READ ONLY)

> Default = 0
> 0 - Calibration done
> 1 - Calibration in progress

5.1.6 CLOCKING ERROR (CLKE) (READ ONLY)

Default = 0
0 - No error
1 - Error

5.2 DAC Control (address 02h)

7	6	5	4	3	2	1	0
Reserved	MUTC	MUTR	MUTL	SOFT	Reserved	RMP1	RMP0
0	0	0	0	0	0	0	0

5.2.1 MUTE ON CONSECUTIVE ZEROS (MUTC)

Default = 0
0 - Disabled
1 - Enabled

Function:

The DAC output will mute following the reception of 512 consecutive audio samples of static 0 or -1 when this function is enabled. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The muting function is affected, similar to volume control changes, by the SOFT bit in the DAC Control register.

5.2.2 MUTE CONTROL (MUTR-MUTL)

Default = 0
0 - Disabled
1 - Enabled

Function:

The output for the selected DAC channel will be muted when this function is enabled. The muting function is affected, similar to volume control changes, by the SOFT bit in the DAC Control register.

5.2.3 SOFT RAMP CONTROL (SOFT)

Default = 0
0 - Soft Ramp level changes
1 - Zero Cross level changes

Function:

Soft Ramp level changes will be implemented by incrementally ramping, in 0.5 dB steps, from the current level to the new level. The rate of change defaults to 0.5 dB per 8 left/right clock periods and is adjustable through the RMP bits in the DAC Control register.

Zero Cross level changes will be implemented in a single step from the current level to the new level. The level change takes effect on a zero crossing to minimize audible artifacts. If the signal does not encounter a zero crossing, the level change will occur after a timeout period of 512 sample periods (10.7 ms at 48 kHz sample rate). Zero crossing is independently monitored and implemented for each channel. The ACCR and ACCL bits in the Converter Status Report register indicate when a level change has occurred for the right and left channel.

5.2.4 SOFT RAMP STEP RATE (RMP)

Default = 00
00 - 1 step per 8 LRCK's
01 - 1 step per 4 LRCK's
10 - 1 step per 16 LRCK's
11 - 1 step per 32 LRCK's

Function:

The rate of change for the Soft Ramp function is adjustable through the RMP bits.

5.3 *Left Channel Output Attenuator Level (address 03h)*

5.4 *Right Channel Output Attenuator Level (address 04h)*

7	6	5	4	3	2	1	0
ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0	0	0	0	0	0	0	0

5.4.1 ATTENUATION LEVEL (ATT7-ATT0)

Default = 00h

Function:

The Output Attenuator Level registers allow for attenuation of the DAC outputs in 0.5 dB increments from 0 to 113.5 dB. Level changes are implemented with an analog volume control until the residual output noise is equal to the noise floor in the mute state. At this point, volume changes are performed digitally. This technique is superior to purely digital volume control because the noise is attenuated by the same amount as the signal, thus preserving dynamic range, see Figure 16. Volume changes are performed as dictated by the SOFT bit in the DAC Control register. ATT0 represents 0.5 dB of attenuation and settings greater than 227 (decimal value) will mute the selected DAC output.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
11100011	227	-113.5 dB
11100100	228	Muted

Table 1. Example Volume Settings

5.5   DSP Port Mode (address 05h)

7	6	5	4	3	2	1	0
Reserved	DEM1	DEM0	DSCK	DOF1	DOF0	DIF1	DIF0
0	0	0	0	0	0	0	0

5.5.1 DE-EMPHASIS CONTROL (DEM)

Default = 00
00 - 44.1 kHz de-emphasis setting
01 - 48 kHz de-emphasis setting
10 - 32 kHz de-emphasis setting
11 - De-emphasis disabled

Function:

Selects the appropriate digital filter to maintain the standard 15 μs/50 μs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates, see Figure 15.

5.5.2 SERIAL INPUT/OUTPUT DATA SCLK POLARITY SELECT (DSCK)

Default = 0
0 - Data valid on rising edge of SCLK
1 - Data valid on falling edge of SCLK

Function:

This function selects the polarity of the SCLK edge used to clock data in and out of the serial audio port.

5.5.3 SERIAL DATA OUTPUT FORMAT (DOF)

Default = 00
00 - I^{2}S compatible
01 - Left justified
10 - Right justified, 24-bit
11 - Right justified, 20-bit

Function:

The required relationship between the left/right clock, serial clock and output serial data is defined by the Serial Data Output Format, and the options are detailed in Figures 8-11.

Note: If the format selected is Right-Justified, SCLK must be 64 Fs when operating in slave mode.

5.5.4 SERIAL DATA INPUT FORMAT (DIF)

Default = 00
00 - I^{2}S compatible
01 - Left justified
10 - Right justified, 24-bit
11- Right justified, 20-bit

Function:

The required relationship between the left/right clock, serial clock and input serial data is defined by the Serial Data Input Format, and the options are detailed in Figures 8-11.

5.6   Converter Status Report (Read Only) (address 06h)

7	6	5	4	3	2	1	0
ACCR	ACCL	LVR2	LVR1	LVR0	LVL2	LVL2	LVL0
0	0	0	0	0	0	0	0

5.6.1   LEFT AND RIGHT CHANNEL ACCEPTANCE BIT (ACCR-ACCL)

Default = 0
0 - Requested setting valid
1 - New setting loaded

Function:

The ACCR and ACCL bits indicate when a change in the Output Attenuator Level has occurred for the left and right channels, respectively. The value will be high when a new setting is loaded into the Output Attenuator Level registers. The value will return low when the requested attenuation setting has taken effect.

5.6.2   LEFT AND RIGHT CHANNEL ADC OUTPUT LEVEL (LVR AND LVL)

Default = 000
000 - Normal output levels
001 - -6 dB level
010 - -5 dB level
011 - -4 dB level
100 - -3 dB level
101 - -2 dB level
110 - -1 dB level
111 - Clipping

Function:

The analog-to-digital converter is continually monitoring the peak digital signal output for both the left and right channel, prior to the digital limiter. The maximum output value is stored in the LVL and LVR bits. The LVL and LVR bits are 'sticky', so they are reset after each read is performed.

5.7   Master Clock Control (address 07h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MCK1	MCK0
0	0	0	0	0	0	0	0

5.7.1   MASTER CLOCK CONTROL (MCK)

Default = 00
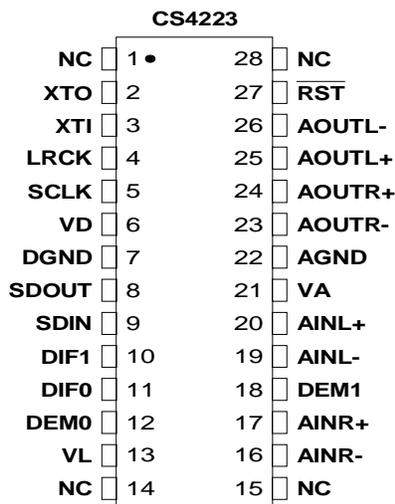00 - XTI = 256 Fs for Master Mode
01 - XTI = 384 Fs for Master Mode
10 - XTI = 512 Fs for Master Mode

Function:

The MCK bits allow for control of the Master Clock, XTI, input frequency.

Note: These bits are not valid when operating in slave mode.

6. PIN DESCRIPTIONS — CS4223

CS4223

NC	1 •	28	NC
XTO	2	27	$\overline{RST}$
XTI	3	26	AOUTL-
LRCK	4	25	AOUTL+
SCLK	5	24	AOUTR+
VD	6	23	AOUTR-
DGND	7	22	AGND
SDOUT	8	21	VA
SDIN	9	20	AINL+
DIF1	10	19	AINL-
DIF0	11	18	DEM1
DEM0	12	17	AINR+
VL	13	16	AINR-
NC	14	15	NC

NC	1,14,15, 28	**No Connect -** These pins are not connected internally and should be tied to DGND to minimize noise coupling.
XTI, XTO	2,3	**Crystal Connections (*Input/Output*) -** Input and output connections for the crystal used to clock the CS4223. Alternatively, a clock may be input into XTI. This is the clock source for the delta-sigma modulator and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs in Slave Mode and 256x in Master Mode.

Fs (kHz)	XTI (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 2. Common Clock Frequencies

LRCK	4	**Left/Right Clock (*Input*) -** Determines which channel is currently being input/output of the serial audio data pins SDIN/SDOUT. The frequency of the Left/Right clock must be equal to the input sample rate. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.
SCLK	5	**Serial Data Clock (*Input*) -** Clocks the individual bits of the serial data into the SDIN pin and out of the SDOUT pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.
VD	6	**Digital Power (*Input*) -** Positive power supply for the digital section. Typically 5.0 VDC.
DGND	7	**Digital Ground (*Input*) -** Digital ground for the digital section.
SDOUT	8	**Serial Data Output (*Output*) -** Two's complement MSB-first serial data is output on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.

SDIN   9   **Serial Data Input (*Input*) -** Two's complement MSB-first serial data is input on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DIF1-0 pins. The options are detailed in Figures 8 - 11.

DIF0, DIF1   10,11   **Digital Interface Format (*Input*) -** The required relationship between the left/right clock, serial clock and serial data is defined by the Digital Interface Format. The options are detailed in Figures 8 - 11.

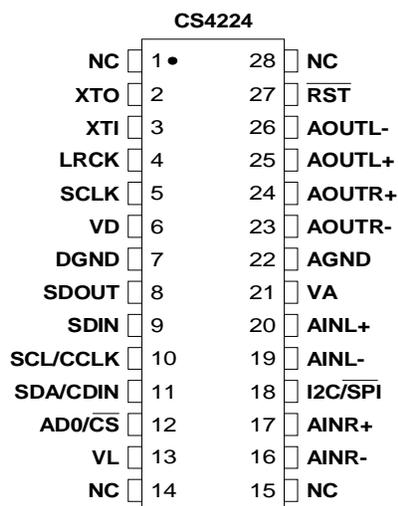| DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit data	0	8
0	1	Left Justified, up to 24-bit data	1	9
1	0	Right Justified, 24-bit Data	2	10
1	1	Right Justified, 20-bit Data	3	11

Table 3. Digital Interface Format - DIF1 and DIF0

DEM0, DEM1   12,18   **De-Emphasis Select (*Input*) -** Controls the activation of the standard 50/15 μs de-emphasis filter. 32, 44.1, or 48 kHz sample rate selection defined in Table 4.

DEM0	DEM1	De-Emphasis
0	0	32 kHz
0	1	44.1 kHz
1	0	48 kHz
1	1	Disabled

Table 4. De-emphasis Control

VL   13   **Digital Logic Power (*Input*) -** Positive power supply for the digital interface section. Typically 3.0 to 5.0 VDC.

AINR-, AINR+   16,17   **Differential Right Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.

AINL-, AINL+   19,20   **Differential Left Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.

VA   21   **Analog Power (*Input*) -** Positive power supply for the analog section. Nominally +5 Volts.

AGND   22   **Analog Ground (*Input*) -** Analog ground reference.

AOUTR-, AOUTR+   23, 24   **Differential Right Channel Analog Output (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.

AOUTL-, AOUTL+   25, 26   **Differential Left Channel Analog Output (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.

RST   27   **Reset (*Input*) -** When low, the device enters a low power mode and all internal registers are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

7. PIN DESCRIPTIONS — CS4224

```
                    CS4224

     NC  [  1 •        28  ]  NC
    XTO  [  2          27  ]  RST
    XTI  [  3          26  ]  AOUTL-
   LRCK  [  4          25  ]  AOUTL+
   SCLK  [  5          24  ]  AOUTR+
     VD  [  6          23  ]  AOUTR-
   DGND  [  7          22  ]  AGND
  SDOUT  [  8          21  ]  VA
   SDIN  [  9          20  ]  AINL+
SCL/CCLK [ 10          19  ]  AINL-
SDA/CDIN [ 11          18  ]  I2C/SPI
 AD0/CS  [ 12          17  ]  AINR+
     VL  [ 13          16  ]  AINR-
     NC  [ 14          15  ]  NC
```

NC	1,14,15, 28	**No Connect** - These pins are not connected internally and should be tied to DGND to minimize noise coupling.
XTI, XTO	2,3	**Crystal Connections (*Input/Output*)** - Input and output connections for the crystal used to clock the CS4224. Alternatively a clock may be input into XTI. This is the clock source for the delta-sigma modulator and digital filters. The frequency of this clock must be either 256x, 384x, or 512x Fs. The default XTI setting in Master Mode is 256x, but this may be changed to 384x or 512x through the Control Port.

Fs (kHz)	XTI (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 5. Common Clock Frequencies

LRCK	4	**Left/Right Clock (*Input*)** - Determines which channel is currently being input/output of the serial audio data pins SDIN/SDOUT. The frequency of the Left/Right clock must be equal to the input sample rate. Although the outputs for each ADC channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SCLK	5	**Serial Data Clock (*Input*)** - Clocks the individual bits of the serial data into the SDIN pin and out of the SDOUT pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
VD	6	**Digital Power (*Input*)** - Positive power supply for the digital section. Typically 5.0 VDC.
DGND	7	**Digital Ground (*Input*)** - Digital ground for the digital section.

SDOUT	8	**Serial Data Output (*Output*) -** Two's complement MSB-first serial data is output on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SDIN	9	**Serial Data Input (*Input*) -** Two's complement MSB-first serial data is input on this pin. The required relationship between the left/right clock, serial clock and serial data is defined by the DSP Port Mode (05h) register. The options are detailed in Figures 8 - 11.
SCL/CCLK	10	**Serial Control Port Clock (*Input*) -** Clocks the serial control bits into and out of the CS4224. In I^{2}C mode, SCL requires an external pull-up resistor according to the I^{2}C specification.
SDA/CDIN	11	**Serial Control Port Data (*Input/Output*)-** SDA is a data I/O line in I^{2}C mode and requires an external pull-up resistor according to the I^{2}C specification. CDIN in the input data line for the serial control port in SPI mode.
AD0/$\overline{\text{CS}}$	12	**Address Bit/Control Chip Select (*Input*) -** In I^{2}C mode, AD0 is a chip address bit. In SPI mode, $\overline{\text{CS}}$ is used to enable the control port interface on the CS4224. The CS4224 control port interface is defined by the $\overline{\text{SPI}}$/I2C pin.
VL	13	**Logic Power (*Input*) -** Positive power supply for the digital interface section. Typically 3.0 to 5.0 VDC.
AINR-, AINR+	16,17	**Differential Right Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
I2C/$\overline{\text{SPI}}$	18	**Control Port Format (*Input*)** - When this pin is high, I^{2}C mode is selected, when low, $\overline{\text{SPI}}$ is selected.
AINL-, AINL+	19,20	**Differential Left Channel Analog Input (*Input*) -** The full scale analog input level (differential) is specified in the Analog Characteristics specification table and may be AC coupled or DC coupled into the device, see Figure 12 for optional line input buffer.
VA	21	**Analog Power (*Input*) -** Positive power supply for the analog section. Typically 5.0 VDC.
AGND	22	**Analog Ground (*Input*) -** Analog ground reference.
AOUTR-, AOUTR+	23, 24	**Differential Right Channel Analog Outputs (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
AOUTL-, AOUTL+	25, 26	**Differential Left Channel Analog Outputs (*Output*) -** The full scale analog output level (differential) is specified in the Analog Characteristics specification table.
$\overline{\text{RST}}$	27	**Reset (*Input*)** - When low, the device enters a low power mode and all internal registers are reset, including the control port. When high, the control port becomes operational and normal operation will occur.

8. APPLICATIONS

8.1 Overview

The CS4223 is a stand-alone device controlled through dedicated pins. The CS4224 is controlled with an external microcontroller using the serial control port.

8.2 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4223/4 requires careful attention to power supply and grounding arrangements to optimize performance. Figures 4 and 5 shows the recommended power arrangement with VA, VD and VL connected to clean supplies. Decoupling capacitors should be located as close to the device package as possible. If desired, all supply pins may be connected to the same supply, but a decoupling capacitor should still be used on each supply pin.

8.3 High Pass Filter

The operational amplifiers in the input circuitry driving the CS4223/4 may generate a small DC offset into the A/D converter. The CS4223/4 includes a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system.

8.4 Analog Outputs

The recommended off-chip analog filter is either a 2nd order Butterworth or a 3rd order Butterworth, if greater out-of-band noise filtering is desired. The CS4223/4 DAC interpolation filter has been pre-compensated for an external 2nd order Butterworth filter with a 3 dB corner at Fs, or a 3rd order Butterworth filter with a 3 dB corner at 0.75 Fs to provide a flat frequency response and linear phase over the passband (see Figure 14 for Fs = 48 kHz). If the recommended filter is not used, small frequency response magnitude and phase errors will occur. In addition to providing out-of-band noise attenua-

tion, the output filters shown in Figure 14 provide differential to single-ended conversion.

8.5 Master vs. Slave Mode

The CS4223/4 may be operated in either master mode or slave mode. In master mode, SCLK and LRCK are outputs which are internally derived from MCLK. The device will operate in master mode when a 47 kΩ pulldown resistor is present on SDOUT at startup or after reset, see Figure 5. LRCK and SCLK are inputs to the CS4223/4 when operating in slave mode. See Figures 8-11 for the available clocking modes.

8.6 De-emphasis

The CS4223/4 includes digital de-emphasis for 32, 44.1, or 48 kHz sample rates. The frequency response of the de-emphasis curve, as shown in Figure 15, will scale proportionally with changes in samples rate, Fs. The de-emphasis feature is included to accommodate older audio recordings that utilize pre-emphasis as a means of noise reduction.

De-emphasis control is achieved with the DEM1/0 pins on the CS4223 or through the DEM1-0 bits in the DSP Port Mode Byte (#5) on the CS4224.

8.7 Power-up / Reset / Power Down Calibration

Upon power up, the user should hold $\overline{RST} = 0$ for approximately 10 ms. In this state, the control port is reset to its default settings and the part remains in the power down mode. At the end of $\overline{RST}$, the device performs an offset calibration which lasts approximately 50 ms after which the device enters normal operation. In the CS4224, a calibration may also be initiated via the CAL bit in the ADC Control Byte (#1). The CALP bit in the ADC Control Byte is a read only bit indicating the status of the calibration.

Reset/Power Down is achieved by lowering the $\overline{RST}$ pin causing the part to enter power down.

Once $\overline{\text{RST}}$ goes high, the control port is functional and the desired settings should be loaded.

The CS4223/4 will also enter power down mode if the master clock source stops for approximately 10 µs or if the LRCK is not synchronous to the master clock. The control port will retain its current settings.

The CS4223/4 will mute the analog outputs and enter the power down mode if the supply drops below approximately 4 volts.

8.8   Control Port Interface (CS4224 only)

The control port is used to load all the internal settings. The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI® and I^{2}C®, with the CS4224 operating as a slave device. The control port interface format is selected by the $\overline{\text{SPI}}$/I2C pin.

8.8.1   SPI Mode

In SPI mode, $\overline{\text{CS}}$ is the CS4224 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 6 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{\text{CS}}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{\text{W}}$), which must be low to write. Register reading from the CS4224 is not supported in the SPI mode. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into a register designated by the MAP.

The CS4224 has a MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is a zero, then the MAP will stay constant for successive writes. If INCR is set to a 1, then MAP will auto increment after each byte is written, allowing block writes of successive registers. Register reading from the CS4224 is not supported in the SPI mode.

8.8.2   I^{2}C Mode

In I^{2}C mode, SDA is a bidirectional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 7. There is no $\overline{\text{CS}}$ pin. Pin AD0 forms the partial chip address and should be tied to VD or DGND as desired. The upper 6 bits of the 7 bit address field must be 001000. In order to communicate with the CS4224, the LSB of the chip address field (first byte sent to the CS4224) should match the setting of the AD0 pin. The eighth bit of the address byte is the R/$\overline{\text{W}}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the Memory Address Pointer will be output. Setting the auto increment bit in MAP, allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

8.9   Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

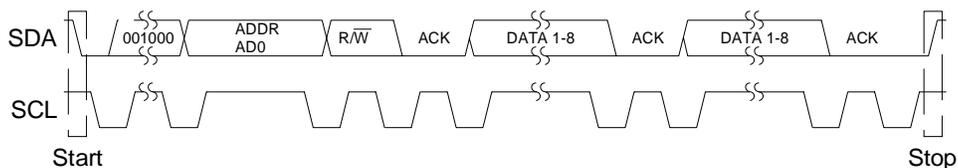### 8.9.1   AUTO-INCREMENT CONTROL (INCR)

Default = 0
0 - Disabled
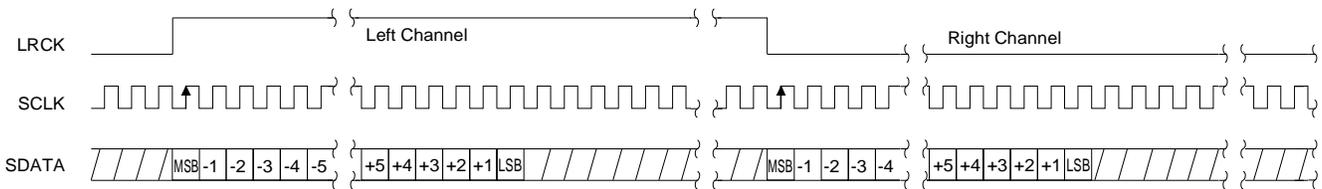1 - Enabled

8.9.2   REGISTER POINTER (MAP)

Default = 000
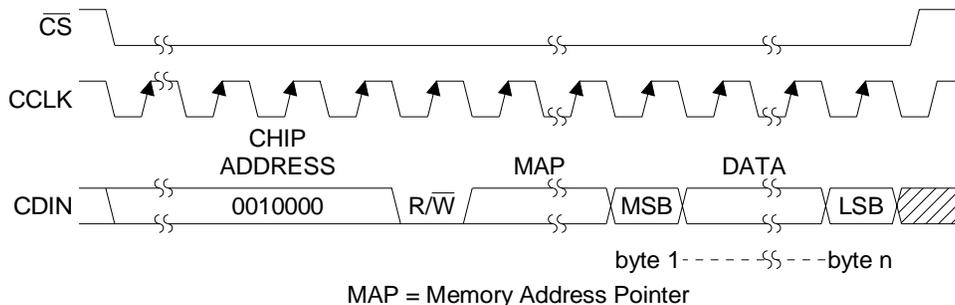
Figure 6. Control Port Timing, SPI mode

Figure 7. Control Port Timing, I^{2}C mode
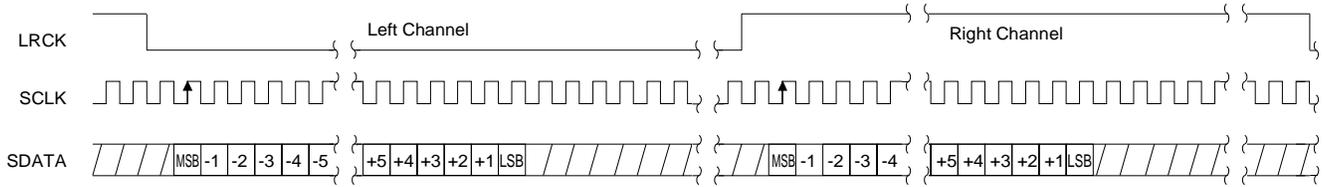
| Master	Slave
I²S, up to 24-bit data XTI = 256, 384, 512 Fs (CS4223-256 Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	I²S, up to 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 48, 64, 128 Fs

Figure 8. Serial Audio Format 0 (I²S)

Master	Slave
Left-justified, up to 24-bit data XTI = 256, 384, 512 Fs (CS4223-256 Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	Left-justified, up to 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 48, 64, 128 Fs

Figure 9. Serial Audio Format 1
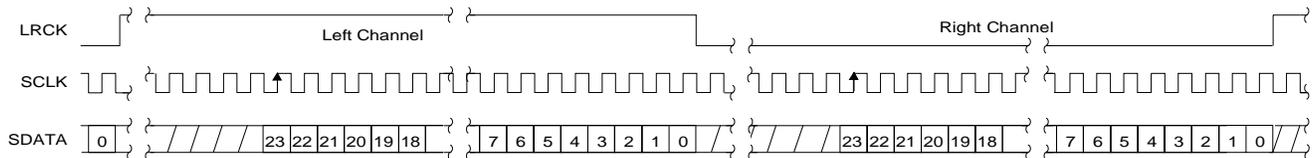
Master	Slave
Right-justified, 24-bit data XTI = 256, 384, 512 Fs (CS4223-256 Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	Right-justified, 24-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 64 Fs

Figure 10. Serial Audio Format 2
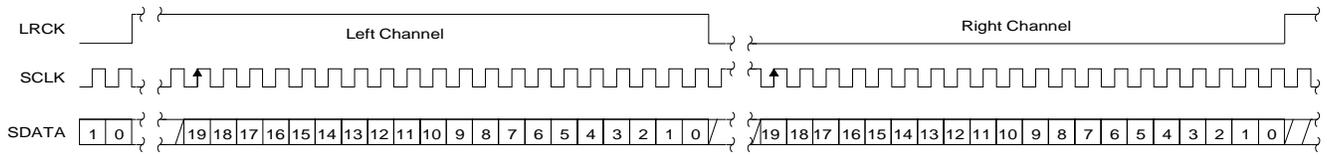
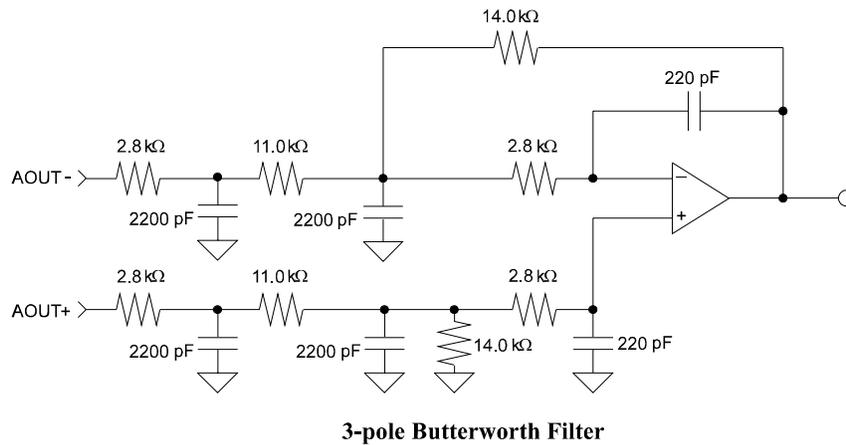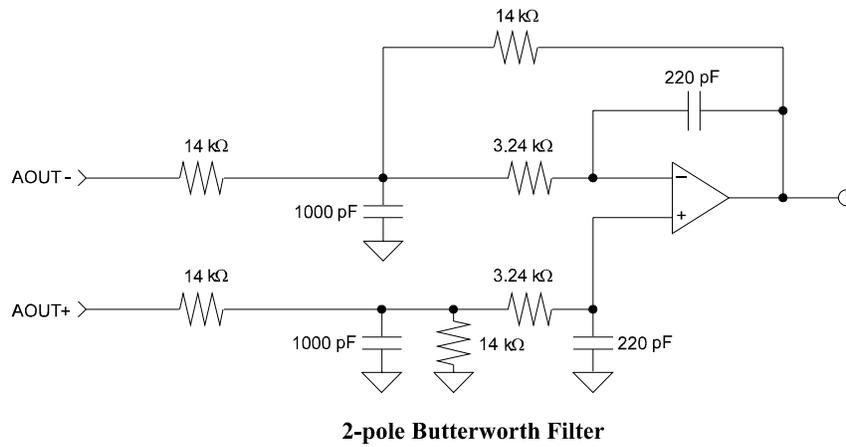| Master	Slave
Right-justified, 20-bit data XTI=256, 384, 512 Fs (CS4223-256Fs only) LRCK = 4 to 50 kHz SCLK = 64 Fs	Right-justified, 20-bit data XTI = 256, 384, 512 Fs LRCK = 4 to 50 kHz SCLK = 64 Fs

Figure 11. Serial Audio Format 3
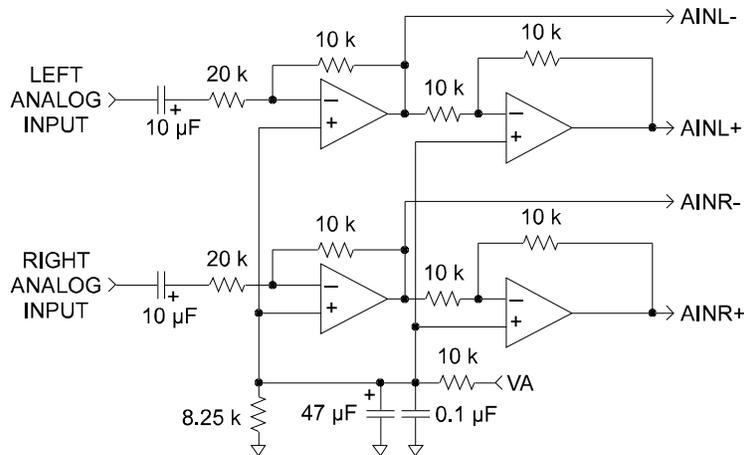
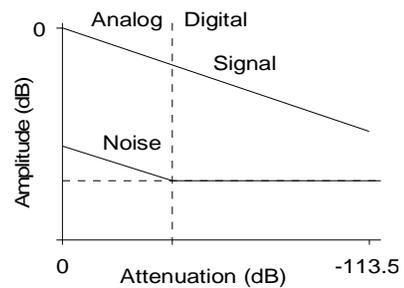**Figure 12. Optional Input Buffer**
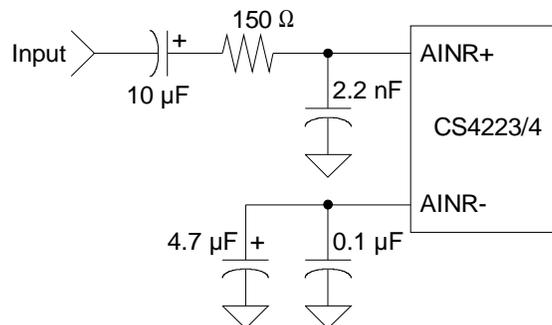
Figure 13. Single-ended Input Application

2-pole Butterworth Filter

3-pole Butterworth Filter
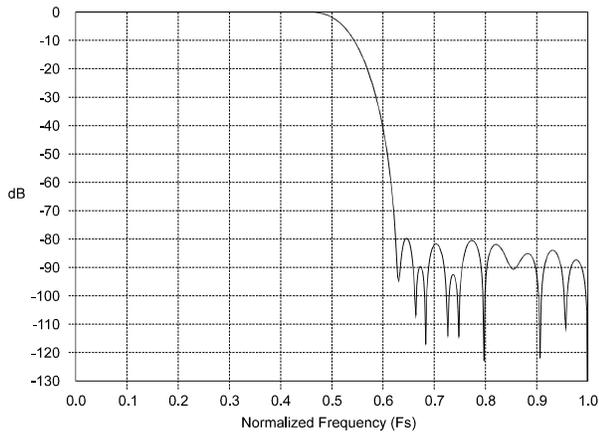
Figure 14. 2- and 3-Pole Butterworth Filters
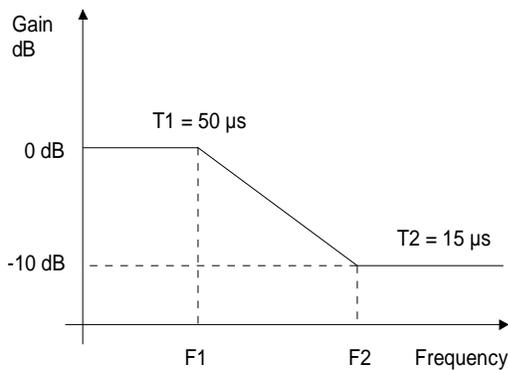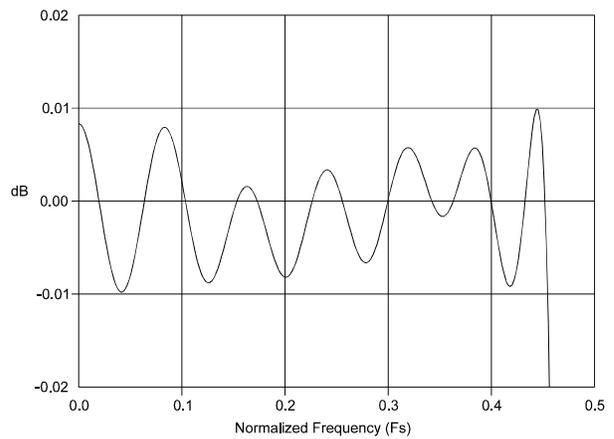

Figure 15. De-emphasis Curve

Figure 16. Hybrid Analog/Digital Attenuation

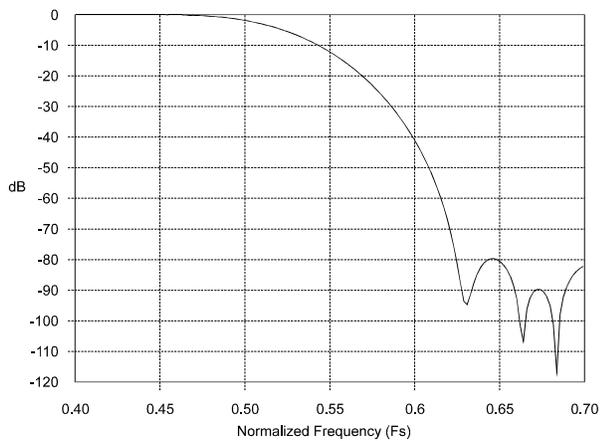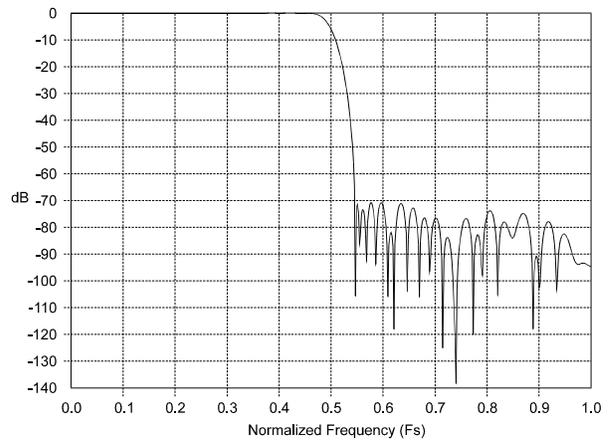## 9. ADC/DAC FILTER RESPONSE

Figure 17. ADC Filter Response

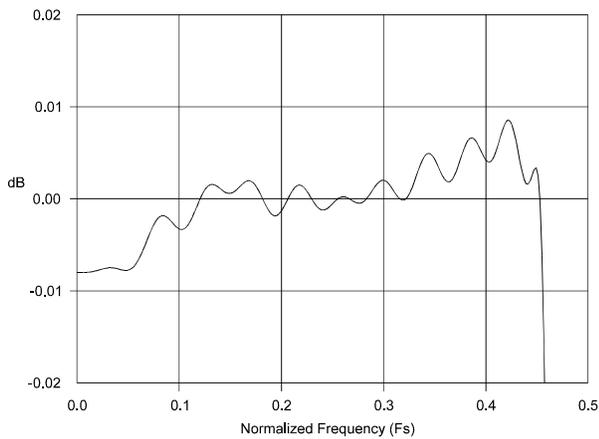Figure 18. ADC Passband Ripple
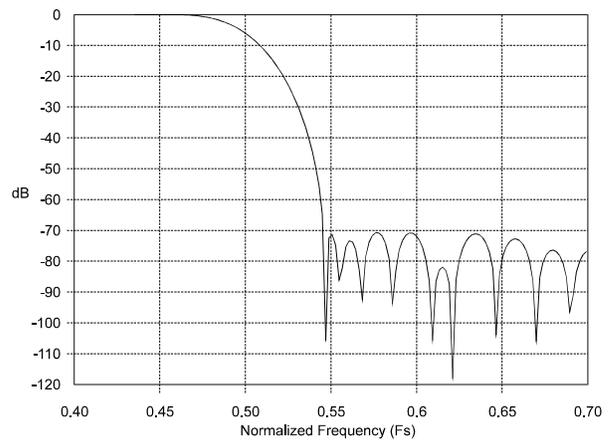
Figure 19. ADC Transition Band

Figure 20. DAC Filter Response

Figure 21. DAC Passband Ripple

Figure 22. DAC Transition Band

10. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 20 Hz to 20 kHz), including distortion components. Expressed in decibels. ADCs are measured at -1 dBFS as suggested in AES17-1991 Annex A and DACs are measured at 0 dBFS.

Idle Channel Noise / Signal-to-Noise-Ratio

The ratio of the rms analog output level with 1 kHz full scale digital input to the rms analog output level with all zeros into the digital input. Measured A-weighted over a 10 Hz to 20 kHz bandwidth. Units in decibels. This specification has been standardized by the Audio Engineering Society, AES17-1991, and referred to as Idle Channel Noise. This specification has also been standardized by the Electronic Industries Association of Japan, EIAJ CP-307, and referred to as Signal-to-Noise-Ratio.

Total Harmonic Distortion (THD)

THD is the ratio of the test signal amplitude to the rms sum of all the in-band harmonics of the test signal. Units in decibels.

Interchannel Isolation

A measure of crosstalk between channels. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Frequency Response

A measure of the amplitude response variation from 20 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units are in decibels.

Gain Error

The deviation from the nominal full scale output for a full scale input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Offset Error

For the ADCs, the deviation in LSB's of the output from mid-scale with the selected inputs tied to a common potential. For the DAC's, the differential output voltage with mid-scale input code. Units are in volts.

11. PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING

TOP VIEW

SIDE VIEW

END VIEW

SEATING PLANE
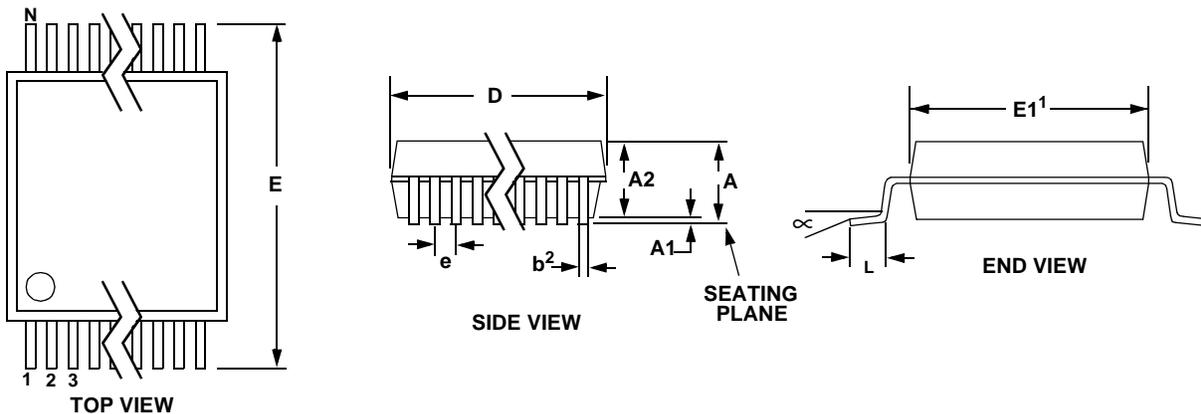
DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.15	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
$\propto$	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

CRYSTAL

• Notes •

SMART
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