

Evaluation Board for CS43122/CS4397

Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Supports PCM Audio and SACD Audio
- Requires only a digital signal source for a complete Digital-to-Analog Converter system
- Included Wall Mount power supply

Description

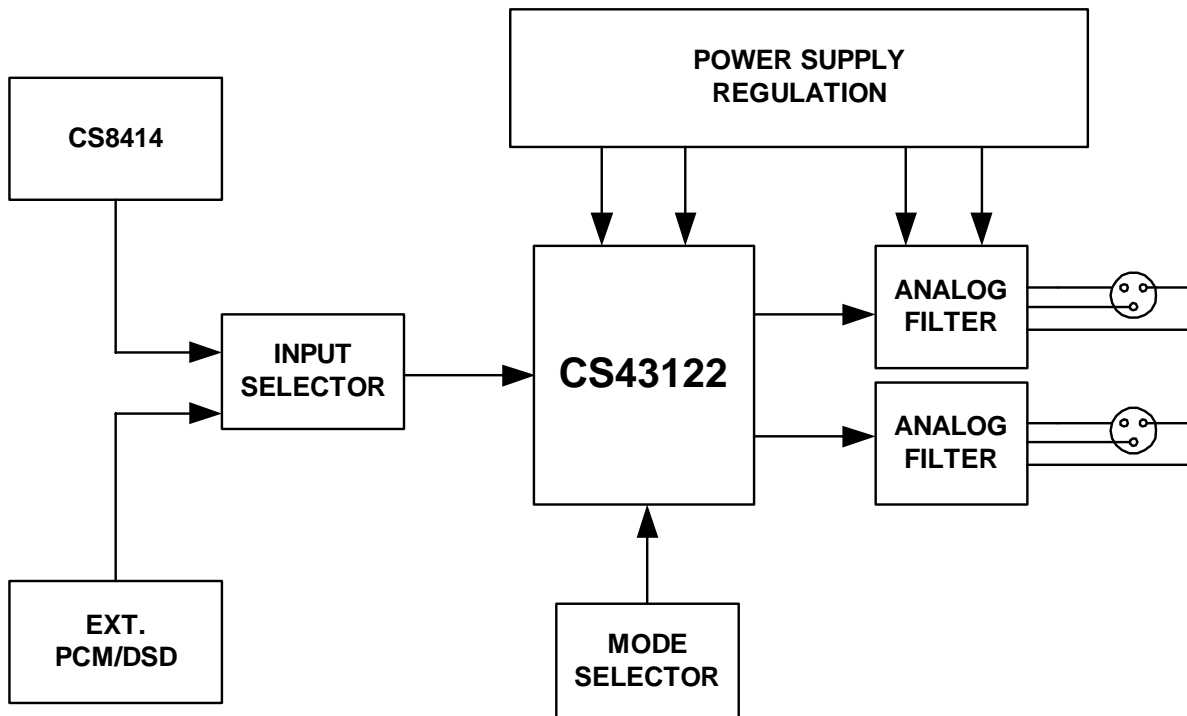
The CDB43122 evaluation board is an excellent means for quickly evaluating the CS43122 or CS4397 24bit-192 kHz D/A converters. The board accepts SPDIF and SACD inputs and, with an analog output interface, presents line level signals via XLR connectors. Evaluation requires an analog signal analyzer and a digital signal source.

The CS8414 digital audio receiver I.C. provides the system timing and data signals necessary to operate the Digital-to-Analog converter and will accept AES/EBU, SPDIF and EIAJ compatible audio data. The evaluation board may also be configured to accept external timing signals for operation in a user application during system development in PCM and DSD modes.

ORDERING INFORMATION

CDB43122

Evaluation Board



Preliminary Product Information

This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. CDB43122 SYSTEM OVERVIEW

The CDB43122 evaluation board is an excellent means of quickly evaluating the CS43122 or CS4397 24 bit - 192 kHz audio D/A converters. The evaluation board features a CS8414 digital audio input interface receiver, an analog output buffer/filter, and on board power supply regulation to be used with a supplied AC Wall Mount power supply. The CS8414 provides an easy interface to 32 kHz to 96 kHz digital audio signal sources. The evaluation board also allows the user to supply external PCM data and DSD data through a 10-pin header for system development.

2. CS43122 DIGITAL TO ANALOG CONVERTER

Please refer to the CS43122 or CS4397 product datasheets for a complete detailed description of these components.

3. CS8414 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8414 Digital Audio Receiver, Figure 1. The outputs of the CS8414 include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256 Fs master clock. The operation of the CS8414 and a discussion of the digital audio interface are included in the CS8414 datasheet.

4. EXTERNAL DIGITAL AUDIO DATA AND DSD INPUT PORT

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, JP1. This header allows the evaluation board to accept externally generated clocks and data.

The port is activated by setting the “MODE” Control Switch “S2” position 6 “INT/EXT” switch to the closed position.

This port accepts PCM data, DSD (CS4397) data or data from an external 8X interpolator such as an

HDCD PMD100 or PMD200. Notice that the board has provisions for terminating this input port for proper signal integrity using resistors R20 through R24.

The board also features automatic mode switching between this port and the SPDIF port when used with a SACD player. See Section 6- “Automatic Mode Switching” for a complete description of this feature.

5. MODE CONTROL

The board utilizes a Dip Switch, “S2” to allow the user to select various operational modes of the CS43122 or CS4397. These modes include selection of the Digital Interface Format, De-emphasis, Sample Rate modes, Internal-External Digital Audio Data, PCM-DSD Automatic Switching, 64x - 128x DSD Data, +3 V/+5 V Digital Supply voltage selection, and Mute control. See Tables 1 through 7 for a complete description of how the switch settings set the different operating modes of the CS43122.

6. AUTOMATIC MODE SWITCHING

The board features an automatic PCM or DSD input data switching mode for use with an external SACD player. When used with an external SACD player that has both a SPDIF output connected to J1 (U5) and DSD data output connected to the JP1 port, will allow the board to switch automatically between the two.

Theory of operation - When an SACD player switches from playing a CD to a DSD disc, the SPDIF output data is disabled, the internal circuitry (U6, U2, U3, U4, U7) detects loss of an SPDIF source and automatically switches the Digital Data Input path (U8) to the DSD input port JP1. This feature can also be controlled from an external control signal by removing R60 and inputting a control signal into JP2. Logic low = PCM mode, Logic high = DSD mode.

7. OUTPUT FILTER

The output buffer/filter uses a balanced configuration. The balanced output filter consist of the 301 ohm resistors and the 2200pf capacitor, and is designed to cancel out the opposing multibit step pattern in each analog output to create a very low out of band noise spectrum. The op-amps provide output buffering and are configured to provide a +4.5db boost when the board switches into DSD mode to compensate for the 4.5db gain loss of the CS4397 in DSD mode. The balanced outputs are AC coupled and are provided on board by XLR type connectors.

8. POWER SUPPLIES

The CDB43122 comes supplied with an external 14 VAC Wall Mount power supply for convenience in setup, and to make measurements easier by eliminating ground loop problems between lab power supplies and measurement equipment (Note: the provided wall mount supply only operates at 110/120V and 50/60 Hz). The external 14 VAC voltage supplied at J11 is rectified, filtered and regulated to produce +/-12 volts by regulators U13 and U14. Separate voltage regulation is used for the digital control circuitry (CS8414) and for the digital power section and analog section for the CS43122 - CS4397. The digital power for the CS43122 - CS4397 is user selectable by switch #9 on dip switch S2. The open position sets the voltage regulator VREG2 to +5.0 volts, the closed position sets the voltage regulator to +3.3 volts.

The CDB43122 evaluation board can also be powered by an external lab power supply by connecting +12 vdc to the +12V (J8) binding post, -12 vdc to -12V (J10), and ground to GND (J9). Up to +/- 13 volts is allowed before reverse voltage protection

diodes D3 and D4 will clamp the input voltage. With JP5 connected, the +5V, VD and VA supplies will be regulated from the supplied +12V. To provide VA and VD externally via the designated binding posts, remove JP5 and lift pin 3 (bottom right pin) on VREG1; +5V to the CS8414 will still be provided by the on board regulator.

WARNING: refer to the CS43122 datasheet for maximum allowable voltage levels. Operation outside this range can cause permanent damage to the device.

9. GROUNDING AND POWER SUPPLY DECOUPLING

For the user to be able to realize the high performance capabilities of the CS43122 or CS4397, it is recommended to pay careful attention to PC board layout, grounding, and placement of the power supply and decoupling capacitors. It is recommended when doing the PC board layout to use one ground plane underneath the part for both the analog and digital sections. Please review the attached PC board photo plots for an example of the suggested grounding method.

It is also recommended to pay careful attention to the placement of the decoupling capacitors tied to VREF (pin 28). This pin requires a very low impedance path to ground at high frequencies as this pin draws high frequency current pulses at 6 MHz. It is important to place the .01 uf capacitor and 100 uf capacitor right next to the pin. Keep the connecting trace as short as possible. High performance capacitors such as NPO for the .01 uf and a low ESR electrolytic or tantalum for the 100 uf are recommended. Low frequency distortion (0-40Hz) performance can also be improved by increasing the FILT+ (pin 27) capacitance value up to 470uf.

10. CS43122/CS4397 MODE SETTINGS (SW2)

Switch #	Label	Position	Description
1	MO	OPEN = 1	See CS43122 datasheet for details
2	M1	OPEN = 1	See CS43122 datasheet for details
3	M2	OPEN = 1	See CS43122 datasheet for details
4	M3	OPEN = 1	See CS43122 datasheet for details
5	M4	OPEN = 1	See CS43122 datasheet for details
6	INT/EX1	OPEN = INT	SETS THE INPUT MUX TO THE CS8414 (INT) OR TO JP1 (EX1)
7	PCM/DSD	OPEN = DISABLED	Activates Auto Switching for PCM and DSD
8	64/128X	OPEN = 128X	SETS THE CLOCK MODE FOR DSD
9	+3V/5V	OPEN = +5V	SETS THE DIGITAL POWER SUPPLY TO +3.3 OR +5 VOLTS
10	/MUTE CTL	OPEN = DISABLED	ENABLES THE EXTERNAL MUTE CONTROL CIRCUITRY
DEFAULT	SWITCH 9 SET CLOSED, ALL OTHERS SET TO OPEN		

SWITCH S2 MODE SETTINGS TABLE

1. Note: Switch #'s 1 to 4 must be open for audio mode to function properly.

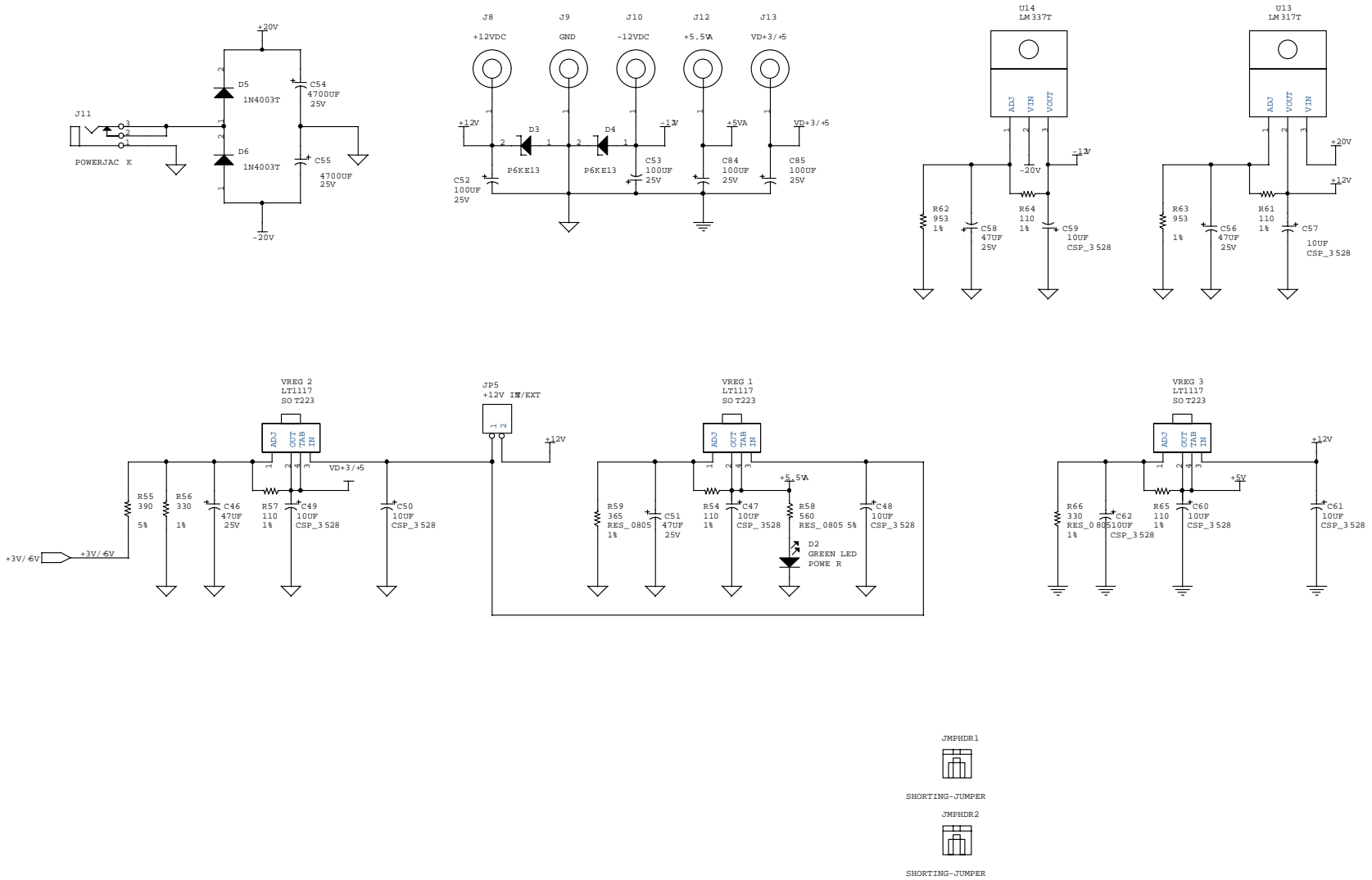


Figure 1. Power Supply

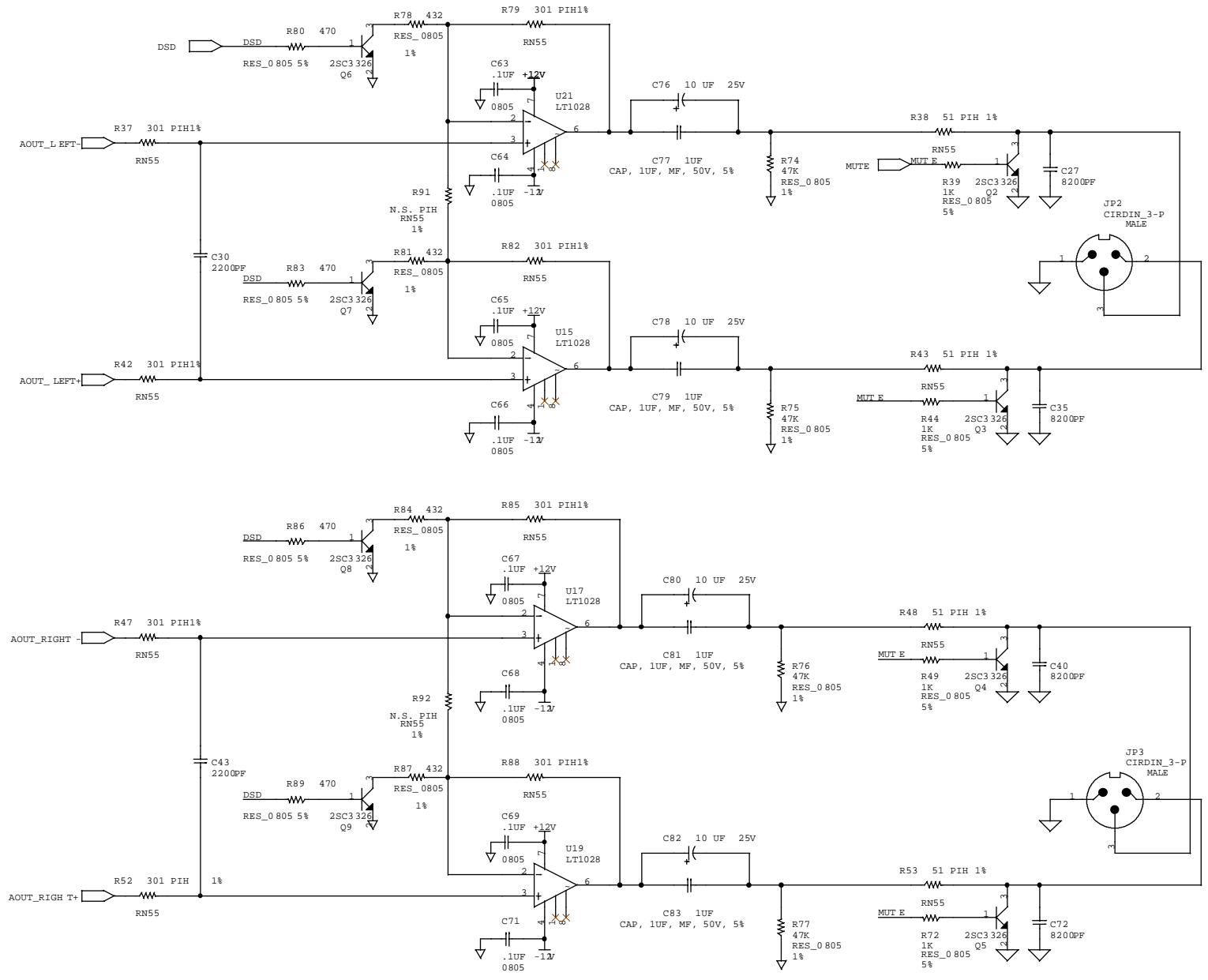


Figure 2. Output Filter

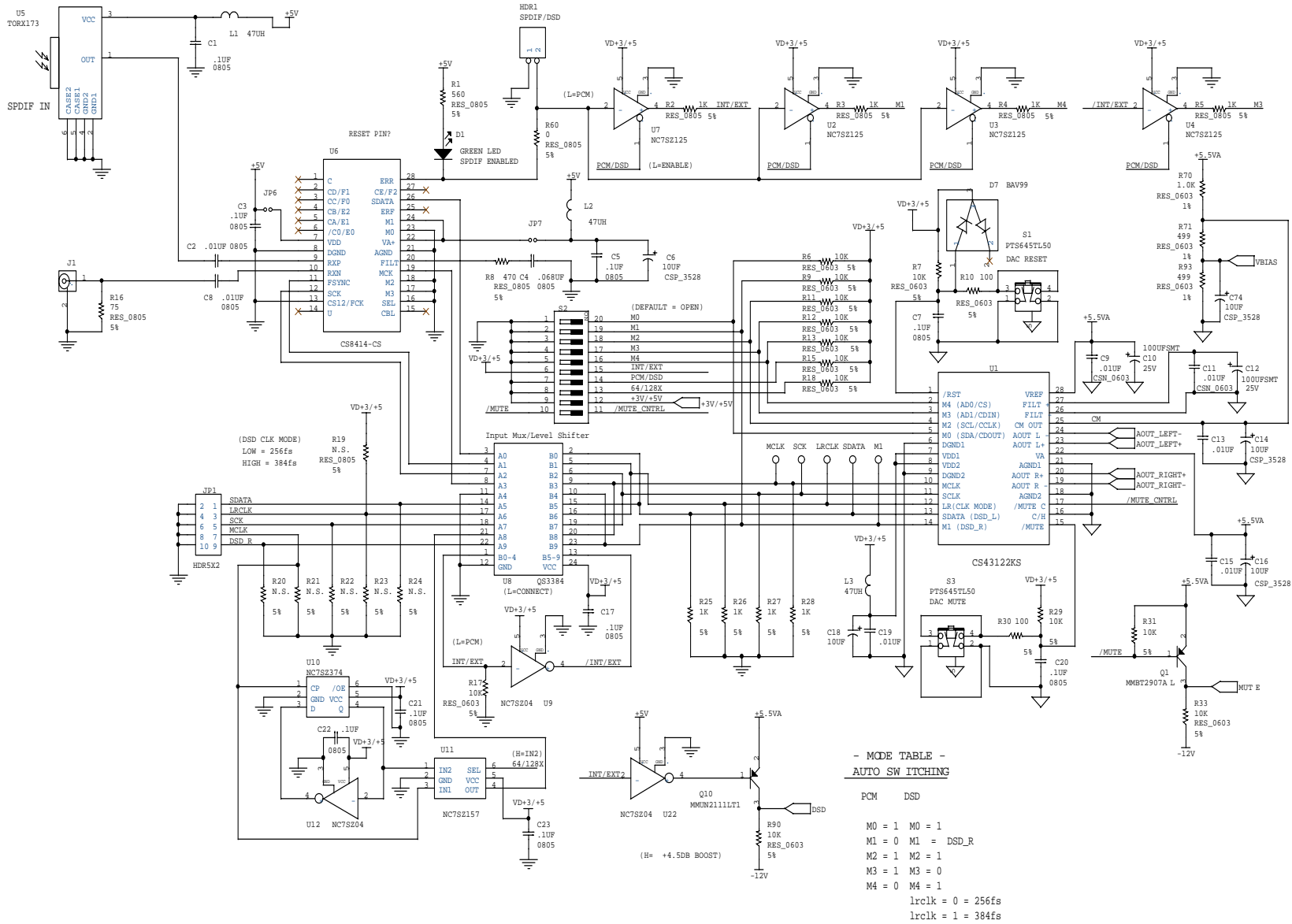
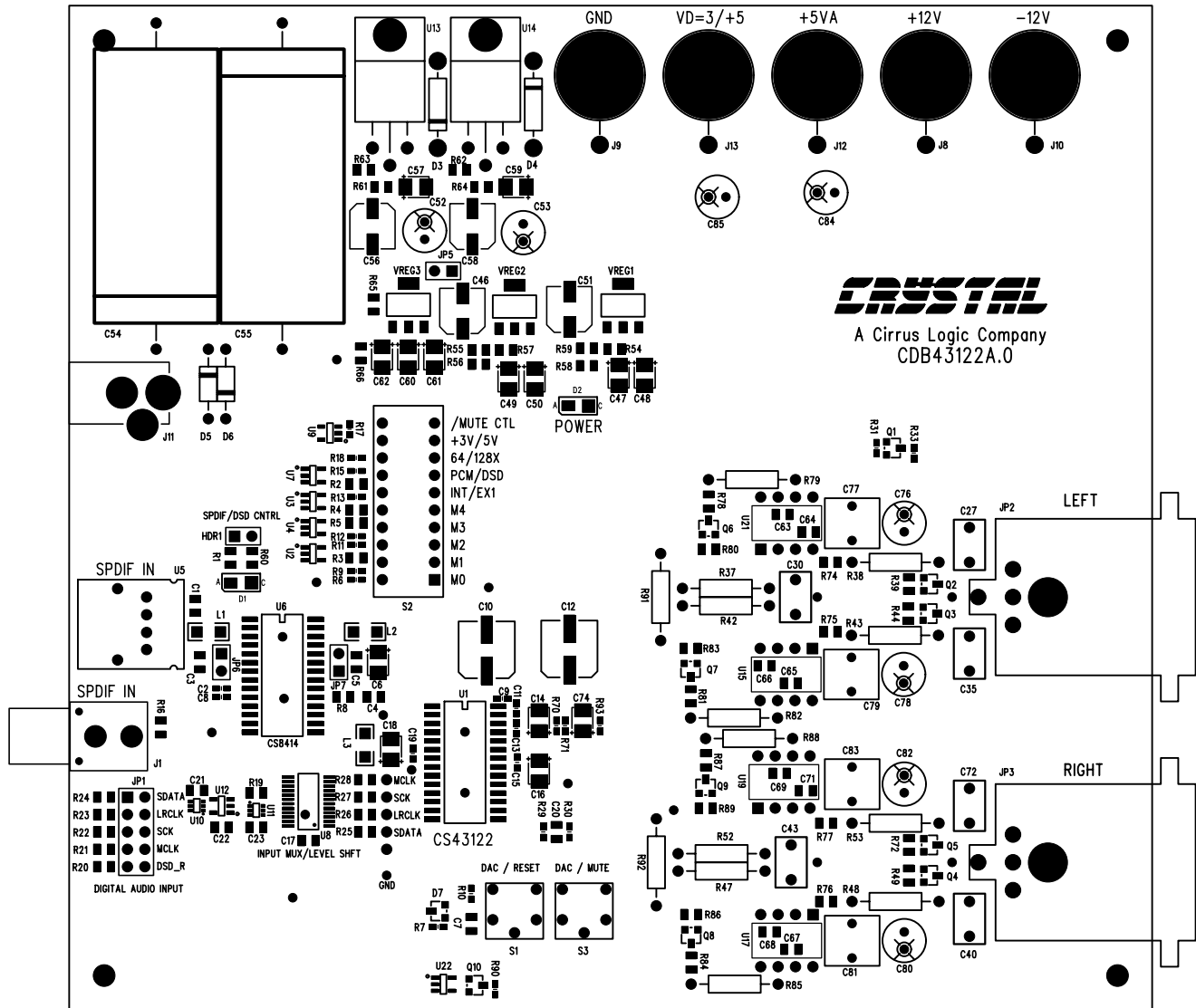


Figure 3. Input Receiver, DAC

CRYSTAL SEMICONDUCTOR

CDB43122 REV-A.0



TOP - SIG/GND

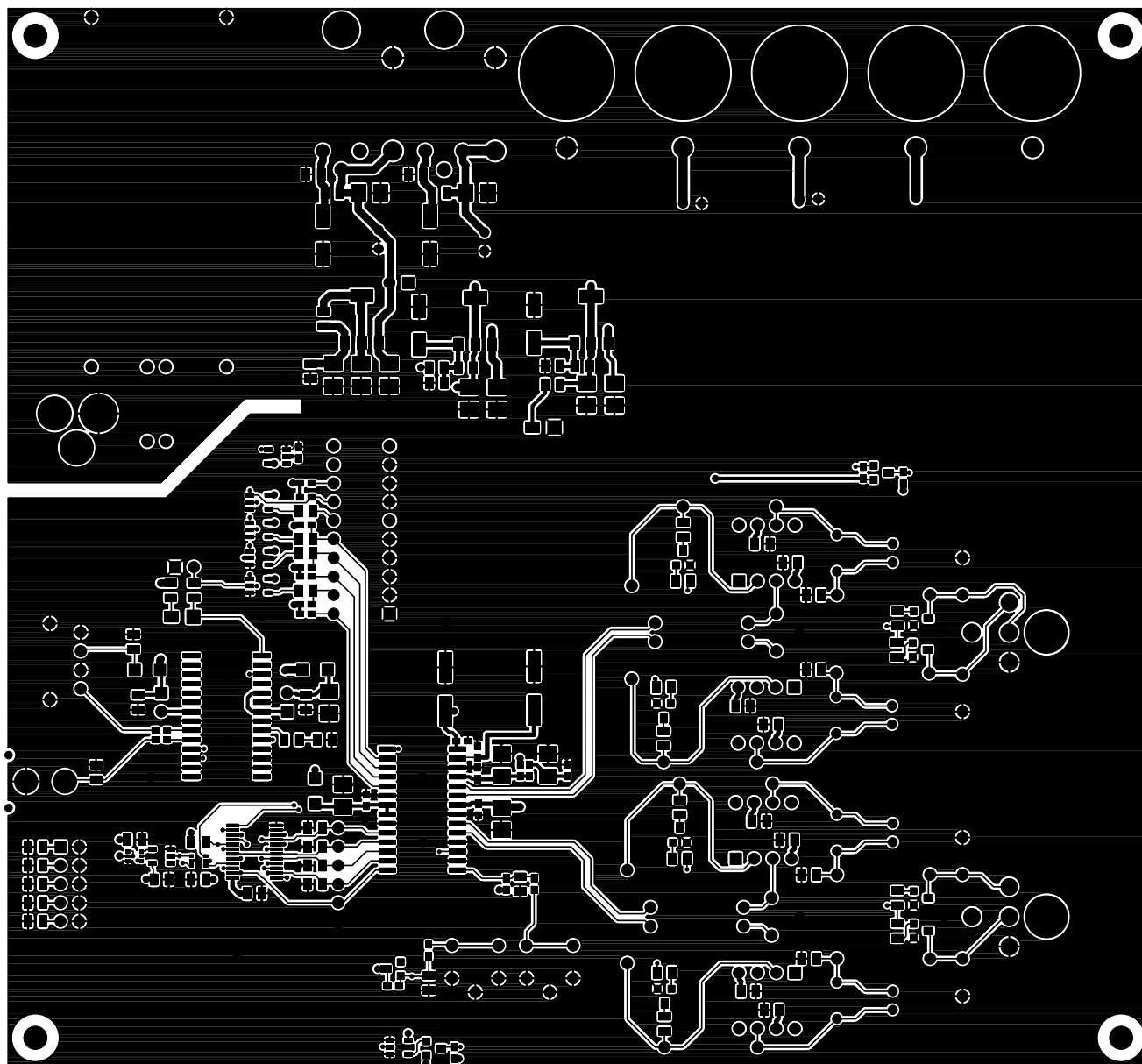
SILKSCREEN TOP

ASSEMBLY DRAWING TOP

Figure 4. Silkscreen Top

CRYSTAL SEMICONDUCTOR

CDB43122 REV-A.0

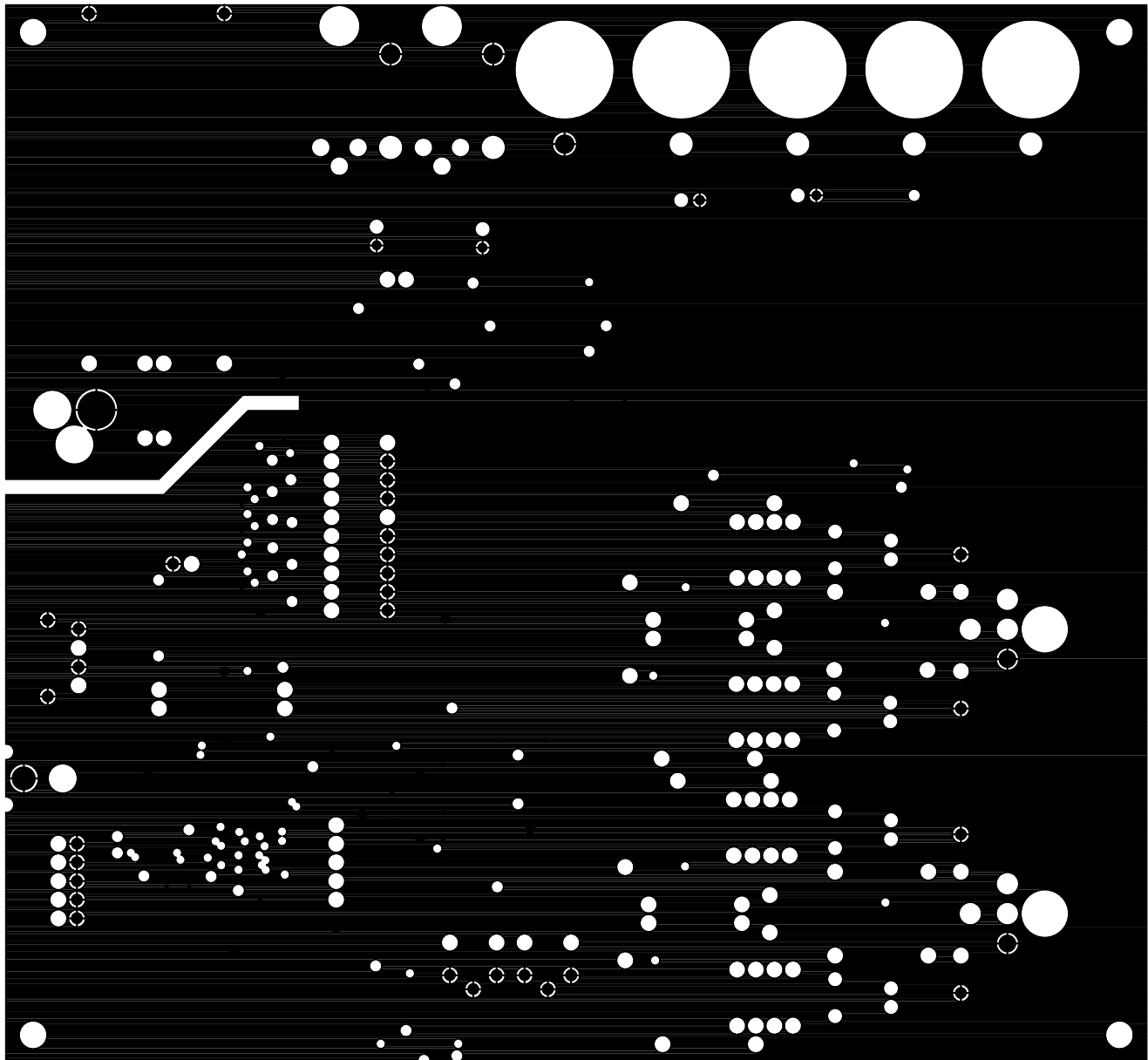


TOP - SIG/GND

Figure 5. Top Layer

CRYSTAL SEMICONDUCTOR

CDB43122 REV-A.0

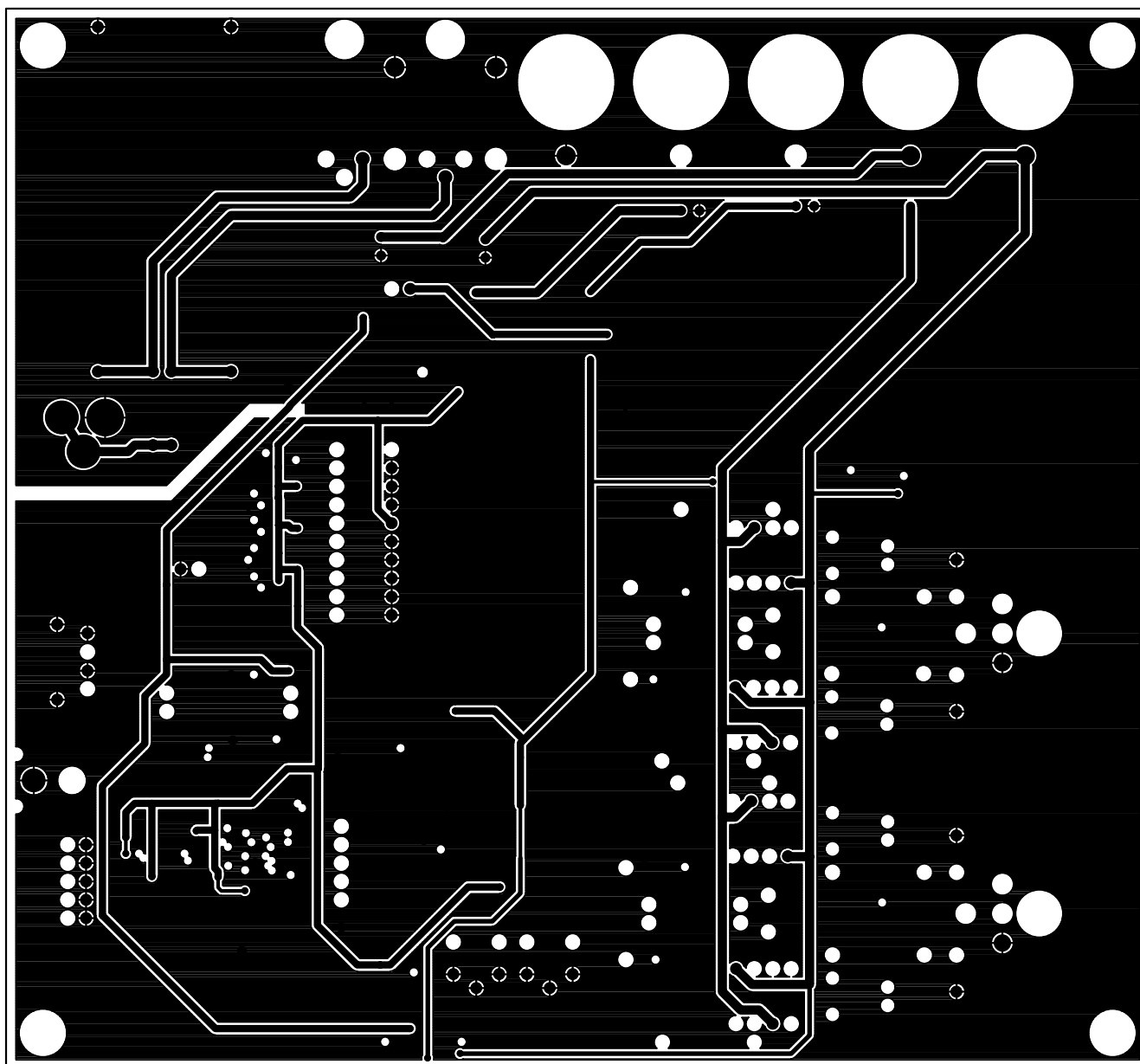


LAYER2 - GND

Figure 6. Second Layer

CRYSTAL SEMICONDUCTOR

CDB43122 REV-A.0

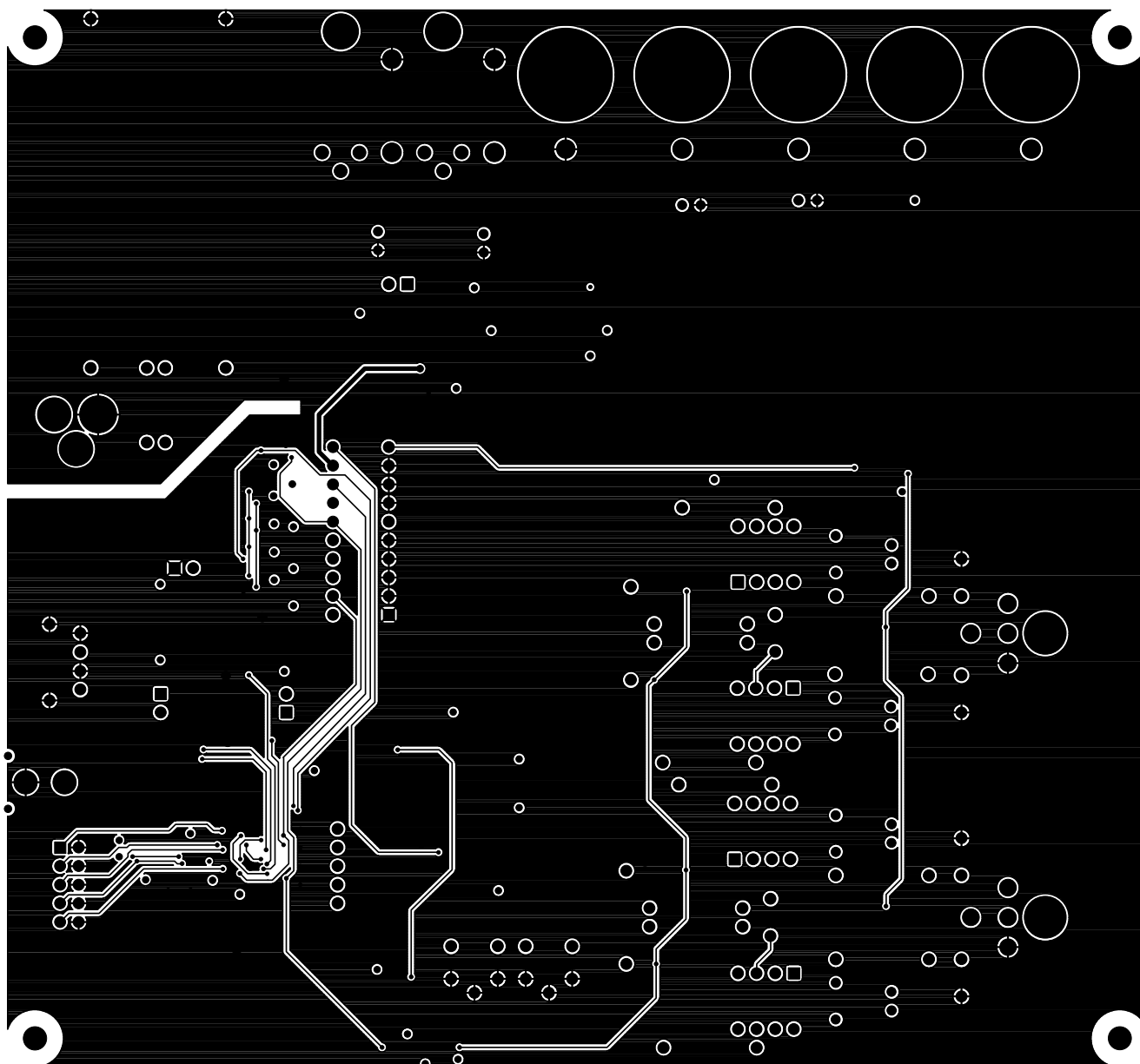


LAYER3 - PWR

Figure 7. Third Layer

CRYSTAL SEMICONDUCTOR

CDB43122 REV-A.0



BOTTOM - SIG/GND

Figure 8. Bottom Layer

SMART
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