CS43122 White Paper

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INTRODUCTION

The Crystal CS43122 design team began with a “clean sheet of paper” and the goal of replacing existing top-end audio converters by redefining the standards for performance and sound quality for high-end audio DACs. The design team focused on designing in improved ease-of- use and an expanded feature set over previous generations of CMOS converters. The CS43122 supports all existing and new industry standard audio formats. This device, now in production, represents the current state-of-the-art in audio signal conversion and demonstrates the innovative thinking found in new audio converter design at Cirrus Logic.

The CS43122 achieves both very low in-band and out-of-band noise interference in a standard 0.35µ 3V/5V N-Well digital CMOS process, using an optional double-poly capacitor module. The original set of specifications precluded the use of conventional single-bit modulation schemes, so the design team researched and implemented some new design strategies.

DIGITAL ARCHITECTURE

The digital section of the CS43122 interpolates incoming PCM data from the serial interface by 8x in the 48 kHz and 96 kHz modes, and by 4x in the 192 kHz input mode. All modes make use of multi-stage FIR interpolation filters, the first stage of each being a half-band structure. Each filter is micro-programmed into a small ROM and executed by a simple shift-and-add ALU engine that uses canonic-signed-digit arithmetic (descending power of 2 coefficients). It runs at a nominal 24.576MHz clock rate. The delta-sigma modulators and DAC analog blocks operate at a constant rate of 128*48 kHz, or 6.144 MHz (when the input rate is a multiple of 48 kHz). Thus, a zero-order-hold is used to raise the output of each of the interpolation filters to the necessary modulator rate, resulting in an overall interpolation ratio of 128x at 48 kHz (1x mode), 64x at 96 kHz (2x mode), and 32x at 192 kHz (4x mode). Digital de-emphasis filtering, available in the 1x mode at 32, 44.1 or 48 kHz, is also realized in the micro-programmed filter engine.

The highest interpolation filter stop-band attenuation is realized in the “1x” or 48 kHz input mode, and features out-of-band image rejection of over 100 dB. Due to the fixed number of master clock cycles available to compute each upsampled output in the ALU, the overall filter lengths are shorter in the higher rate 2x and 4x modes. In these modes, however, the filter performance is still very good, but the stop-band attenuation is relaxed compared to that in the 1x mode.

A third order, 5-bit, multiple-feedback delta-sigma architecture with second generation DEM (Dynamic Element Matching), and switched capacitor discrete time DAC was chosen for this design. The advanced DEM circuitry utilizes a patent-pending restricted- search 2^{nd} order mismatch shaping Data-Weighted-Averaging algorithm, known as R2DWA [1]. It guarantees that the output spectrum will be free of distortion components, due to static non-linearity in the analog section. This non-linearity arises from random capacitor mismatch in the linearly arrayed, multi-element DAC. The random mismatch error is effectively 2^{nd} order “noise-shaped”, by the DEM circuitry, such that the bulk of the error noise spectrum is pushed up out of the audio band. The restricted-search method employed is a good trade-off between design complexity and performance, and is relatively immune to low level tone artifacts.

The use of a third-order, dithered, 25-level delta-sigma modulator provides an attendant reduction in ultrasonic shaped noise by dramatically reducing the digital feedback step size. The zero input idling pattern, in the DAC modulator, is typically three codes wide (out of a possible 25), and is much lower in amplitude than the usual 50% 1/0 idling pattern of a single bit modulator. A bilinear dither generator, using a 23-bit LFSR, outputs a signal that is ±0.625% of full scale, and is summed at the quantizer input in the multi-bit modulator. The pseudo-random sequence repetition rate is less than 1 Hz, at a 6.144 MHz sampling rate, and is not audible. This helps to randomize delta tones, occurring at $F_{modulator}/2$, which are seen when the DC output level is exactly mid-way between any pair of adjacent quantization levels. Visible in band limit cycle tones, although extremely low in amplitude, are effectively randomized by the dither generator.

ANALOG ARCHITECTURE

The analog section of the DAC employs a 25-level (24-element) fully differential switched capacitor output filter, using a single active integrator with direct charge transfer and modified 2-phase clocking. The amplifier used in this design is a two-stage medium bias (2.5 mA per output leg) non-folded cascode class-AB design, with current-mode quiescent bias control, and continuous time common-mode feedback. The large CMOS output stages were designed to drive a balanced load of less than 2kΩ, with very low audio band distortion.

A single pole low-pass cutoff at approximately 196 kHz is an inherent feature of this DAC, when operating at 128*48 kHz, or 6.144 MHz. The elevated cutoff frequency was chosen, such that it was at least twice that of the highest reproducible signal, at a 192 kHz sampling rate. It does not need to be re-programmed for changes in operating mode, and thus allows for a fixed sampling-to-integration capacitor ratio (5 in this case). The phase shift and droop of this single pole filter are minimal below 20 kHz, but still digitally compensated. At high sample rates (96 kHz and 192 kHz), the in-band droop is more severe, and must be digitally compensated by the internal multi-stage interpolation filter to realize required passband flatness.

Each differential analog output channel of the CS43122 is essentially a superposition of the outputs of 24 identical, unit-element, fully differential DACs. They are driven by a randomized thermometer coded output, from the DEM digital section, with an idling level centered around code 0 (the output is coded as –12,….0,….+12). All charge packets from the unit element DACs are combined in the direct charge transfer integrator to produce the sum total analog output with the desired 196 kHz LPF function.

A unique reference-sampling scheme employs rough and fine charge phases to effectively low pass filter noise on the VREF input pin. Thus, the 5 V analog power supply may be used as a voltage reference input. It generates a single-pole low-pass discrete-time transfer function. This function is related to the DAC sampling frequency and the ratio between the total internal capacitance switched to the VREF terminal (100 pF) and a large external filter capacitor (>100 µF) on the FILT+ terminal. During the 8 ns Phase-1 rough-charge period, half the DAC sampling capacitors are switched directly to the VREF pin (and the other half are grounded). Subsequently, during the much longer Phase-1 fine-charge period, the same half-set of DAC sampling capacitors are connected to the large external filter capacitor on the FILT+ pin, which is used to complete reference sampling. This technique provides as much as 60 dB of noise rejection on the VREF pin at 1 kHz.

LAYOUT

The CS43122 design team devised several new layout techniques to mitigate noise coupling between the digital and analog sections and to quench digital power bus bounce. The digital section uses hundreds of on-chip N-gate bypass capacitors, which are placed underneath the power rail distribution system. At the –122 dB level, A-weighted integrated noise in the DC-20kHz band is a mere 1.985 µV RMS - a very stringent requirement. Any coupling of periodic tones or spikes will be very noticeable against the low spectral density of the analog noise floor.

Great care was therefore invested to make sure the digital and analog layouts were optimal. All signals crossing between the digital/analog domains are electrically level-shifted using isolated cross-coupled inverters. This ensures that no direct connection is necessary between the analog and digital grounds on the chip that could corrupt the quiet internal analog supplies. Consequently, no noisy digital signal is ever allowed into the analog section. It is re-referenced to analog +5 V instead, and then routed to its destination.

The internal reference-bussing scheme had to accommodate fast, high-current pulses from an external HF bypass capacitor during the 8 ns rough-charge phase (approximately 80 mA peak) without ringing. It uses a differentially ballasted, low-inductance, internal bus structure with extensive shielding between it and the active circuitry below. The balanced analog outputs for each DAC channel feature geometrically symmetrical layout, and massive, identical signal path lengths all the way out to the Aout+/Aout- bond pads. This improves output matching, eliminating differential routing resistance.

A modified substrate noise management approach allows independent return paths for digital sub-tie and analog sub-tie connections and prevents extremely noisy digital substrate displacement currents from coupling into the quiet analog section. The digital sub-tie bus terminates at its own dedicated package pin and is tied down externally to the board ground-plane. This affords complete isolation from the internal analog ground bus.

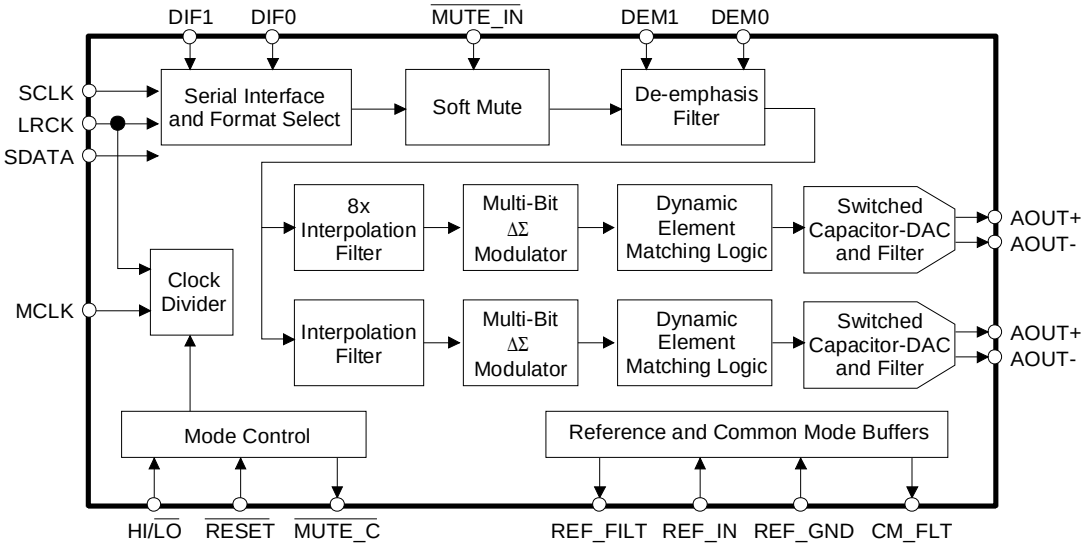
CONCLUSION

Many innovative circuit design and layout techniques were employed to make this product release possible. In addition to the solid engineering practices implemented throughout the design phase, much thought was given to floor planning and layout to provide transparent digital-to-analog conversion and deliver unprecedented sound quality for the ultimate listening experience.

Note: The block diagram for the Crystal CS43122 on the next page provides a detailed description of the device design.

REFERENCES

[1] Gong, Xue-Mei et al “A 120dB Multi-bit SC Audio DAC with Second-Order Mismatch Shaping”, ISSCC 2000 digest of technical papers, copyright 2000 IEEE.



Crystal CS43122 Block Diagram