CDB43L42

Evaluation Board for CS43L42 Rev. D

Features

- Demonstrates recommended layout and grounding arrangements
- CS8415A receives AES/EBU, S/PDIF, and EIAJ-340 Compatible Digital Audio
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

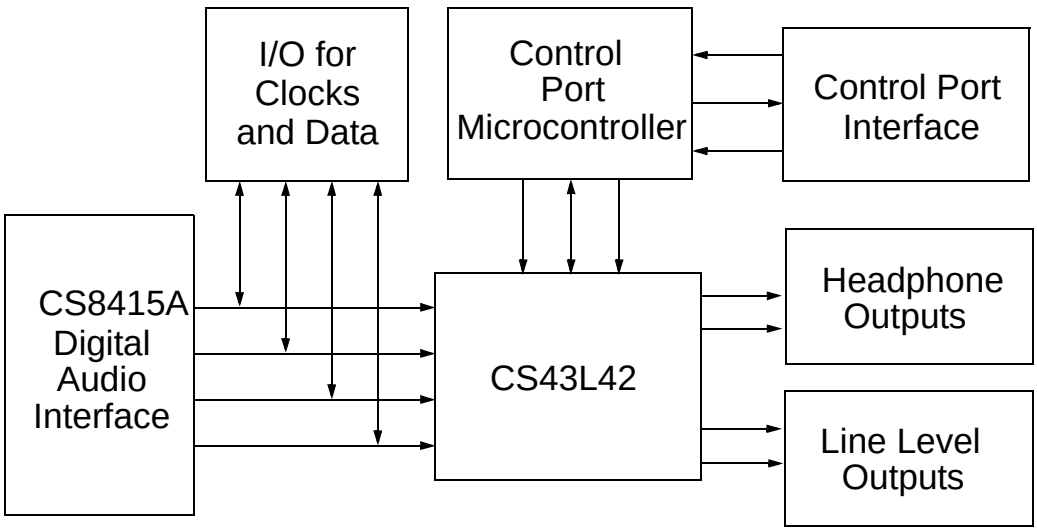
Description

The CDB43L42 evaluation board is an excellent means for quickly evaluating the CS43L42 24-bit, stereo D/A converter. Evaluation requires an analog signal analyzer, a digital signal source, a PC for controlling the CS43L42 (for control port mode only) and a power supply. Analog headphone outputs are provided via a 1/8" headphone jack and RCA phono jacks. Line outputs are provided via RCA phono jacks.

The CS8415A digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converter and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB43L42	Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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Contacting Cirrus Logic Support

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http://www.cirrus.com/corporate/contacts/

1. CDB43L42 SYSTEM OVERVIEW

The CDB43L42 evaluation board is an excellent means of quickly evaluating the CS43L42. The CS8415A digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB43L42 schematic has been partitioned into 12 schematics shown in Figures 2 through 13. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS43L42 DIGITAL TO ANALOG CONVERTER

A description of the CS43L42 is included in the CS43L42 datasheet.

3. CS8415A DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8415A Digital Audio Receiver, Figure 4. The outputs of the CS8415A include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256 x Fs master clock. The operation of the CS8415A and a discussion of the digital audio interface are included in the CS8415A datasheet.

The evaluation board has been designed such that the input can be either optical or coax, see Figure 5. However, both inputs cannot be driven simultaneously.

4. CS8415A DATA FORMAT

The CS8415A data format is selected via software when in Control Port mode. When in Stand-Alone mode the CS8451A data format is selected via the DIP switch. See Table 2 for details.

5. HEADPHONE OUTPUT

A 1/8 inch, stereo headphone jack is included on the evaluation board for connecting 16 ohm or greater headphones to the CS43L42. If no headphones are connected to the 1/8 inch jack, then a 16 ohm resistor is connected to each of the CS43L42 headphone outputs, HP_A and HP_B. This is useful when evaluating the CS43L42 headphone amplifier with test equipment that has high-impedance inputs. RCA jacks are also provided on the headphone outputs for easy connection to test equipment.

6. LINE OUTPUT

The CS43L42 line level outputs are available via RCA jacks. An external mute circuit is included on the CDB43L42 to ensure an absolute minimum of extraneous clicks and pops during power-up. See Figure 12 for details.

7. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, HDR1. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 10.

8. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by six binding posts (GND, +5 V, VL, VA, VA_HP, and VA_LINE), see Figure 13. The +5 V input supplies power to the +5 Volt digital circuitry (VA_+5, VD_+5), while the VL input supplies power to the Voltage Level Converters and the CS43L42 VL pin. VA, VA_HP, and VA_LINE supply power to the CS43L42. For ease of use, it is possible to connect VA, VA_HP, VL, and VA_LINE to the same supply.

WARNING: VA, VL, and VA_LINE must be between +1.7V and +3.6V. VA_HP must be between

+0.9 V and +3.6 V. Operation outside of this range can cause permanent damage to the device. See the CS43L42 datasheet for more details.

9. GROUNDING AND POWER SUPPLY DECOUPLING

The CS43L42 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 2 details the power distribution used on this board. The decoupling capacitors are located as close to the CS43L42 as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yields large reductions in radiated noise. See Figures 26-28 for the CDB43L42 PCB layout artwork.

10. CONTROL PORT SOFTWARE

The CDB43L42 is shipped with Windows based software for interfacing with the CS43L42 control port via the serial connector, J1. The software can be used to communicate with the CS43L42 in Two Wire mode. Note: DIP 2-4 must be set appropriately for control port mode operation.

11. POPGUARD® IMPROVEMENT

The CDB43L42 Rev A includes a hardware improvement for the PopGuard® Transient Control feature of the CS43L42 Rev D. Please see the CS43L42 errata for further details. This additional hardware includes the transistors Q1, Q2, Q4, and Q5 as well as R13, R14, R24, R33, R34, and C7. Please refer to Figure 3. To bypass this hardware improvement, stuff R18 and R19 with 0 ohm resistors and change R25 and R26 to 1 k ohm resistors.

12. CDB43L42 PERFORMANCE PLOTS

The CDB43L42 Rev A performance plots shown in Figures 14 through 25 were generated using an Audio Precision System Two Cascade with the S2-AES17LP 20 kHz brickwall filter applied. All tests were performed at a sampling rate of 48 kHz and with VL, VA, VA_HP, and VA_LINE set to the indicated voltage supply. Please note that due to the architecture of the Audio Precision systems, either the S2-AES17LP 20 kHz brickwall filter must be installed or a low pass filter must be used between the CDB43L42 and the Audio Precision for proper measurements. If an external filter is used, it must provide at least 15 dB of attenuation at 120 kHz. This can be achieved with a simple 3-pole filter.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 V	Input	+ 5 Volt power
VA, VL, VA_LINE	Input	+ 1.8 Volt to + 3.3 Volt power for the CS43L42 and the Voltage Level Converters
VA_HP	Input	+0.9 Volt to +3.3 Volt power for the CS43L42 headphone amp
GND	Input	Ground connection from power supply
Coax Input	Input	Digital audio interface input via coax
Optical Input	Input	Digital audio interface input via optical
HDR1	Input/Output	I/O for master, serial, left/right clocks and serial data
Serial Port	Input/Output	Serial connection to PC for Two Wire mode control port signals
HDR2	Input/Output	I/O for Two Wire mode control port signals
HP_A (J3)	Output	Channel A headphone output
HP_B (J2)	Output	Channel B headphone output
HP_A&B (J10)	Output	Channel A and B headphone output
AOUTA ( )	Output	Channel A line output
AOUTB ( )	Output	Channel B line output

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
Program/Run	Programming switch for the control port microcontroller	Program *Run	Configures CDB43L42 to program the µC Configures CDB43L42 for normal operation
HRM/BRM	Selects High Rate or Base Rate Mode	HRM (/2) *BRM (x1)	Selects High Rate Mode Selects Base Rate Mode
EXT/INT SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode External SCLK Mode
Reset (S1)	Resets the CDB43L42		
DIP 1	Enable/Disable the CS8415A	*0 1	CS8415A is enabled (HDR1 is an output) Disabled (External Clocks and Data are input via HDR1)
DIP 2-4	Configures the interface format and CS43L42 operational mode	*000 001 010 011 100	Control Port mode Stand Alone mode, I2S Stand Alone mode, LJ24 Stand Alone mode, RJ16 (8415A not avail.) Stand Alone mode, RJ24

Notes: *Default factory settings

Table 2. CDB43L42 Jumper and Switch settings

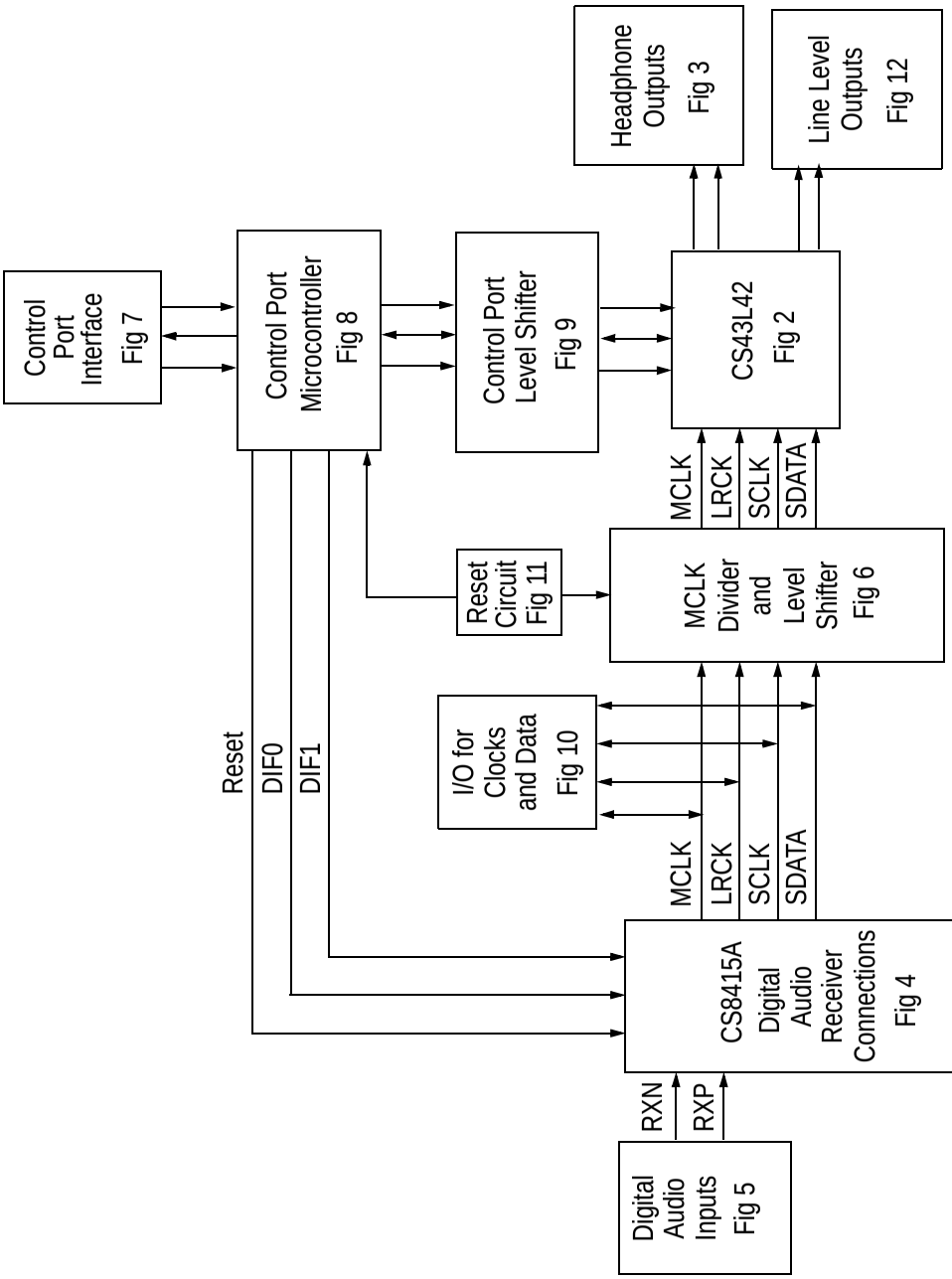


Figure 1. System Block Diagram and Signal Flow

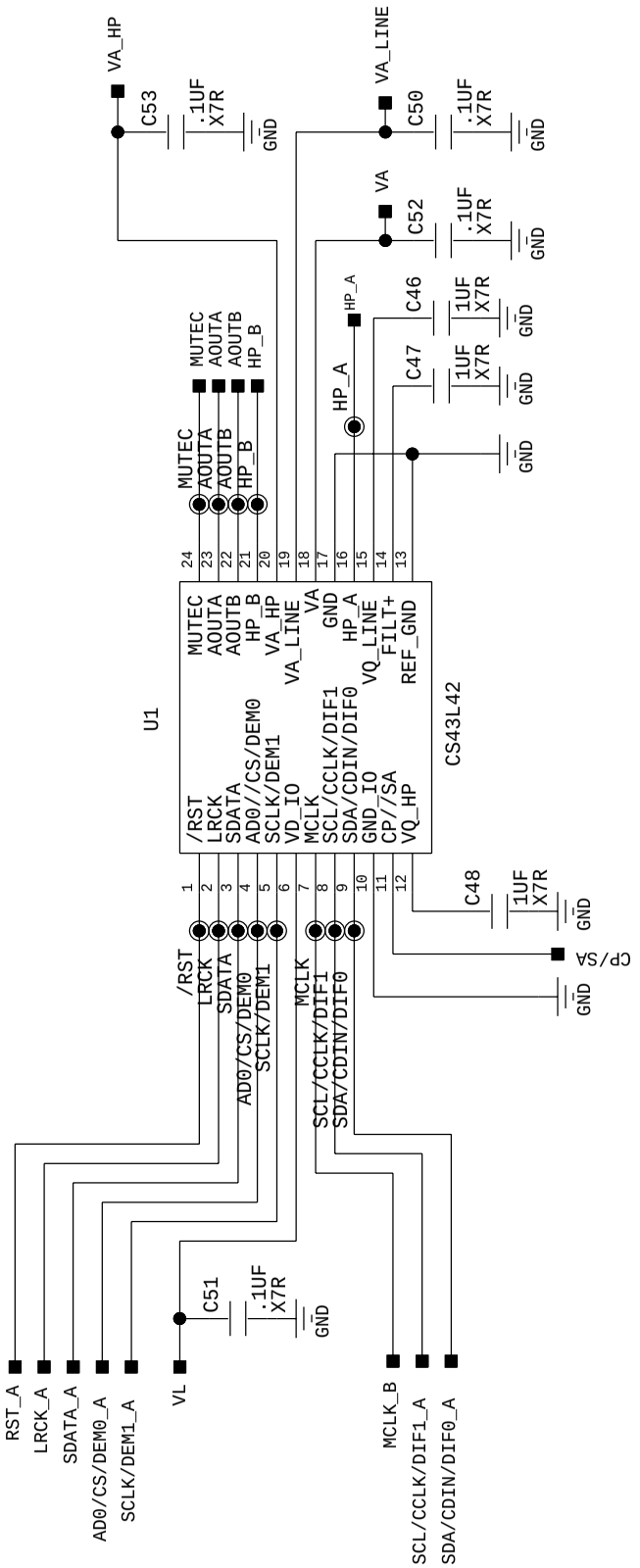


Figure 2. CS43L42

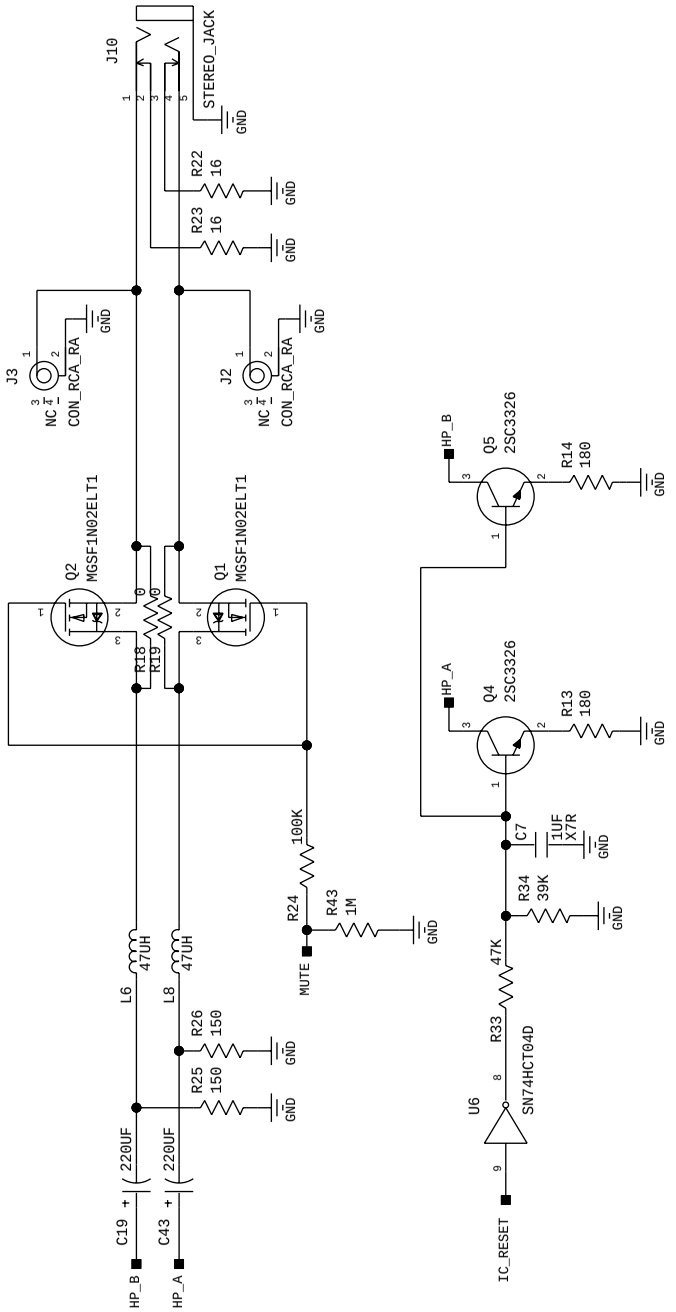


Figure 3. Headphone Outputs

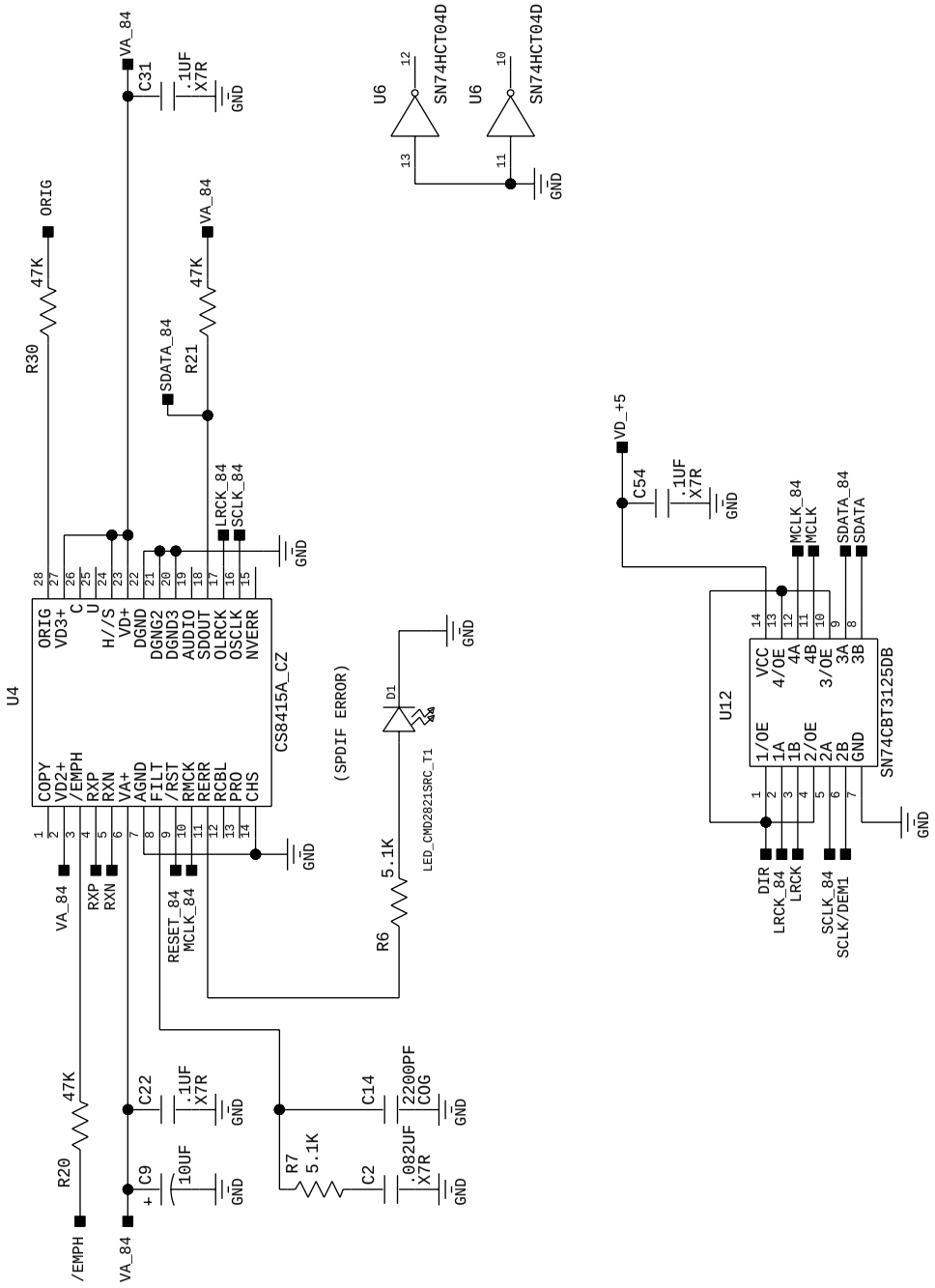


Figure 4. CS8415A Digital Audio Receiver

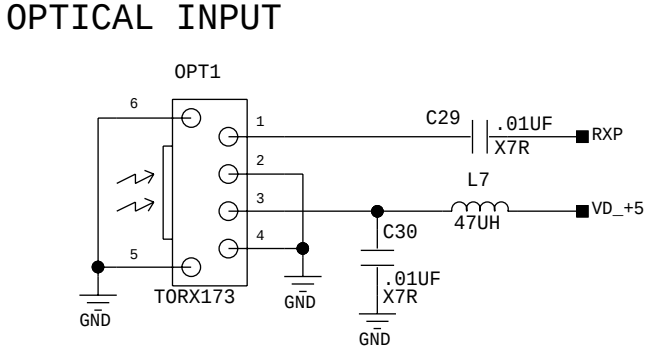


Figure 5. Digital Audio Inputs

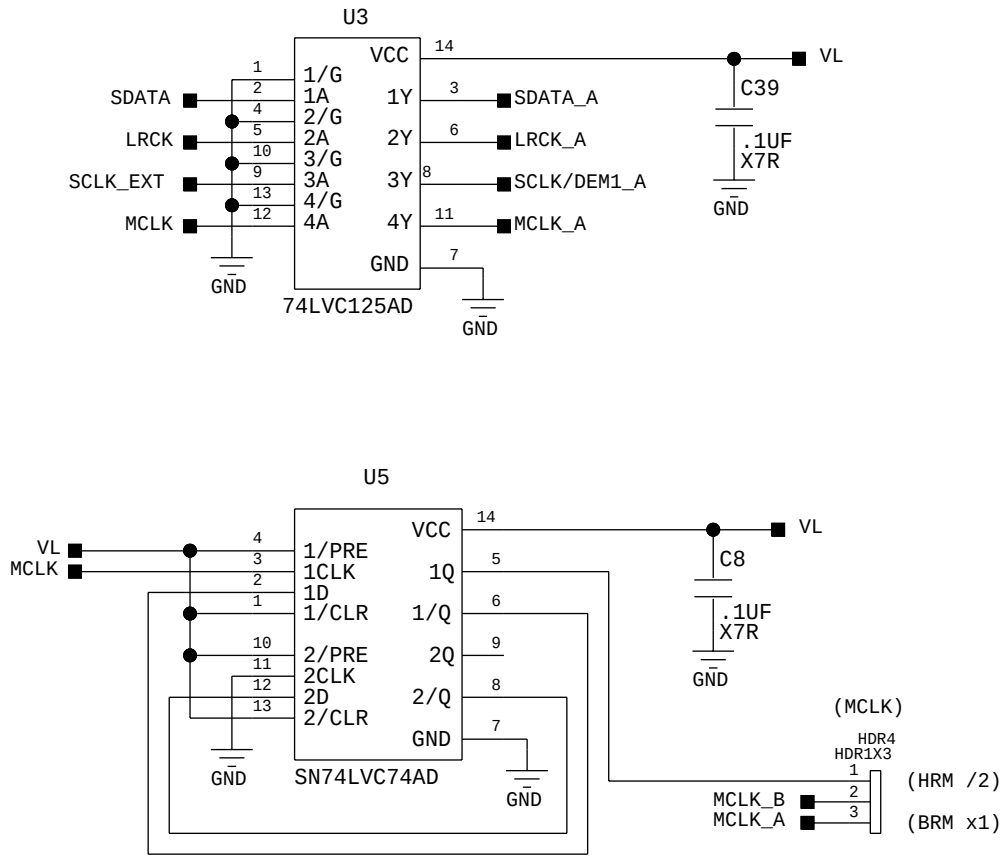


Figure 6. MCLK Divider and Level Shifter

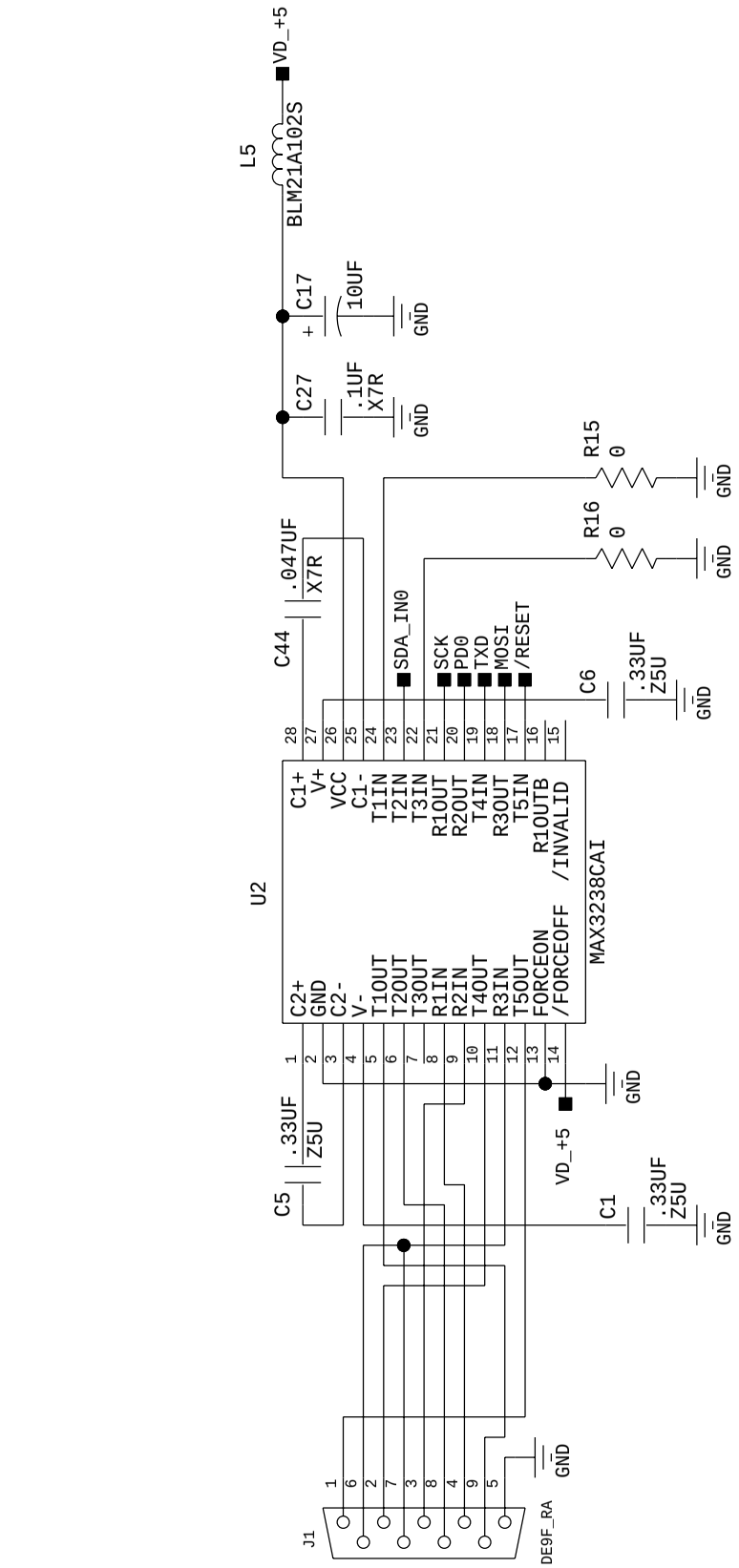


Figure 7. Control Port Interface

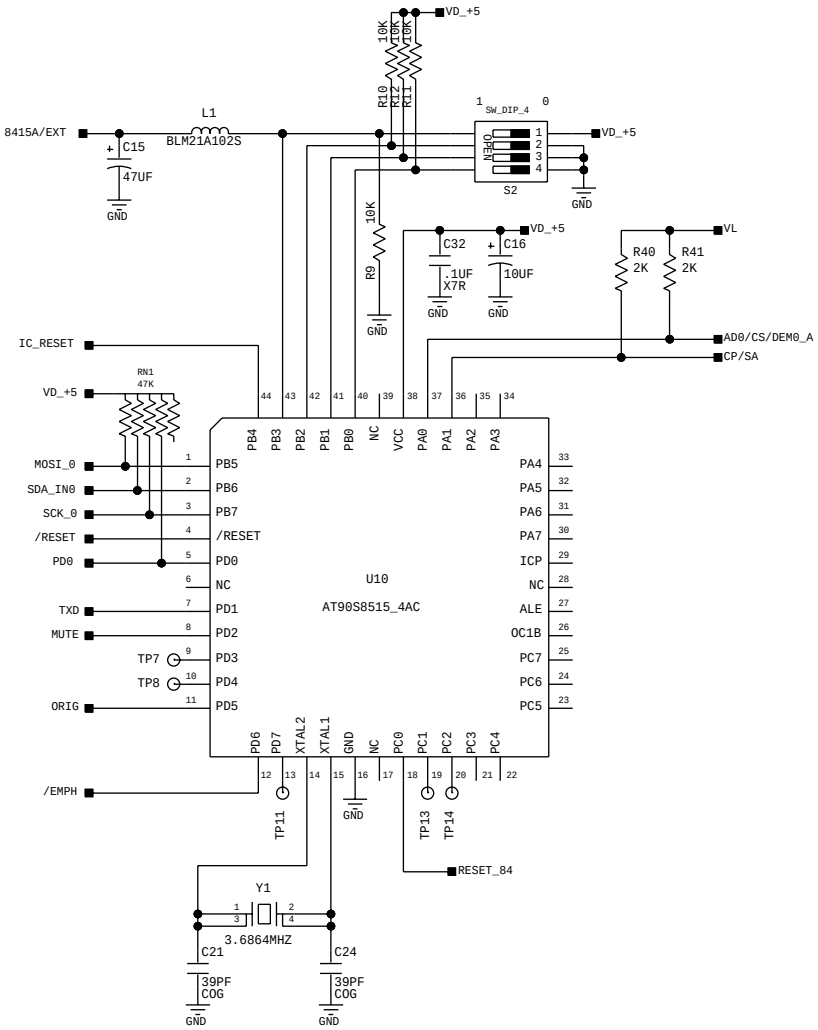


Figure 8. Control Port Microcontroller

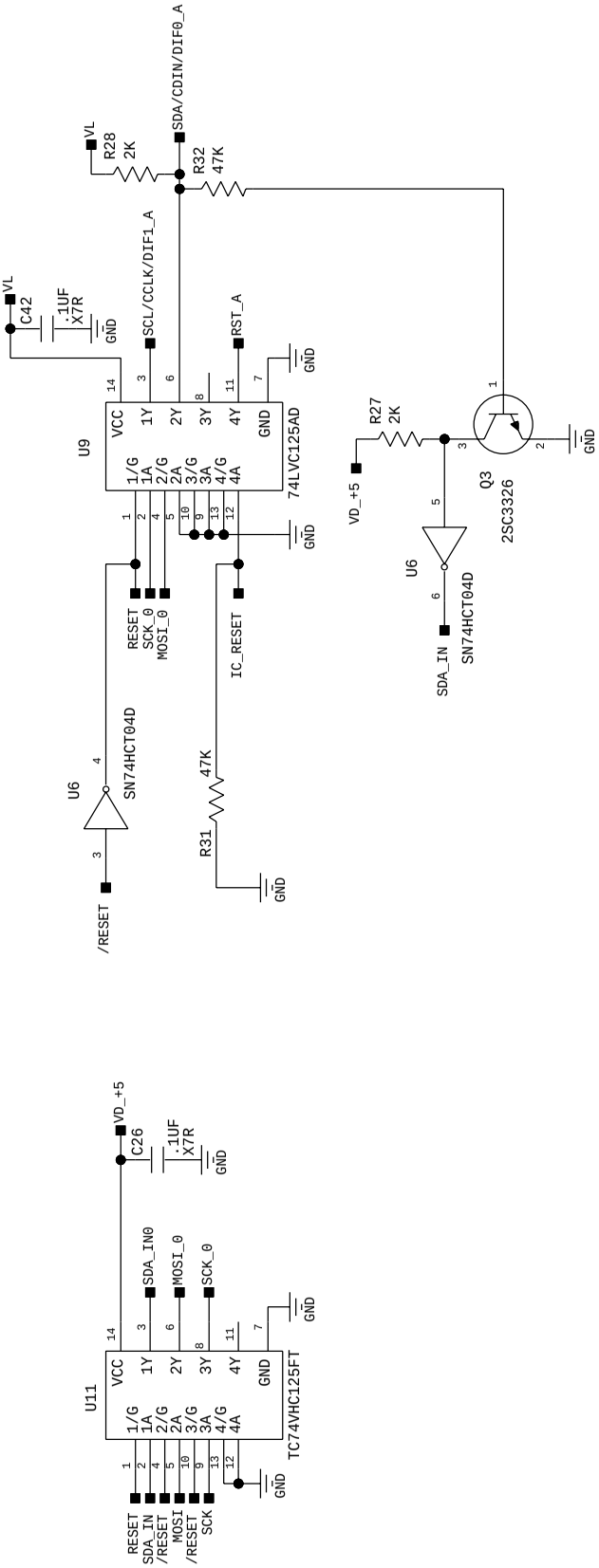


Figure 9. Control Port Level Shifter

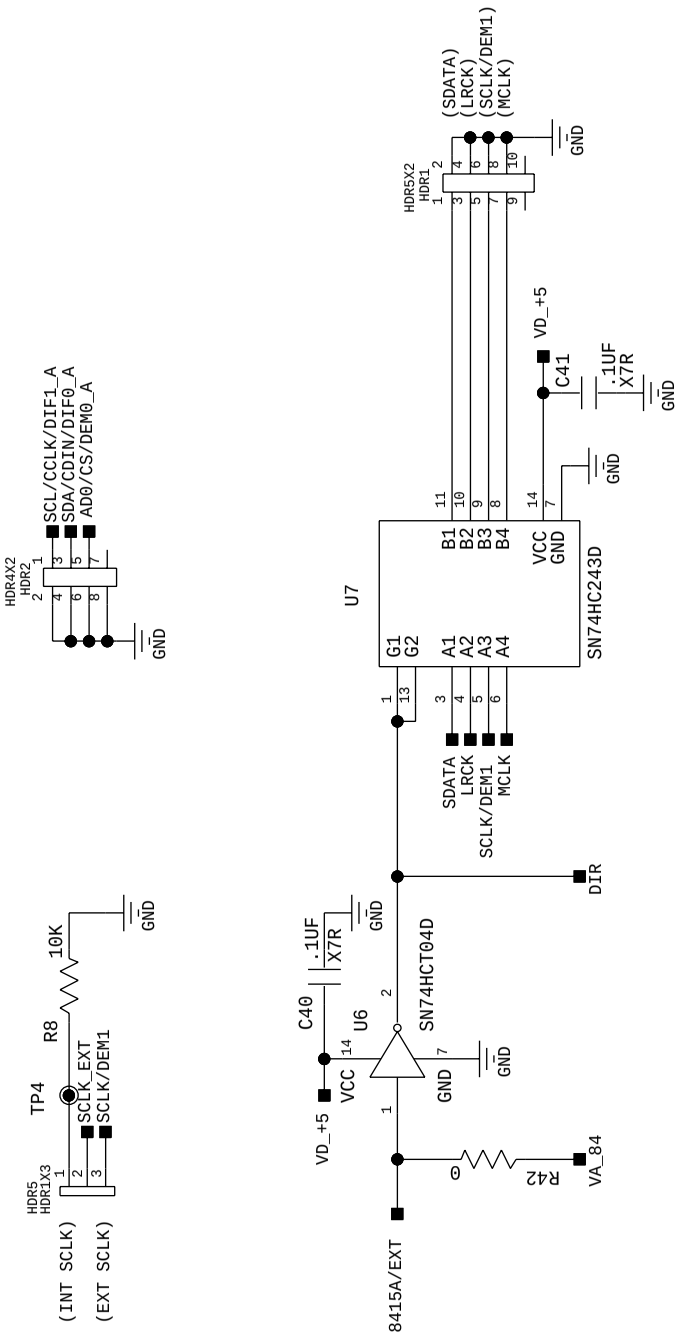


Figure 10. I/O for Clocks and Data

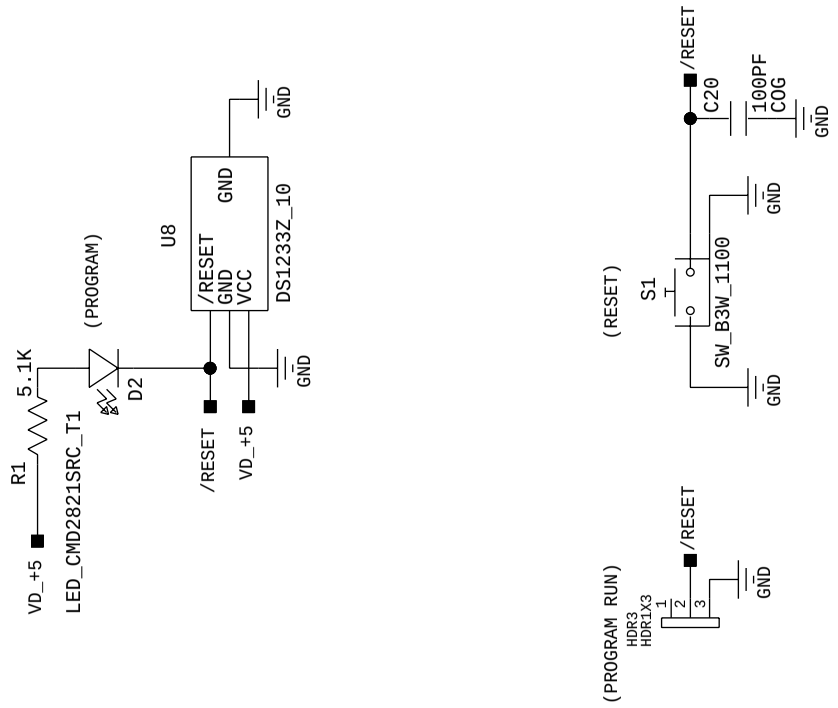


Figure 11. Reset Circuit

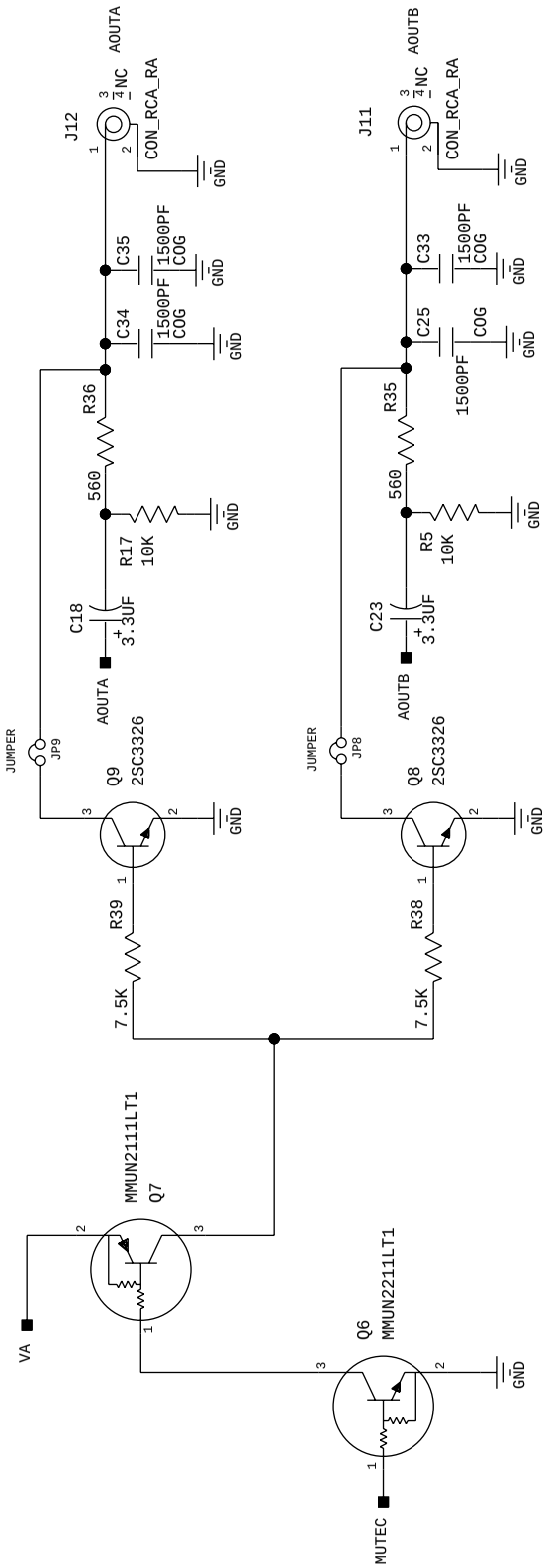


Figure 12. Line Level Outputs

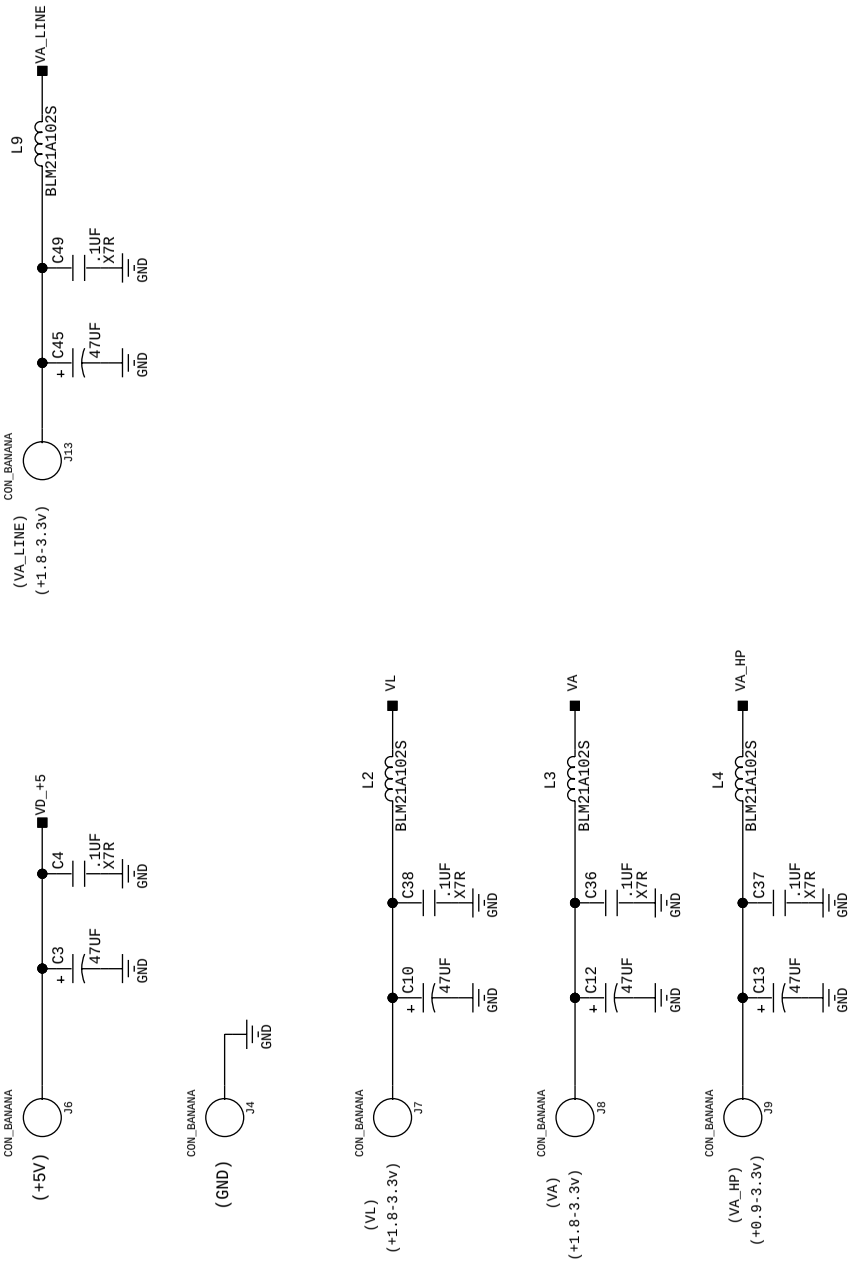


Figure 13. Power Supply

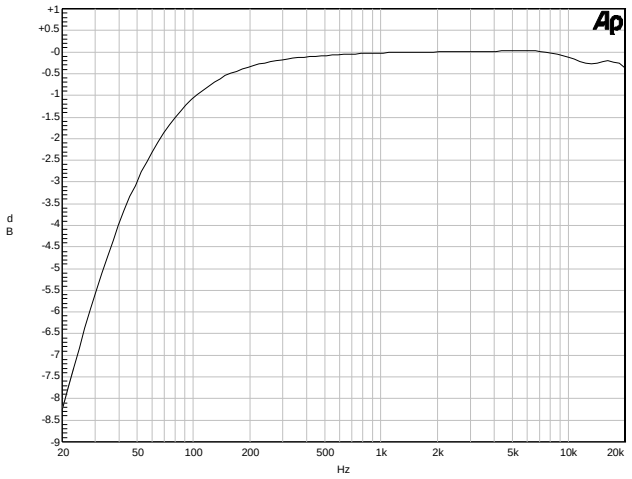


Figure 14. Headphone Output - Frequency Response at 1.8 V

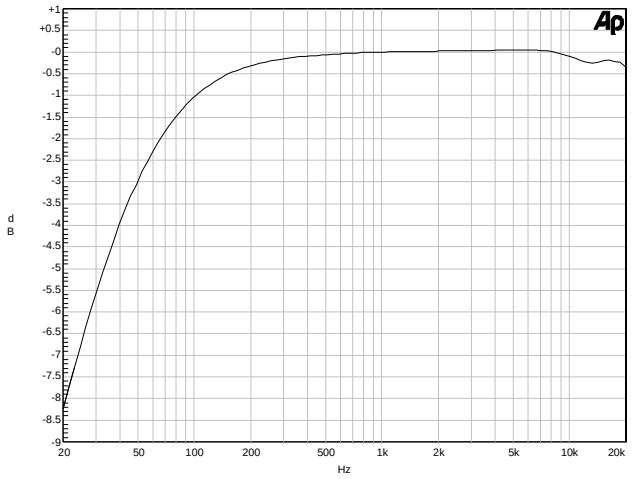


Figure 15. Headphone Output - Frequency Response at 3.0 V

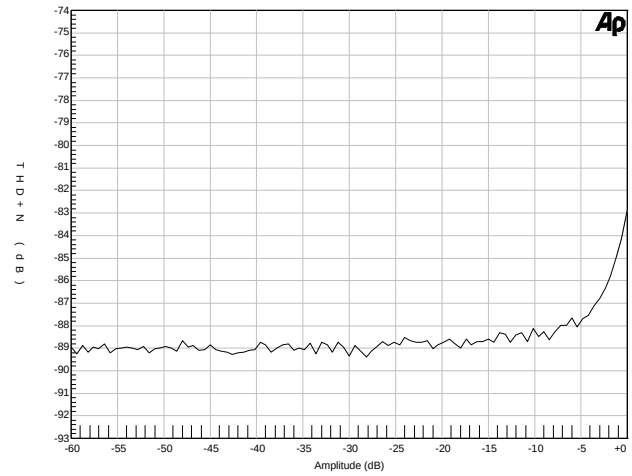


Figure 16. Headphone Output - THD+N versus Amplitude at 1.8 V

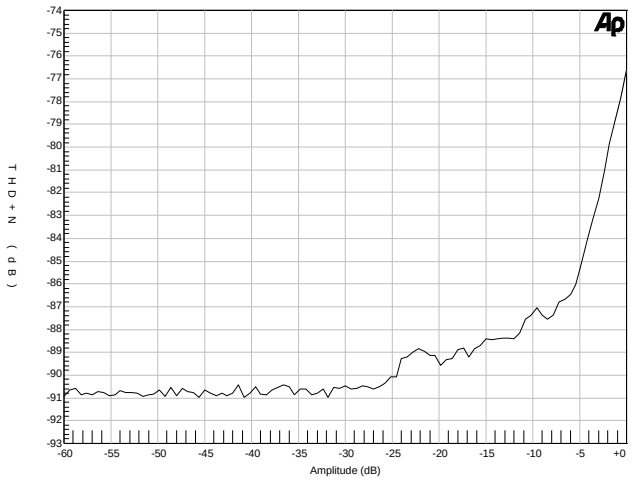


Figure 17. Headphone Output - THD+N versus Amplitude at 3.0 V

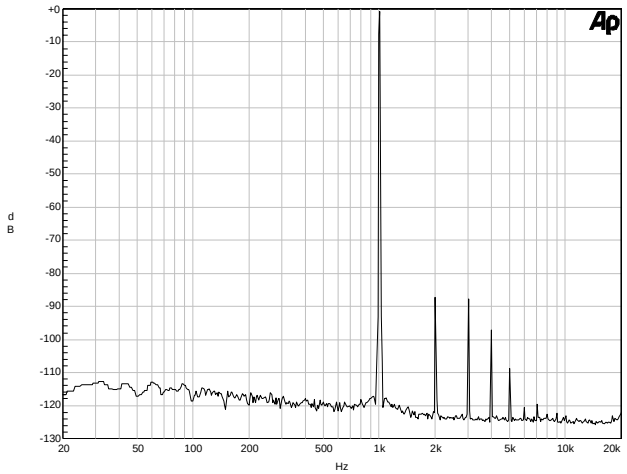


Figure 18. Headphone Output - FFT of 1 kHz Sine Wave at 1.8 V

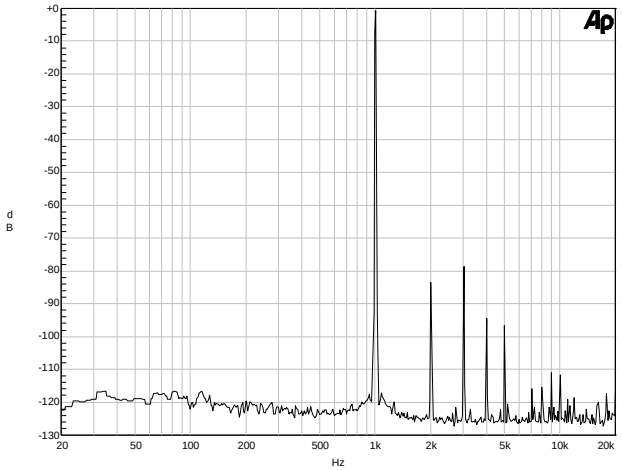


Figure 19. Headphone Output - FFT of 1 kHz Sine Wave at 3.0 V

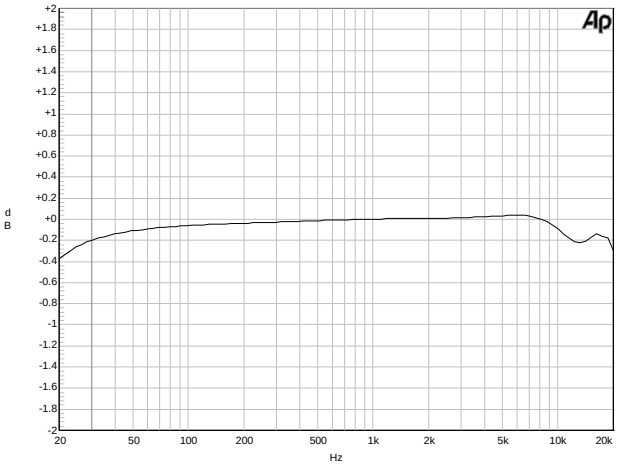


Figure 20. Line Output - Frequency Response at 1.8 V

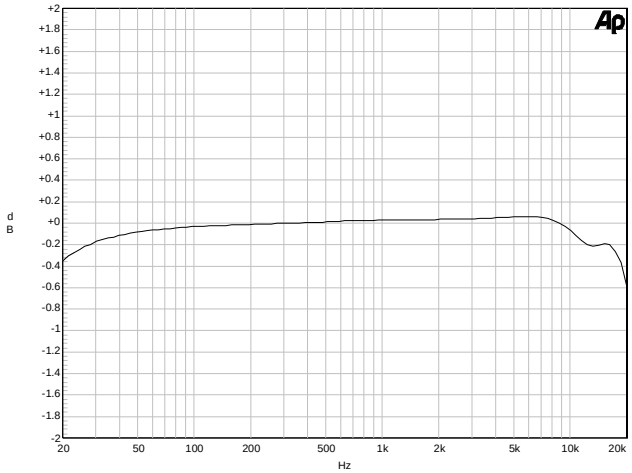


Figure 21. Line Output - Frequency Response at 3.0 V

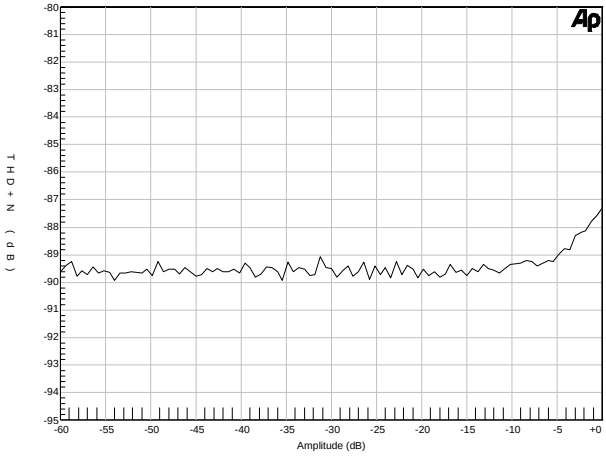


Figure 22. Line Output - THD+N versus Amplitude at 1.8 V

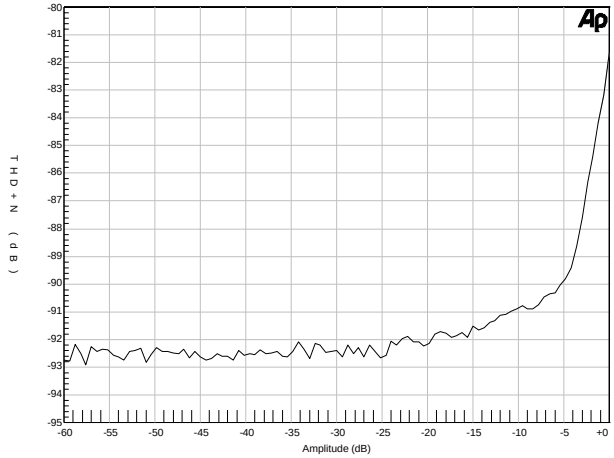


Figure 23. Line Output - THD+N versus Amplitude at 3.0 V

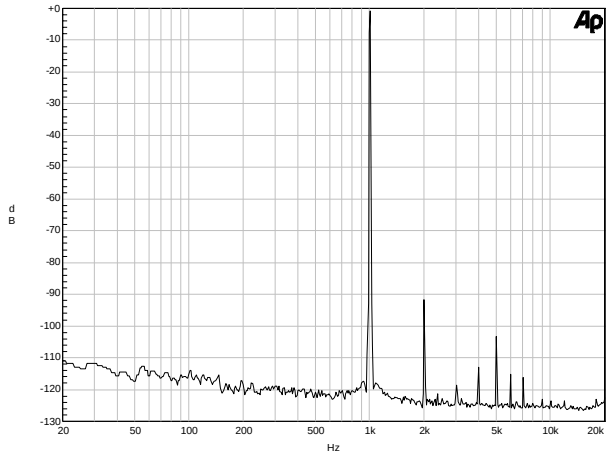


Figure 24. Line Output - FFT of 1 kHz Sine Wave at 1.8 V

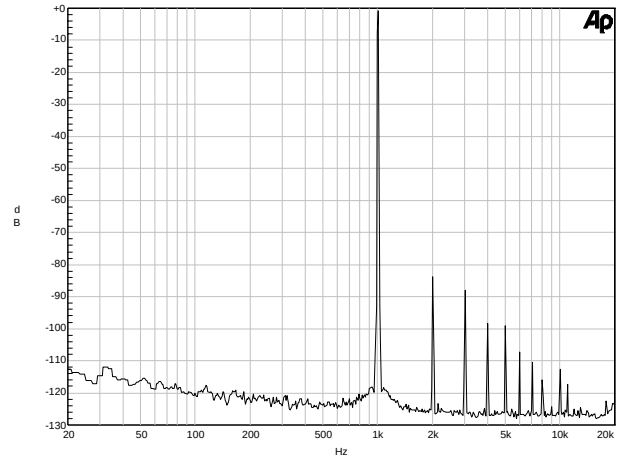


Figure 25. Line Output - FFT of 1 kHz Sine Wave at 3.0 V

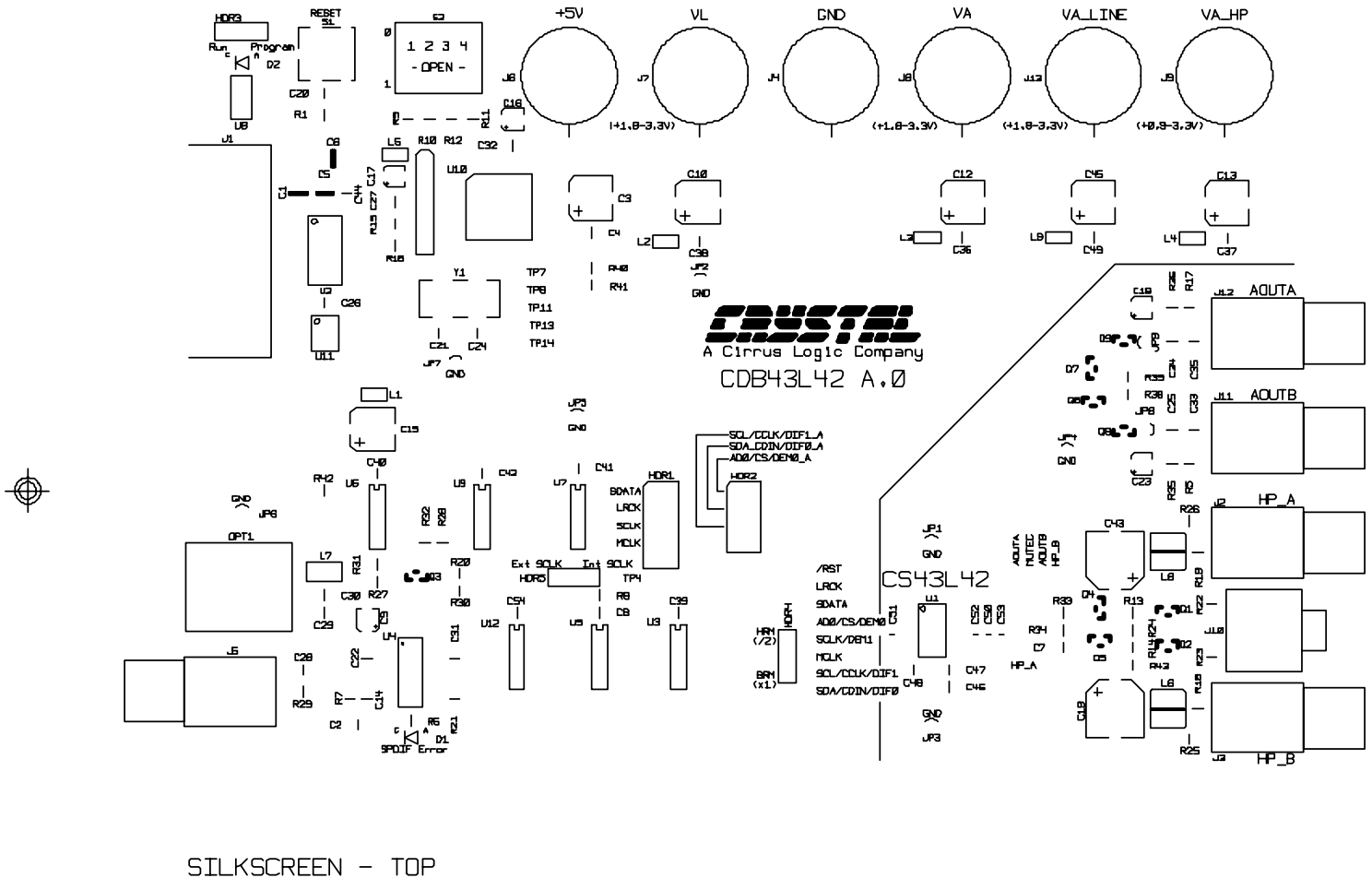
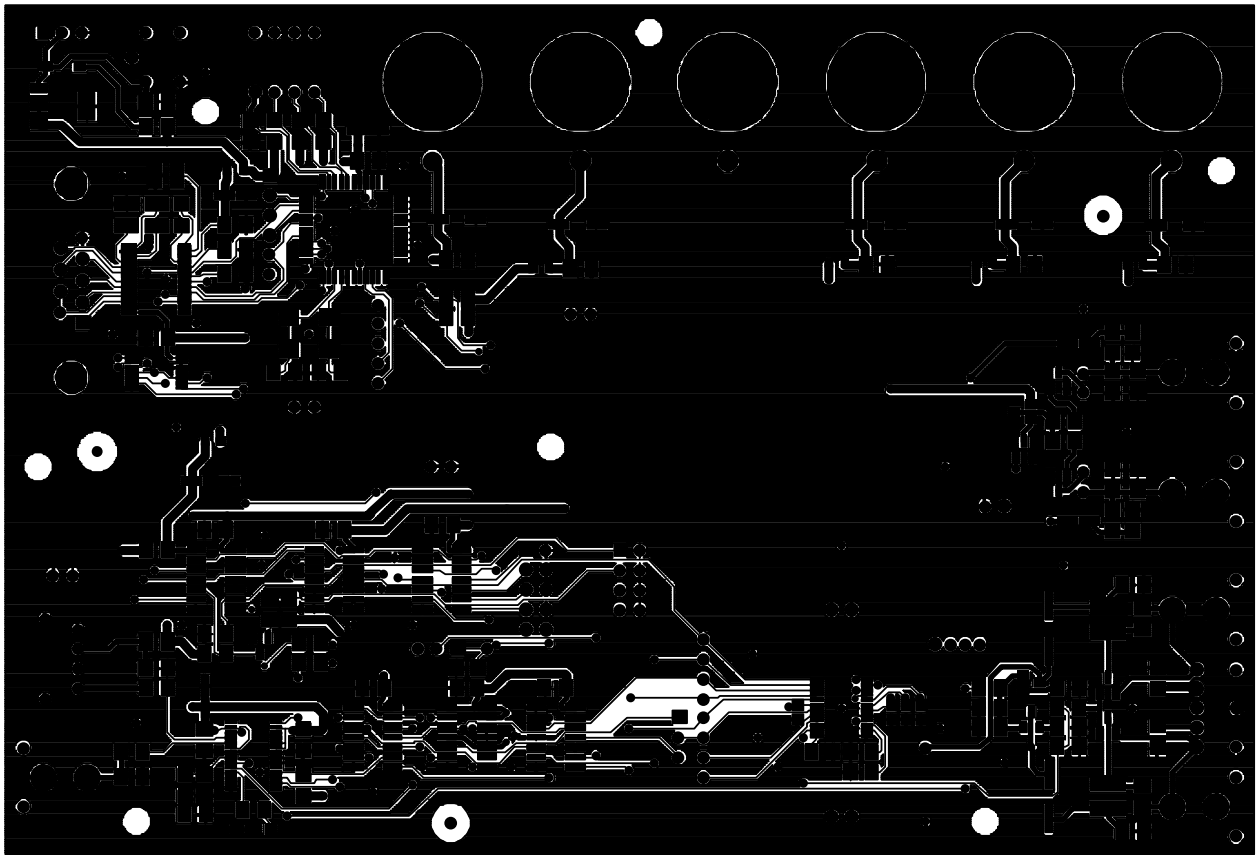


Figure 26. Silkscreen Top

CRYSTAL SEMICONDUCTOR
Customer Demonstration Board
CDB43L42A.0



TOP SIDE

Figure 27. Top Side

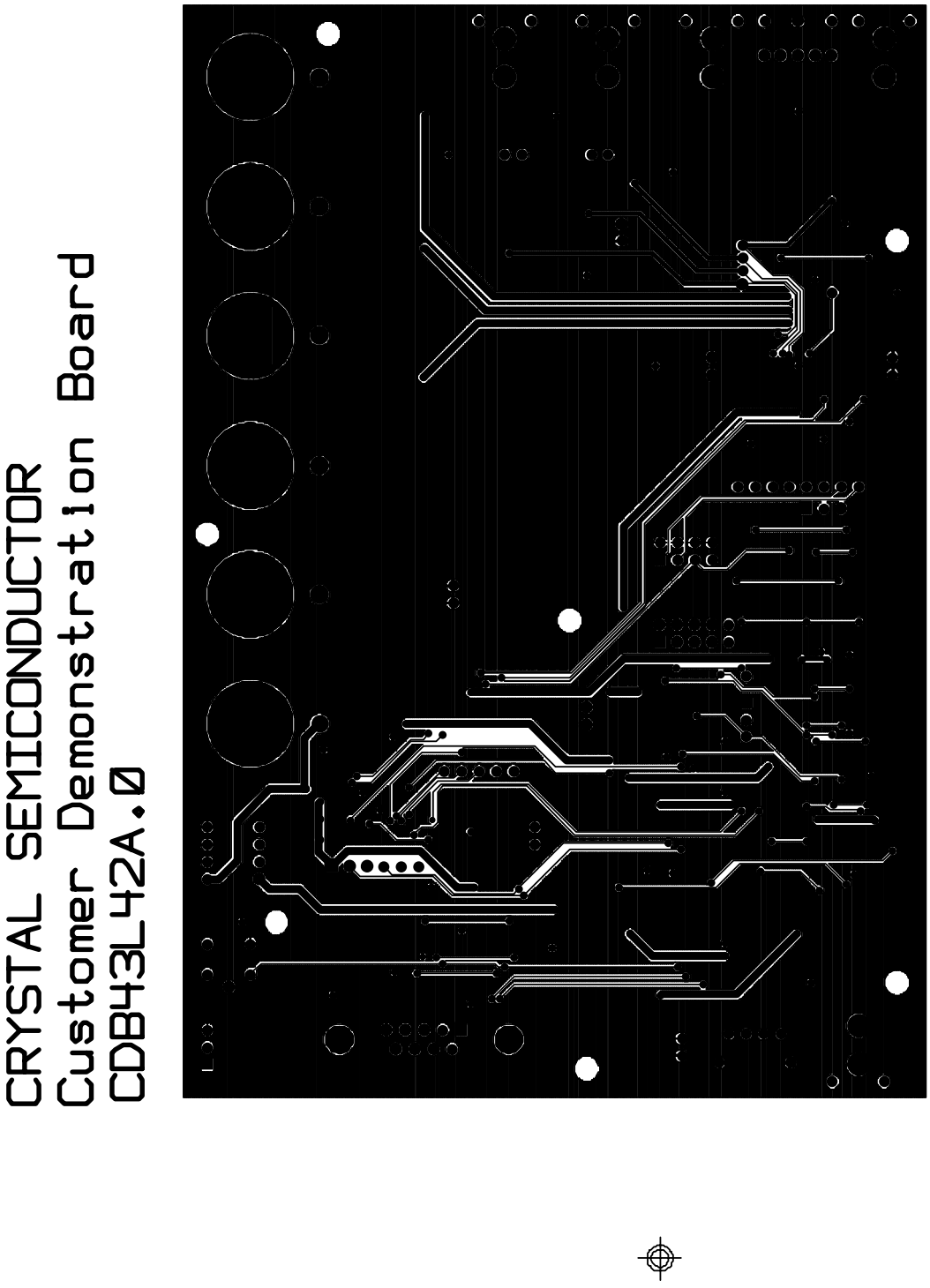


Figure 28. Bottom Side

• Notes •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