CDB5333

Evaluation Board for CS5333

Features

- Demonstrates recommended layout and grounding arrangements
- CS8404A generates AES/EBU, S/PDIF, and EIAJ-340 compatible digital audio
- Requires only an analog signal source and power supplies for a complete Analog-to-Digital-Converter system

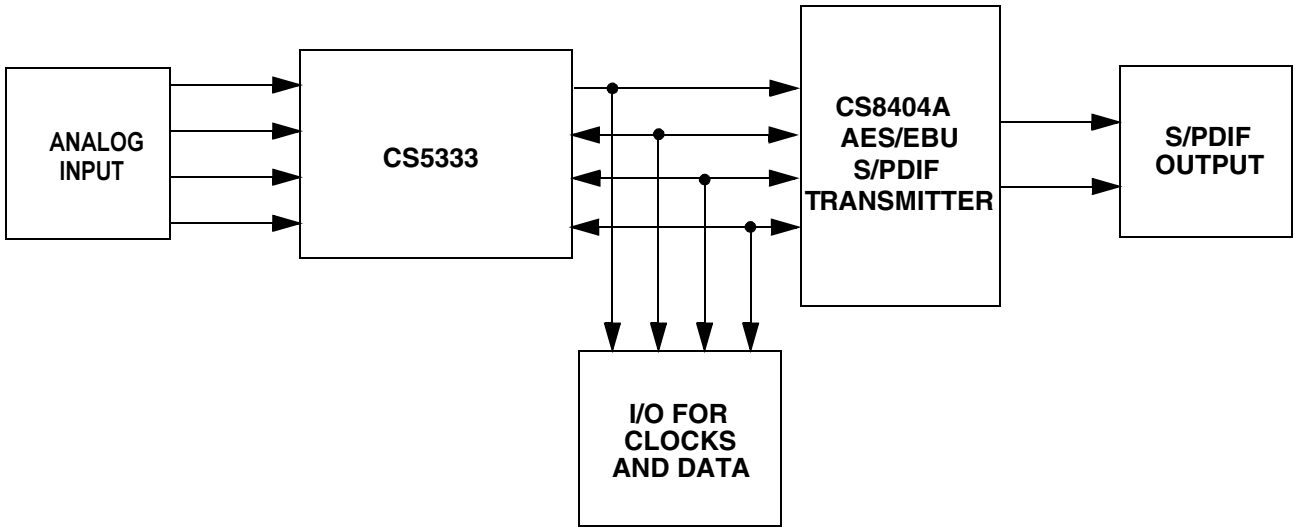
Description

The CDB5333 evaluation board is an excellent means for quickly evaluating the CS5333 24-bit, stereo A/D converter. Evaluation requires a digital signal analyzer, an analog signal source, and a power supply.

Also included is a CS8404A digital audio interface transmitter which generates AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono and optical connectors.

ORDERING INFORMATION

CDB5333	Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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http://www.cirrus.com/corporate/contacts/

1. CDB5333 SYSTEM OVERVIEW

The CDB5333 evaluation board is an excellent means of quickly evaluating the CS5333. The CS8404A digital audio interface transmitter provides an easy interface to digital audio signal analyzers including the majority of digital audio test equipment.

The CDB5333 schematic has been partitioned into 8 schematics shown in Figures 2 through 9. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the interconnections between the partitioned schematics.

2. CS5333 ANALOG TO DIGITAL CONVERTER

A description of the CS5333 is included in the CS5333 datasheet.

3. CS8404A DIGITAL AUDIO TRANSMITTER

The system generates and encodes standard S/PDIF data using a CS8404A Digital Audio Transmitter, Figure 7. The outputs of the CS8404A are RS422 compatible differential line drivers. The CS8404A data format has been configured for I2S. A description of the CS8404A is included in the CS8404A datasheet.

Note: The CS8404A can not be the clock source for the board

4. INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow interfacing to external systems via the 10-pin header, J6. The schematic for the clock/data input/output is shown in Figure 6.

The CDB5333 allows some flexibility as to the generation of the clocks. When in slave mode, the MCLK, SCLK, and LRCK must be provided via the header, J6. When operating the CS5333 in master mode, MCLK is generated from the on board oscillator, Y1. This oscillator is socketed to allow other frequency oscillators to be used.

Note: When providing MCLK externally, the on board oscillator must be removed.

5. POWER SUPPLY CIRCUITRY

Power is supplied to the evaluation board by four binding posts (GND, +5 V, VA, VL), see Figure 9. The +5 V input supplies power to the +5 V digital circuitry (+5 V) and the amplifiers (VAA_+5 V), while the two +1.8/+3.3 V inputs supply power to the VA and VL pins of the CS5333 and to the level shifter circuits.

6. GROUNDING AND POWER SUPPLY DECOUPLING

The CS5333 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 3 details the power distribution used on this board. The decoupling capacitors are located as close to the CS5333 as possible. Extensive use of ground plane fill in the evaluation board yields large reductions in radiated noise.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 V	Input	+ 5 Volt power
VA	Input	+ 1.8 to + 3.3 Volt power for the CS5333
VL	Input	+ 1.8 to +3.3 Volt power for the CS5333
GND	Input	Ground connection from power supply
Left Audio In	Input	Analog input left channel
Right Audio In	Input	Analog input right channel
Optical Output	Output	Digital audio output
Coax Output	Output	Digital audio output

Table 1. System Connections

JUMPER / SWITCH	PURPOSE	POSITION	FUNCTION SELECTED
J3	MCLK divide/Mode select	HI *LOW	Master: High Rate mode Slave: MCLK divide Master: Base Rate mode Slave: NA
J4	Data format select	HI *LOW	Left Justified, up to 24-bit data I2S, up to 24-bit data
J5	MCLK divider for the CS8404A	DIV1 *DIV2 DIV4	MCLK goes straight to CS8404A MCLK divided by two prior to CS8404A MCLK divided by four prior to CS8404A
J7	Master/Slave select for CS5333	*HI LOW	CS5333 in Master mode CS5333 in Slave mode
J6	Input/Output for clocks/data	-	-
S1	Reset for the CDB5333	-	-

Notes: * denotes default factory settings

Table 2. CDB5333 Jumper and Switch Settings

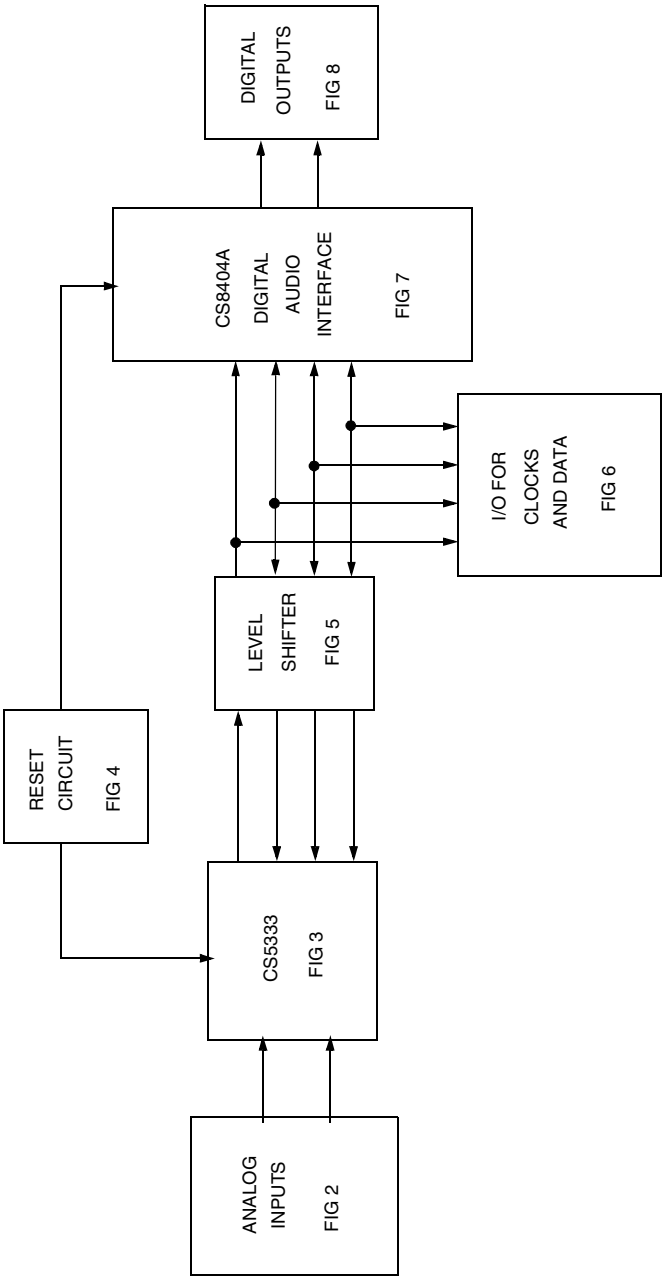

Figure 1. System Block Diagram and Signal Flow

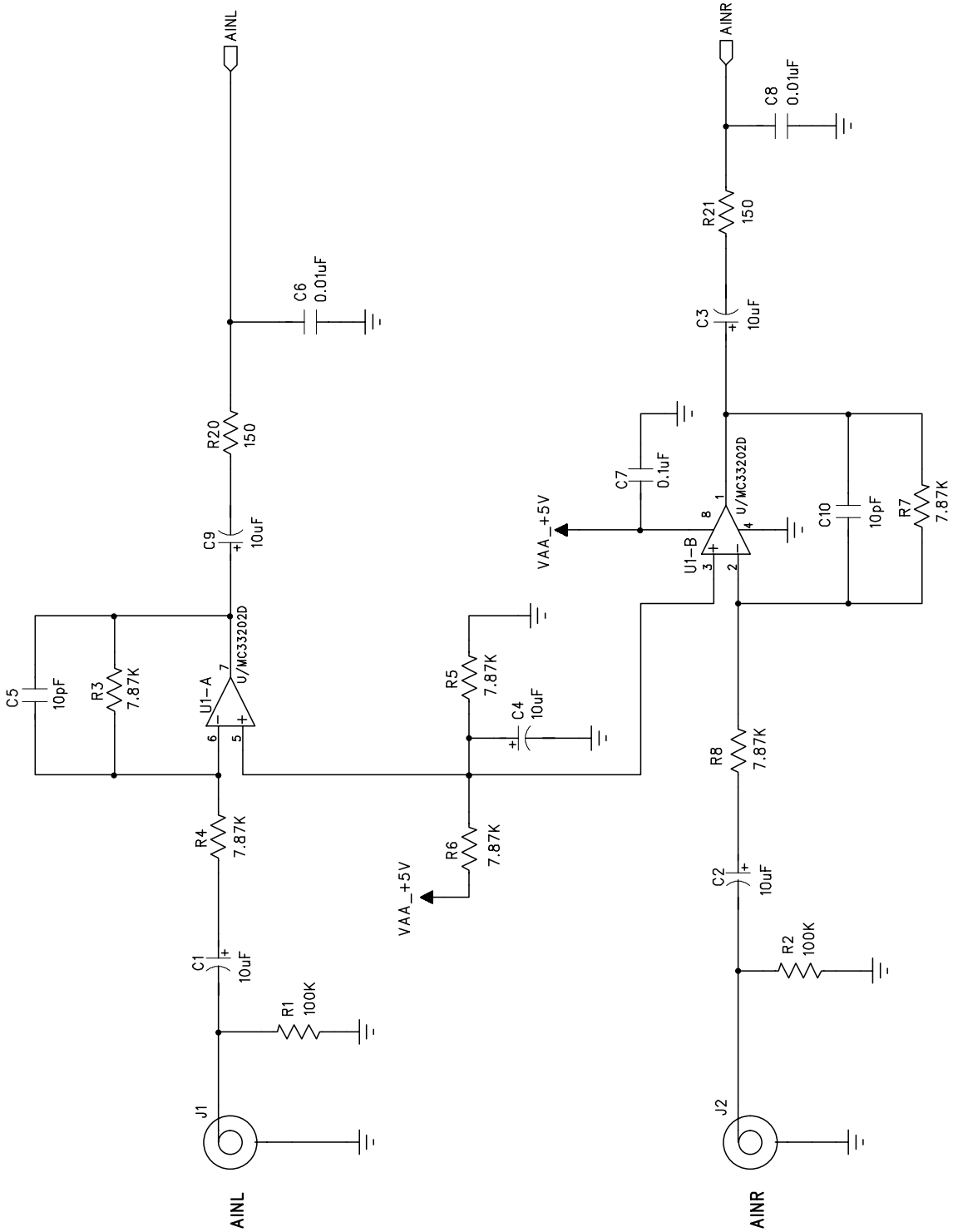

Figure 2. Analog Audio Input

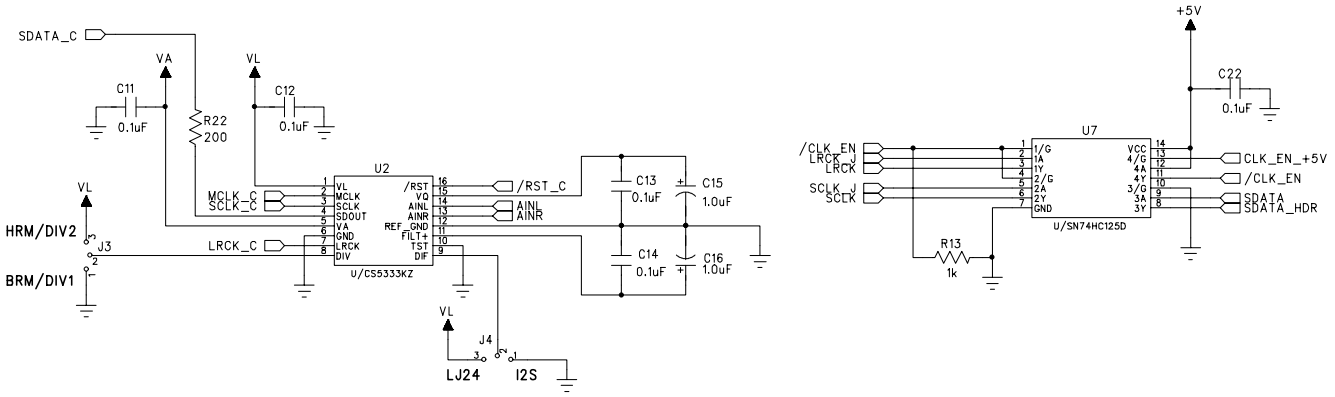

Figure 3. CS5333

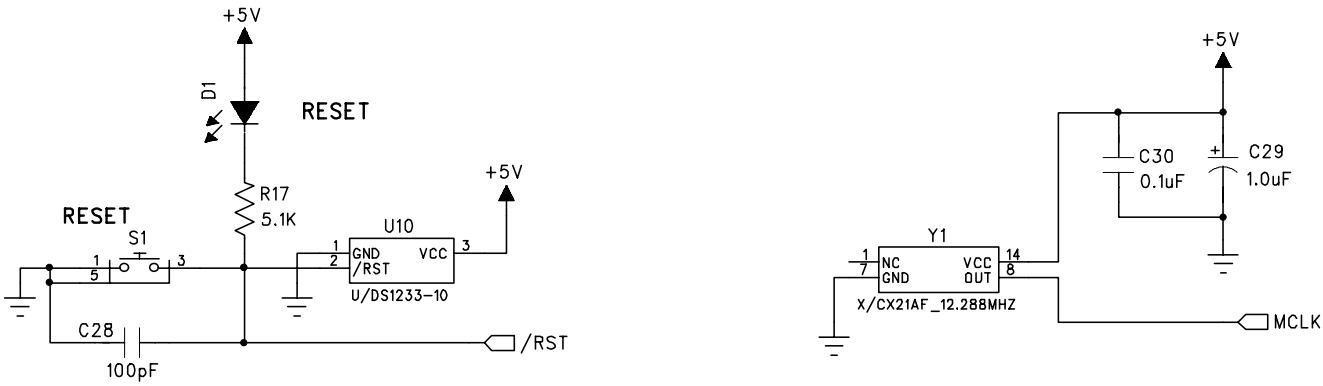

Figure 4. Reset Circuit

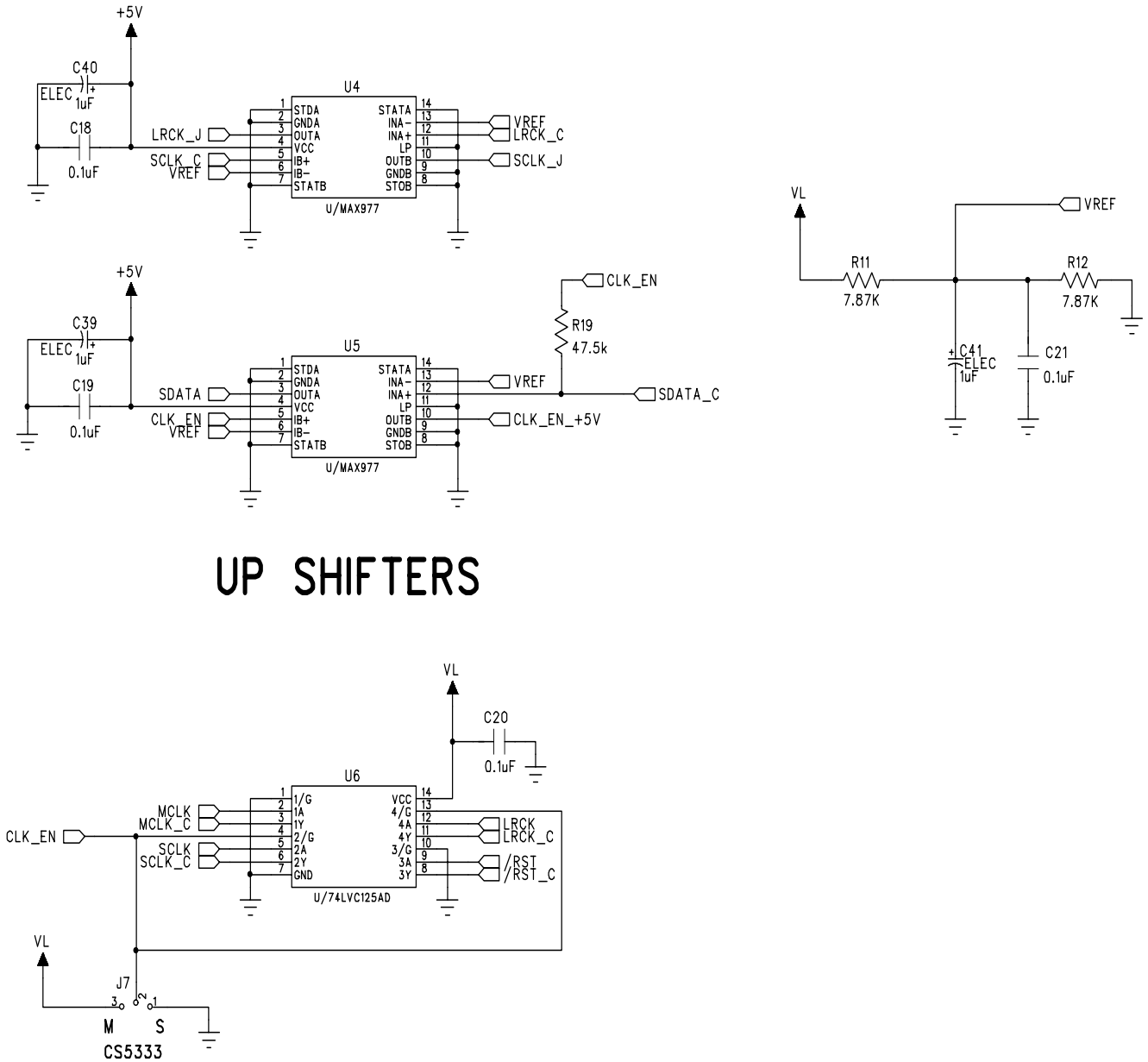

Figure 5. Level Shifters

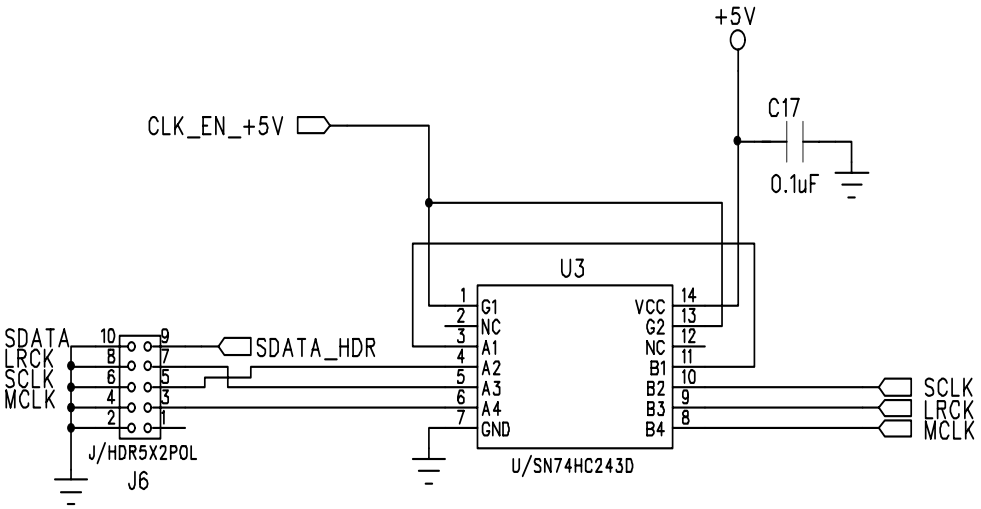

Figure 6. I/O for Clocks/Data

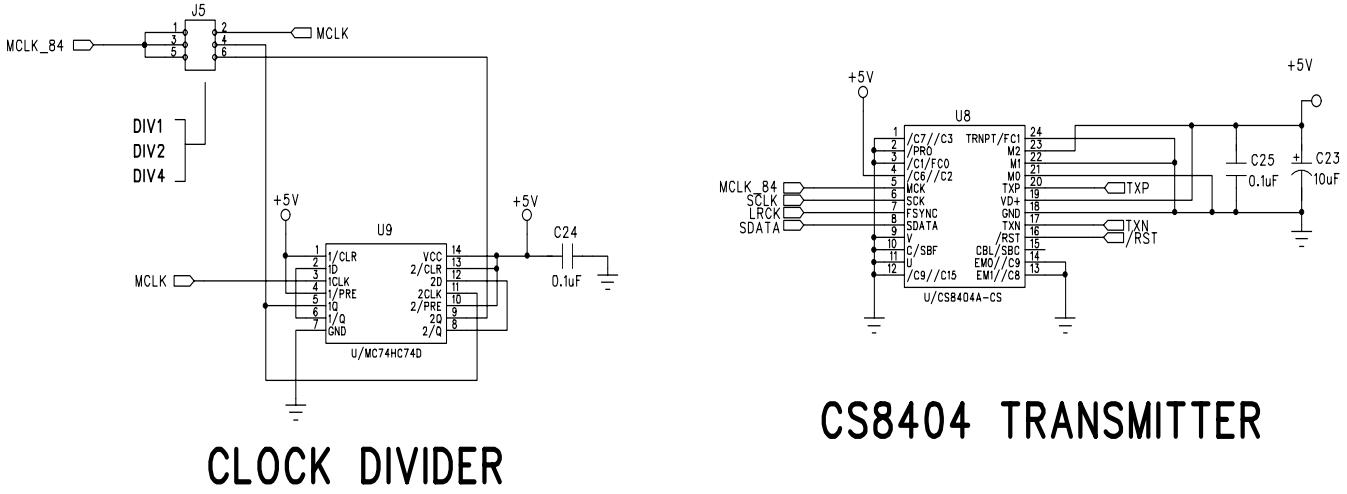

Figure 7. CS8404A Digital Audio Interface

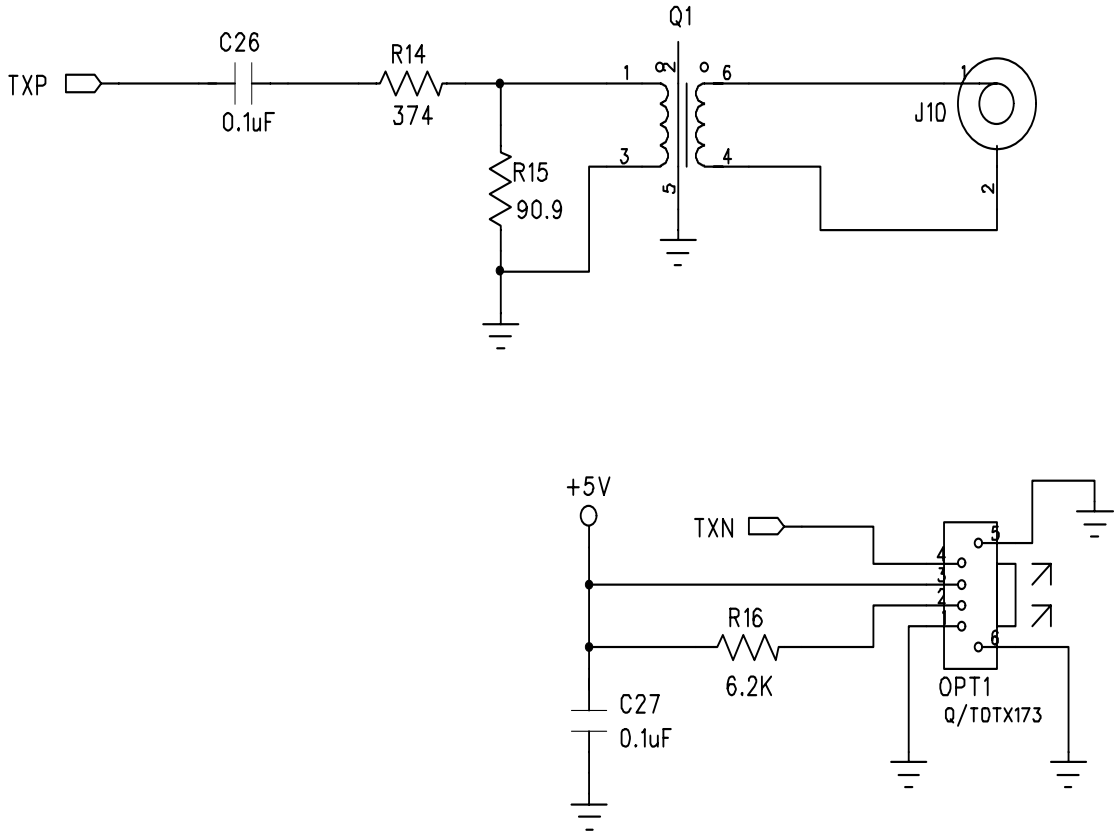

Figure 8. Digital Audio Output

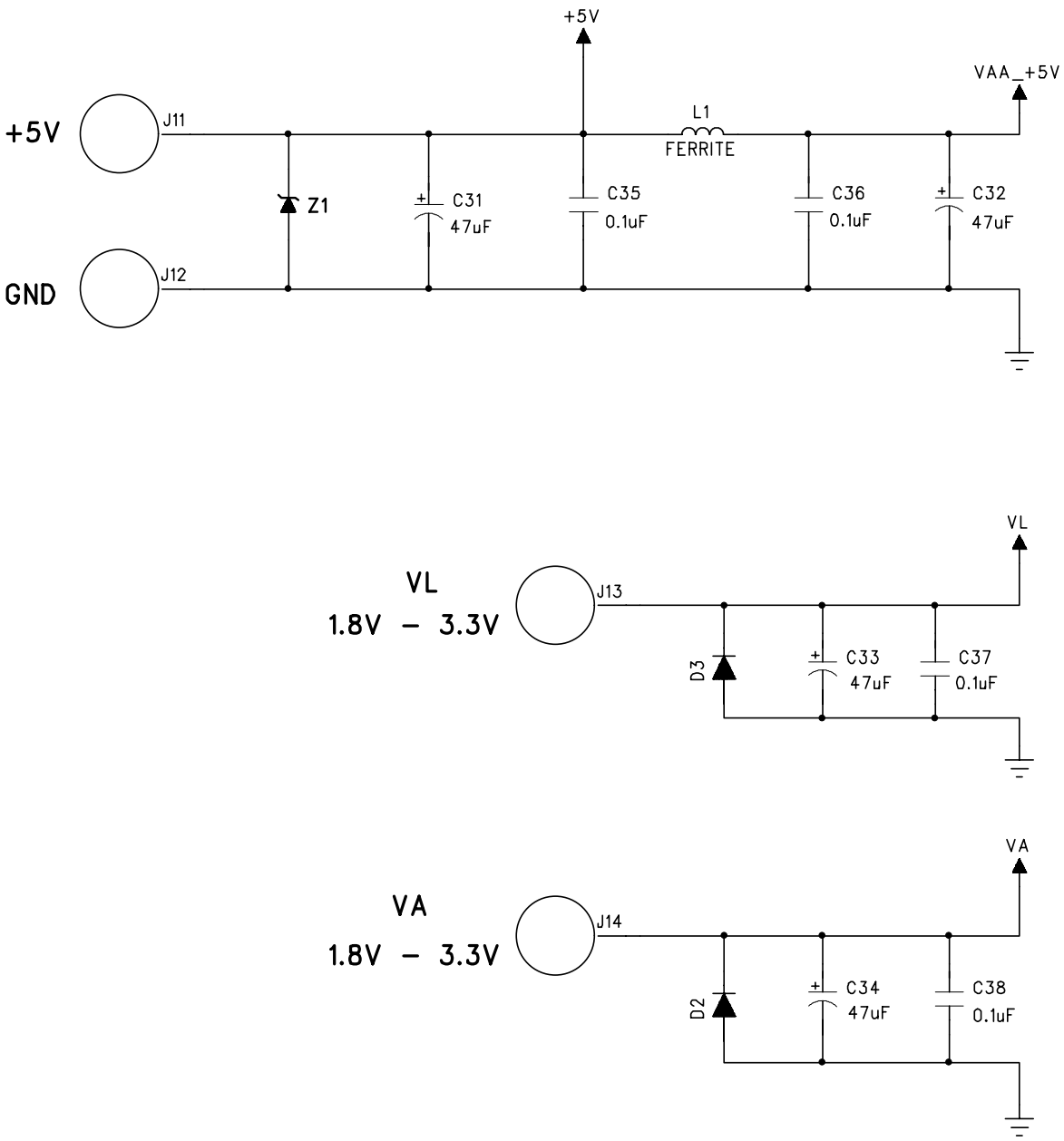

Figure 9. Power Circuit

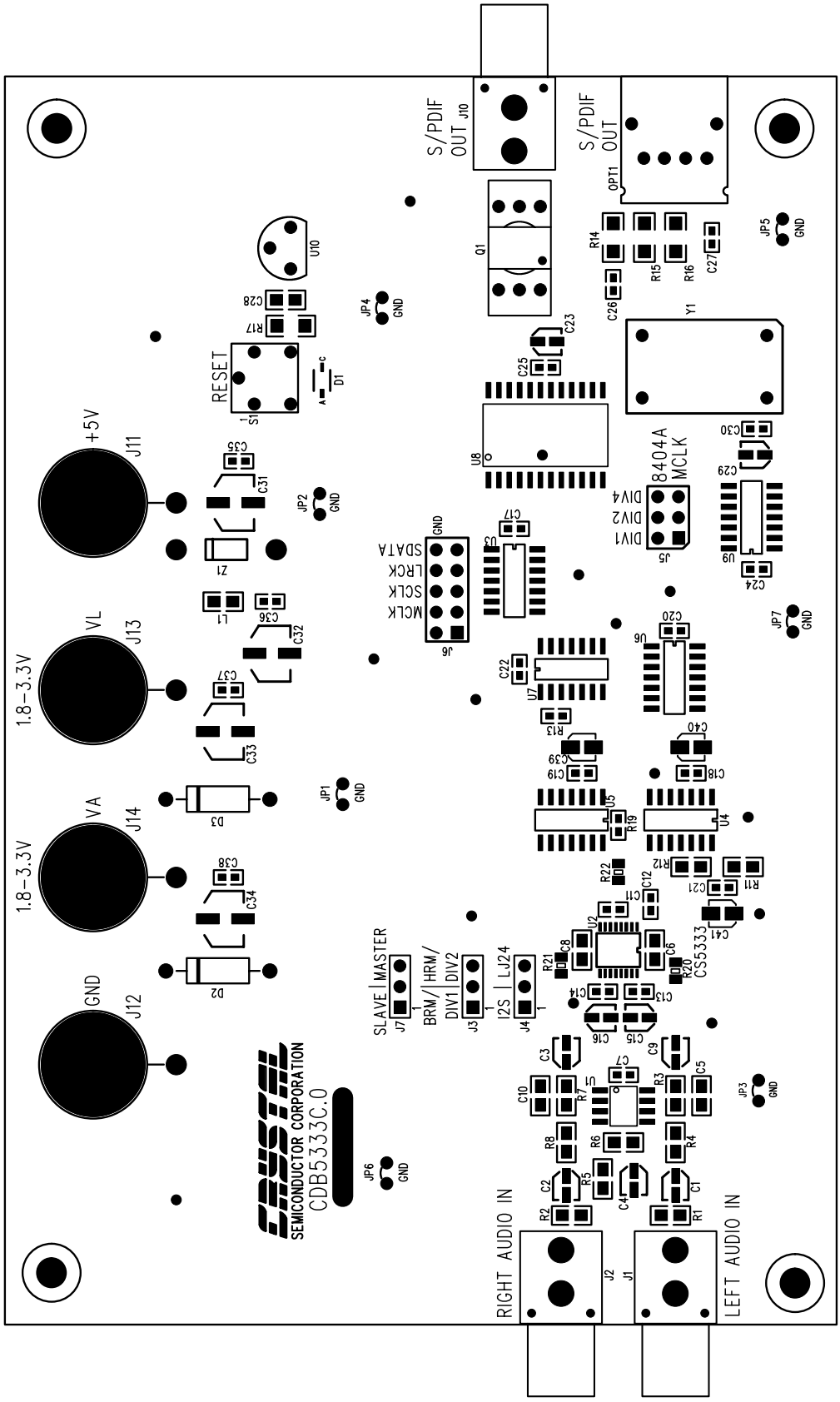

Figure 10. Top Layer Silkscreen

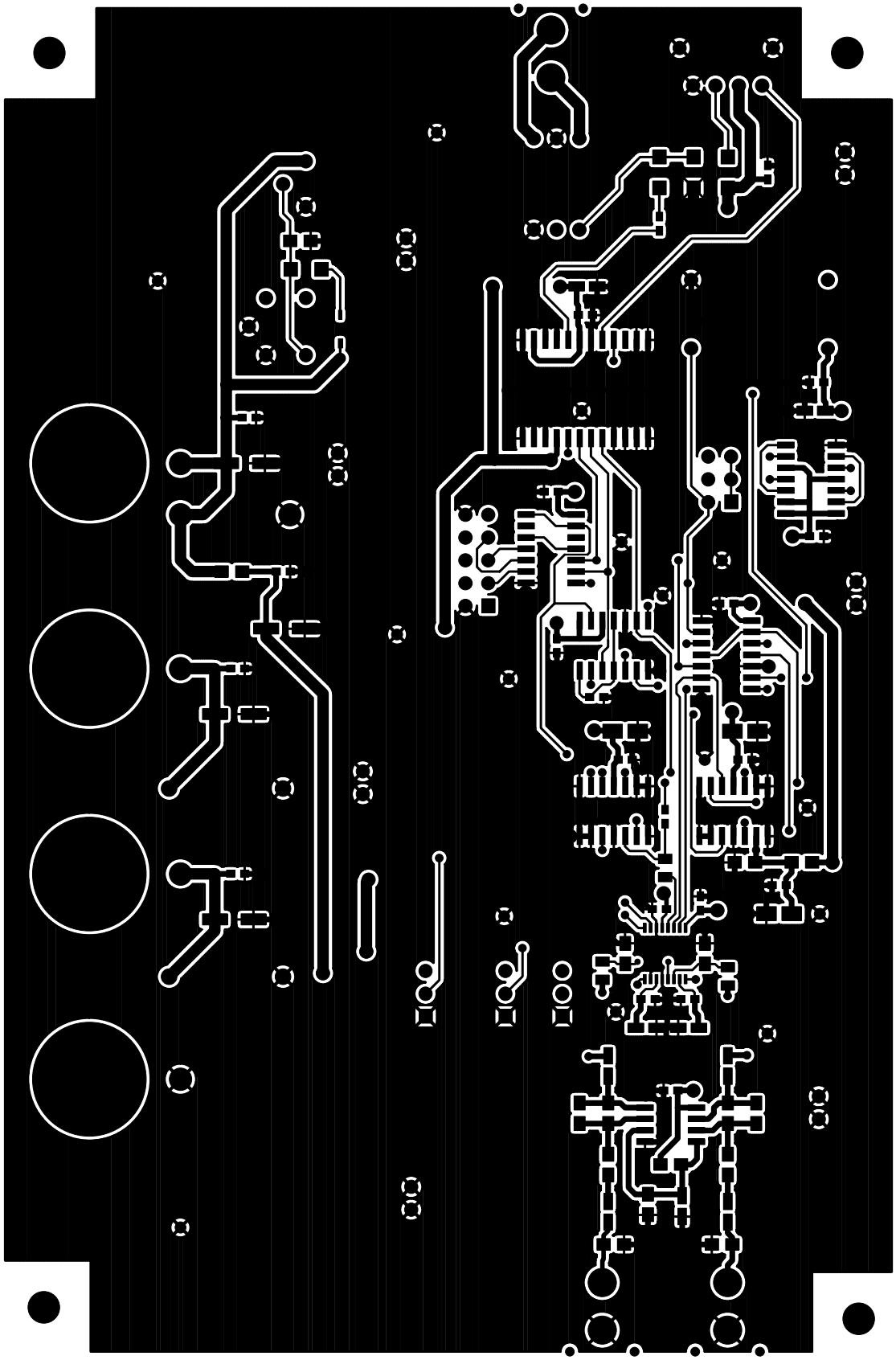

Figure 11. Top Layer

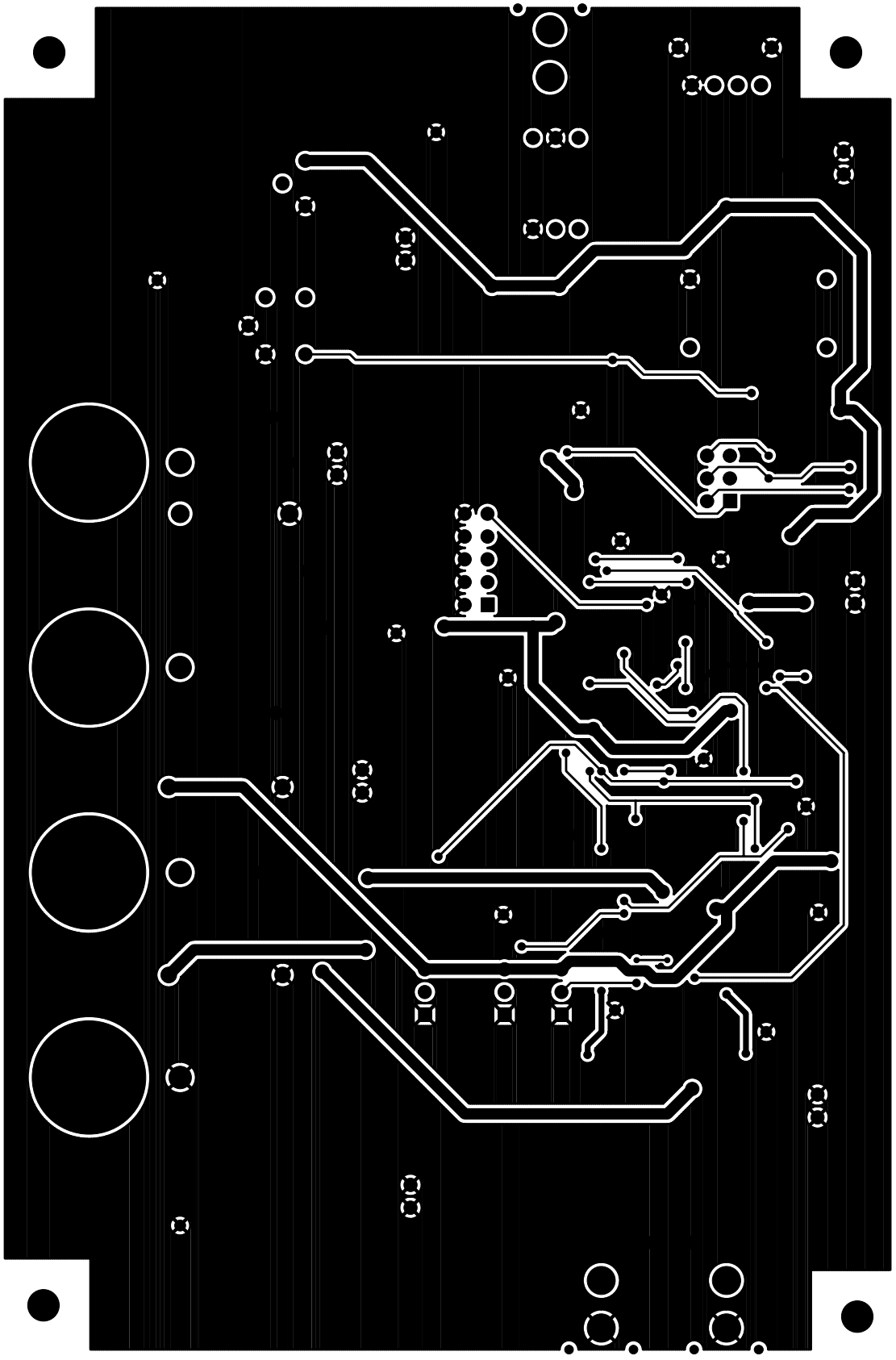

Figure 12. Bottom Layer

• Notes •


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