CDB5540
CDB5541

CDB5540/41 Evaluation Board and Software

Features

- RS-232 Serial Communication with PC
- On-board Microcontroller
- On-board Voltage Reference
- LabWindows®/CVI® Evaluation Software
  - Chip Control and Data Capture
  - FFT Analysis
  - Time Domain Analysis
  - Noise Histogram Analysis
- Supports the CS5540 and CS5541 16-pin ADCs

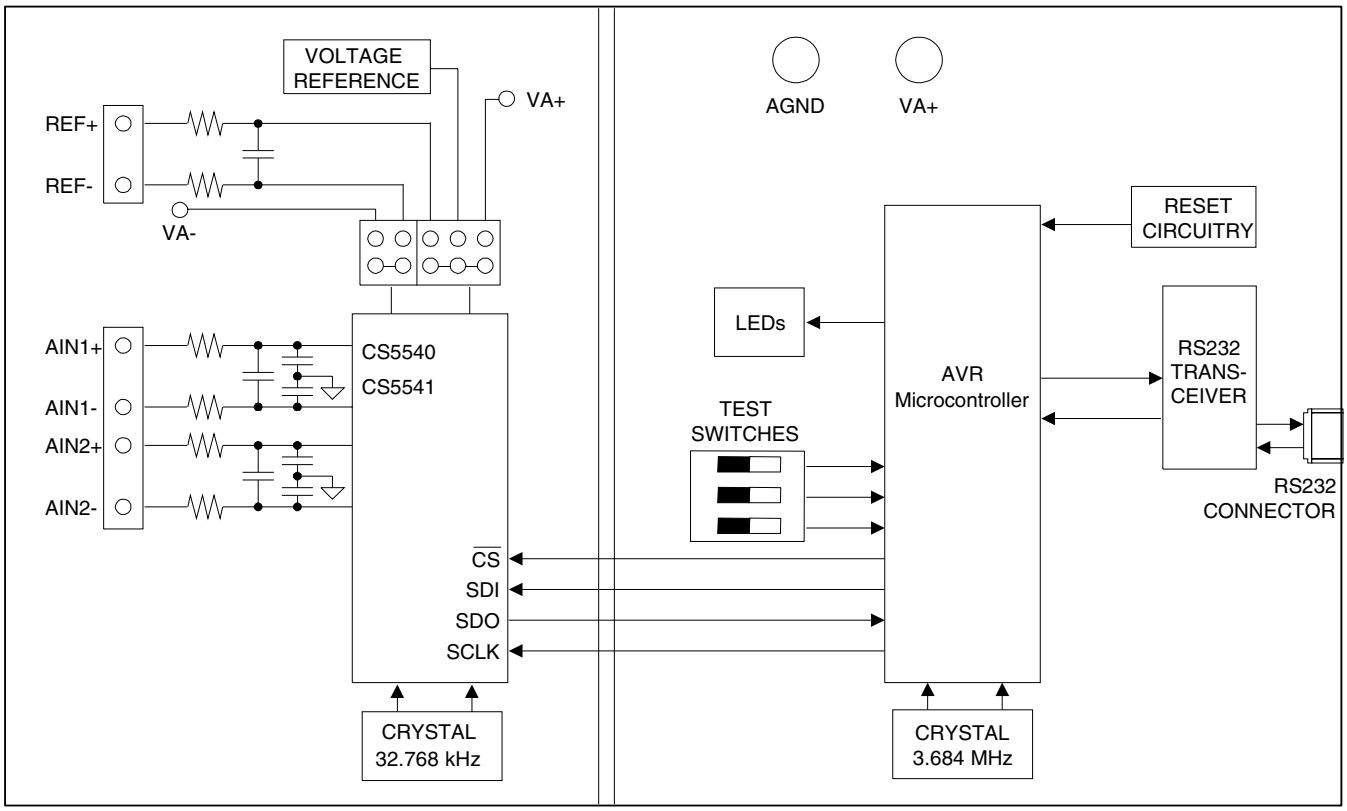
General Description

The CDB5540/41 is an inexpensive tool designed to evaluate the performance of the CS5540/41 16-pin Analog to Digital Converters. This document, as well as the CS5540 or CS5541 data sheet should be read thoroughly before using the CDB5540/41 Evaluation System.

The evaluation system consists of a CDB5540/41 Board and PC software which allows the user to easily capture and analyze data. The provided analysis functions in the software include Time Domain Analysis, Histogram Analysis, and Frequency Domain Analysis.

ORDERING INFORMATION:

CDB5540	Evaluation System
CDB5541	Evaluation System



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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http://www.cirrus.com/corporate/contacts/sales/cfm

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1. HARDWARE

1.1 Introduction

The CDB5540 and CDB5541 evaluation systems provide a quick means of testing the CS5540 and CS5541 Analog-to-Digital Converters (ADCs). The CS5540/41 are low-power, low-voltage Δ–Σ analog-to-digital converters (ADC), targeted at temperature and pressure measurement, and various portable devices where low power consumption is required.

The CDB5540/41 evaluation boards are equipped with either a CS5540 or a CS5541 and interfaces directly to a PC though an RS-232 serial interface.

The included analysis software allows the user to control the various functions of the CS5540/41, as well as capture and save data. The software also provides data analysis tools to display the time domain, frequency domain, and noise histogram performance for a captured set of data.

1.2 Evaluation Board Overview

The evaluation board is partitioned into two main sections: analog and digital. The analog section consists of the ADC and a voltage reference. The digital section consists of the AVR microcontroller, the hardware test switches, the reset circuitry and the RS-232 interface.

The evaluation board's analog and digital sections operate from a single +3.0 V power supply and interface to an IBM® compatible PC through the RS-232 interface. The board comes equipped with an AVR microcontroller and a 9-pin RS-232 cable which physically interfaces the evaluation board to the PC. The software provides a means to display and evaluate the performance of the ADC in the time or frequency domains.

The evaluation board supports a single supply configuration. The AGND post should be connected to 0 V, and the VA+ post should be connected to 3.0 V. HDR14 is populated such that VA+ powers VCC, the board logic supply voltage, and VD+, the digital ADC supply voltage. HDR13 is populated such that AGND, the analog ADC ground, is directly connected to DGND, GND1, and VA- (the digital ADC ground, board logic ground, and VA- of the ADC, respectively). All of this is represented in Figure 7, which depicts the power supply configuration.

Figures 11-13 show layout plots of the evaluation board, with the ground planes removed, so that signal traces may be seen easier. This can serve as an aid when designing a board.

1.2.1 Analog Section

The evaluation board runs at 32.768 kHz. However, by configuring HDR2, a variable clock may be provided from either the microcontroller or from an external source connected to the XOSC connector on J5. Analog input signals can be connected to the converter via connectors J2 (CH 1) and J12 (CH 2). Note that a simple RC network filters the input to reduce broadband noise.

The evaluation system provides three voltage reference options: the on-board 2.5V reference, the power supply voltage, or an external voltage reference source, as shown in Table 2. When using an external reference, the signal must be connected to XREF+ and XREF- on connector J3.

A schematic of the ADC and the components directly around it, are depicted in Figure 8. A schematic representation of the voltage reference circuit, as well as the external signal connectors, is portrayed in Figure 9.

1.2.2 Digital Section

Figure 10 represents the schematic of the digital section of the evaluation board. It contains the microcontroller, test switches, and an RS-232 interface IC. The test switches aid in debugging communication problems between the board and the PC. The microcontroller, which derives its clock from a 3.684 MHz crystal, is initially config-

ured to communicate via RS-232 at 19200 baud, no parity, 8-bit data, and 1 stop bit. The baud rate can be changed with software to go as fast as 38400 baud.

The microcontroller can be reset by depressing pushbutton switch S1. On reset or upon power-up, the LED's on the board will count down, until only LED4 remains lit. This LED is the POWER LED, and informs the user that the board is powered on.

LED1, the BUSY LED, lights when the microcontroller is busy performing an operation. It is normal for the LED to turn on and off, and is useful when collecting large data sets.

1.2.3 Serial Interface

The CS5540/41 serial interface is *SPI*® and *MICROWIRE*™ compatible. The interface control lines ($\overline{CS}$, SDO, and SCLK) are connected to the AVR microcontroller on the CDB5540/41.

1.2.4 Clock Source Options

The evaluation board provides three sources for the master clock: the on-board crystal, the microcontroller, and an external clock signal.

1) The 32.768 kHz crystal oscillator can be chosen by selecting the "Crystal Oscillator - 32.768 kHz" option in the software. HDR2 on the evaluation board should be set according to Table 3.

2) The microcontroller can be used to generate a clock for the ADC. The microcontroller's clock can be chosen by selecting the "Microcontroller" option in the software. HDR2 on the evaluation board should be set according to Table 3.

The clock frequency can be selected by changing the "Oscillator Frequency" box in the software. Note that the frequency options are limited by the microcontroller's counter/timer circuitry, which divides the 3.6864 MHz clock by integer values to produce the clock output.

3) An external clock can be provided by the user, and connected to the XOSC post on J5. The "External Clock Source" option in the software should be selected when using an external clock source, and HDR2 on the evaluation board should be set according to Table 3.

1.2.5 Headers, Jumpers, and DIP Switches

Table 1 describes the headers and DIP switches on the evaluation board, with their appropriate default settings.

Table 2 describes the various jumper settings for HDR11 and HDR9, which select the voltage reference that is used.

HDR2 selects the MCLK source that is used. Jumper settings are depicted in Table 3.

DIP switch SW1 is used to control the AVR modes and Table 4 illustrates the various modes it can be set to. When testing the RS-232 link in the PC software, the DIP switches should all be in the CLOSED position.

Configurations other than those specified are not recommended.

Name	Functional Description	Default Setting	Default Jumpers
HDR1.	Tests UART/RS-232 communication link between the microcontroller and the PC.	RS-232 set to Normal Mode.	
HDR2.	Selects MCLK source.	32.768 kHz Crystal	XTAL ●—● MCLK uC O O MCLK XOSC O O MCLK
HDR9.	Selects VREF-.	On-Board Reference.	XREF- O O VREF- VA- O O VREF- VA+ O O VREF- REF- ●—● VREF-
HDR11.	Selects VREF+.	On-Board Reference.	XREF+ O O VREF+ VA- O O VREF+ VA+ O O VREF+ REF+ ●—● VREF+
SW1.	Controls AVR modes.	CS5540	SW1, SW2, SW3 - OPEN
.		CS5541	SW1, SW3 - OPEN SW2 - CLOSED

Table 1. Default Header and DIP Switch Settings

Reference	Description	HDR11	HDR9
REF.	Selects On-Board Reference	XREF+ O O VREF+ VA- O O VREF+ VA+ O O VREF+ REF+ ●—● VREF+	XREF- O O VREF- VA- O O VREF- VA+ O O VREF- REF- ●—● VREF-
Supply.	Selects Power Supply Voltage	XREF+ O O VREF+ VA- O O VREF+ VA+ ●—● VREF+ REF+ O O VREF+	XREF- O O VREF- VA- ●—● VREF- VA+ O O VREF- REF- O O VREF-
XREF.	Selects External Reference	XREF+ ●—● VREF+ VA- O O VREF+ VA+ O O VREF+ REF+ O O VREF+	XREF- ●—● VREF- VA- O O VREF- VA+ O O VREF- REF- O O VREF-

Table 2. Voltage Reference Settings

Reference	Description	HDR2
XTAL.	Selects On-Board Crystal	MCLK ●—● XTAL MCLK O O uC MCLK O O XOSC
uC.	Selects Micro-controller Clock	MCLK O O XTAL MCLK ●—● uC MCLK O O XOSC
XOSC.	Selects External MCLK	MCLK O O XTAL MCLK O O uC MCLK ●—● XOSC

Table 3. MCLK Settings

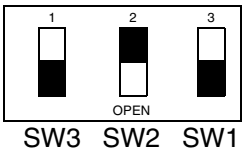
Eval Board Mode	SW1 Settings
CS5540 SW1 is OPEN SW2 is OPEN SW3 is OPEN	
CS5541 SW1 is OPEN SW2 is CLOSED SW3 is OPEN	
RS-232 Test Mode SW1 is CLOSED SW2 is CLOSED SW3 is CLOSED	

Table 4. DIP Switch SW1 Settings

2. SOFTWARE

The evaluation system comes with software and an RS-232 cable to link the evaluation board to the PC. The executable software was developed with LabWindows/CVI and meant to run under Windows 95® or later. After installing the software, read the readme.txt file for any last minute changes in the software.

2.1 Installation Procedure

1) Turn on the PC, running Windows 95 or 98.
2) Insert the Installation Diskette #1 into the PC.
3) Select the Run option from the Start menu.
4) At the prompt, type: A:\SETUP.EXE <enter>.
5) The program will begin installation.
6) If it has not already been installed on the PC, the user will be prompted to enter the directory in which to install the CVI Run-Time Engine. The Run-Time Engine manages executables created with LabWindows/CVI. If the default directory is acceptable, select OK and the Run-Time Engine will be installed there.
7) After the Run-Time Engine is installed, the user is prompted to enter the directory in which to install the Eval5540/41 software. Select OK to accept the default directory, or choose an alternate directory.
8) Once the program is installed, it can be run by double clicking on the Eval5540/41 icon, or through the Start menu.

Note: *The software is written to run with 640 x 480 resolution; however, it will work with 1024 x 768 resolution. If the user interface seems to be a little small, the user might consider setting the display settings to 640 x 480. (640 x 480 was chosen to accommodate a variety of computers).*

2.2 Using the Software

At start-up, the title screen appears first (Figure 1). This window contains information concerning the software's title, revision number, copyright date, etc. Additionally, at the top of the screen is a menu bar which displays user options. Notice, the menu bar item *Window* is initially disabled. This eliminates any conflicts with the mouse or concurrent use of modems. Before proceeding any further, the user is prompted to select the serial communication port.

2.2.1 Selecting the COM Port and Part

To initialize a port, pull down option *ComPorts* from the menu bar and select either COM1 or COM2. Next, the user is prompted to select the appropriate part under the *Parts* menu. After a port is initialized and the correct part is selected, it is a good idea to test the RS-232 link between the PC and the evaluation board. To do this, pull down the *Setup* menu from the menu bar and select the option TEST RS232. The user is then prompted to set all the evaluation board's test switches to the CLOSED position and then reset the board. Once this is done, proceed with the test. If the test fails, check the hardware connection and repeat again. Otherwise, set the test switches back to the correct mode as specified in this document, and press reset again.

If the user wishes to change the speed of communications between the PC and the microcontroller, this can be achieved through the BAUD RATE option.

2.2.2 Setup Window Functions

To make sure that the software and evaluation board are set up correctly, it is recommended that the user proceed to the Setup Window and test the functionality of the part before proceeding (Figure 2). To access the Setup Window, the user can pull down the Window menu item, or press F1 on the keyboard. The following describes the various options and indicators in the Setup Window.

Clock Source: This pull-down menu allows the user to select the type of clock that will be used

with the ADC, so that the software knows what to expect from the microcontroller. Selecting from this menu also gives the user a warning to examine the jumper settings on HDR2 of the evaluation board. There are three options available on this menu:

On-board Crystal Oscillator - 32 kHz - This option tells the software that the master clock for the ADC is coming from the on-board 32.768 kHz crystal. This option is selected by default.

Microcontroller - This option tells the software that the microcontroller will provide the ADC with a master clock. The microcontroller's clock frequency is user-selectable from the Setup Window. The clock frequency is limited to integer sub-multiples of the microcontroller's 3.6864 MHz master clock (3.6864 MHz / N). Be sure that the jumper is set properly on HDR2 when this option is selected.

External Clock Source - This option tells the software that the master clock for the ADC will be coming from an outside source. The clock source should be connected to the XOSC post on J5.

Oscillator Frequency: This box displays the frequency of the oscillator that the ADC is running on. When using an external clock source, the user can type in the frequency of the clock source, and the FFT plots will scale accordingly. When using the microcontroller as a clock source, the user should adjust this value until it is close to the desired frequency. The value in this box will automatically be adjusted to a frequency that the microcontroller can provide.

Power-down Mode: This pull-down menu allows the user to put the ADC in sleep or standby mode. The ADC will power down according to the data sheet specifications.

SPI Init: This button issues an SPI Initialization command to the CS5541.

Command Word Components

Channel Select: This pull-down menu allows the user to select which channel the ADC will convert. In the CS5541, this affects the command word. Default selection is "AIN1+/-".

Unipolar/Bipolar: This pull-down menu controls whether unipolar or bipolar mode is used. In the CS5541, this affects the command word. Default selection is "Bipolar".

Filter Select: This pull-down menu controls which digital filter is used for the CS5541. In the CS5541, this affects the command word. Default selection is "Four Cycle Settling - 53.7 Hz".

Conversion Calibration Select: This pull-down menu controls which calibration mode is used in the CS5541. In the CS5541, this affects the command word. Default selection is "One-Time Calibration".

Command Word: This box displays the command word that is sent to the CS5541. For more information on the command word and command word format refer to the CS5541 data sheet.

Sampling Frequency: This box displays the computed sampling frequency for the specified oscillator frequency. This number is used when performing FFT analysis.

2.3 Data Collection Window Overview

The Data Collection Window is used to collect and analyze data sets using the evaluation board. The software supports Time Domain, Frequency Domain (FFT) and Histogram analysis of collected data sets. To go to the Data Collection Window, pull down the *Window* menu item and select "Data Collection Window", or press F2 on the keyboard. The following controls and indicators are present in the Data Collection Window regardless of what test is being performed.

COLLECT: Initiates the data conversion collection process. COLLECT has two modes of opera-

tion: collect from file or collect from converter. To collect from a file, a previously saved file from the ComPorts->DISK menu bar option must be selected. Once a file is selected, its content will displayed on the graph when the COLLECT button is pressed. If the user is collecting conversions from the evaluation board to analyze, the appropriate COM port must be selected. The user is then free to collect the preset number of conversions (preset by the CONFIG pop-up menu discussed below). Notice, there is a significant acquisition time difference between collecting from a file and collecting from the evaluation board. Data can only be collected from the evaluation board at the converter's current sampling frequency, and will take much longer than retrieving previously collected data from a file.

CANCEL: This button allows the user to exit from the COLLECT algorithm during a collection. It is recommended that the user reset the evaluation board after pressing this button, so that the evaluation board will stop collecting data and wait for the next command.

OUTPUT: This button calls up a pop-up window which allows the user to save the collected data set to a file or print out the information on the screen. Two printing options are available: printing only the plot data, and printing the entire screen including the calculated statistics for the current analysis mode.

ZOOM: Pressing this button allows the user to zoom in on a specific portion of the current graph. To zoom, click on the ZOOM icon, then click on the graph to select one corner of the desired Zoom area. When prompted, click on the graph again to select the opposite corner of the desired zoom area. Once an area has been zoomed to, the printing functions can be used to print a hard copy of that region. Click on RESTORE when done with the zoom function to display the entire data set graph. A region can also be magnified further by clicking on the ZOOM button again.

RESTORE: Restores the display of the graph after zoom has been entered. No matter how far in the user has magnified the data plot, the RESTORE button will return to the fully zoomed-out data plot.

TIME DOMAIN / FFT / HISTOGRAM Selector: This pull-down menu selects between time domain, frequency domain, and histogram mode to perform and display the appropriate analysis of the data set.

CONFIG: Opens a pop-up panel (Figure 4) to configure how much data is to be collected, and how to process the data once it is collected. The following are controls and indicators associated with the CONFIG panel.

SAMPLES: Allows the user to select the number of conversions to collect, between 16 and 32,768.

WINDOW: Used in the Power Spectrum Window to calculate the FFT. Windowing algorithms include the Blackman, Blackman-Harris, Hanning, 5-term Hodie, and 7-term Hodie. The 5-term Hodie and 7-term Hodie are windowing algorithms developed at Cirrus Logic. If information concerning these algorithms is needed, call technical support.

AVERAGE: Sets the number of consecutive FFT's to perform and average.

LIMITED NOISE BANDWIDTH: Limits the amount of noise in the converters bandwidth. Default is 0 Hz.

OK: Accept the changes and close the window

2.3.1 Histogram Plots

The following is a description of the indicators associated with Histogram analysis (Figure 6).

BIN: Displays the x-axis value of the cursor on the Histogram. This represents the output code from the part.

MAGNITUDE: Displays the y-axis value of the cursor on the Histogram. This represents the num-

ber of times a certain output code occurred in the collected data set.

MAXIMUM: Indicator for the maximum value of the collected data set.

MEAN: Indicator for the mean (average) of the data sample set.

MINIMUM: Indicator for the minimum value of the collected data set.

STD. DEV.: Indicator for the Standard Deviation of the collected data set.

VARIANCE: Indicates the Variance for the current data set.

2.3.2 Frequency Domain (FFT) Plots

The following describe the indicators associated with Frequency Domain (FFT) analysis (Figure 3).

FREQUENCY: Displays the x-axis value of the cursor on the FFT display. This represents the center frequency of the currently selected bin in Hz.

MAGNITUDE: Displays the y-axis value of the cursor on the FFT display. This represents the total power in dB contained in the selected bin.

S/D: Indicator for the Signal-to-Distortion Ratio, in dB. This is the ratio of the signal magnitude to the magnitude of the first four harmonics.

S/N+D: Indicator for the Signal-to-Noise + Distortion Ratio in dB. This is the ratio of the signal magnitude to the magnitude of the first four harmonics and the noise.

SNR: Indicator for the Signal-to-Noise Ratio in dB. This is the ratio of the signal magnitude to the magnitude of the noise (an average noise value is included in place of the first four harmonics).

S/PN: Indicator for the Signal-to-Peak Noise Ratio in dB. This is the ratio of the signal magnitude to the magnitude of the highest noise component not included in the harmonics of the signal.

# of AVG: Displays the number of FFT's averaged in the current display.

2.3.3 Time Domain Plots

The following indicators are associated with Time Domain analysis (Figure 5).

COUNT: Displays current x-position of the cursor on the time domain display. This represents the position of the code within the collected sample set.

MAGNITUDE: Displays current y-position of the cursor on the time domain display. This represents the actual code from the converter.

MAXIMUM: Indicator for the maximum value of the collected data set.

MINIMUM: Indicator for the minimum value of the collected data set.

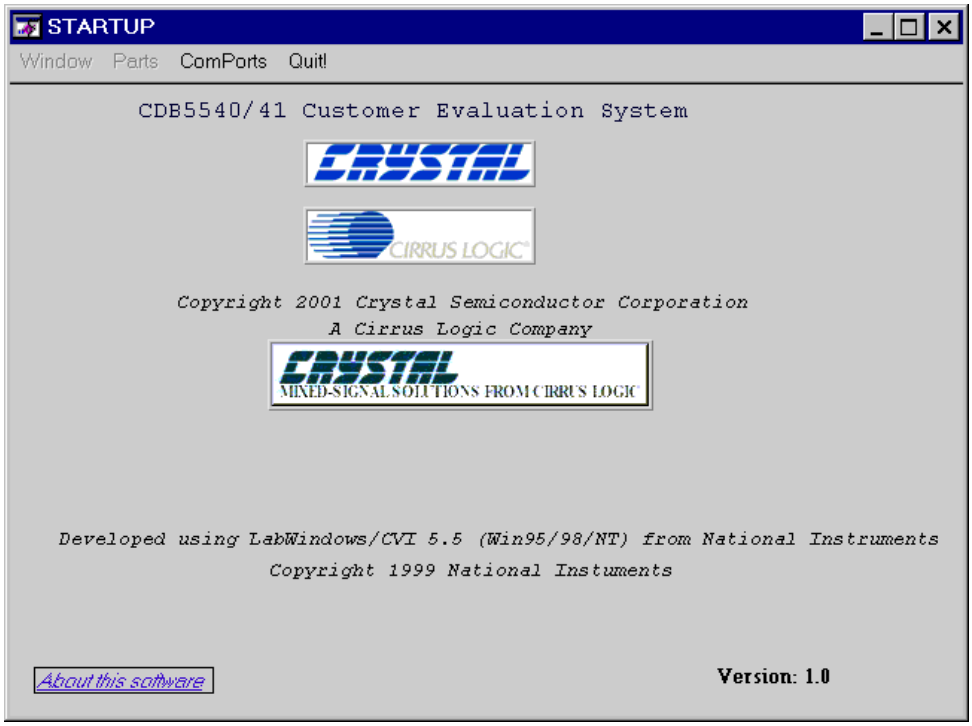


Figure 1. Title Screen

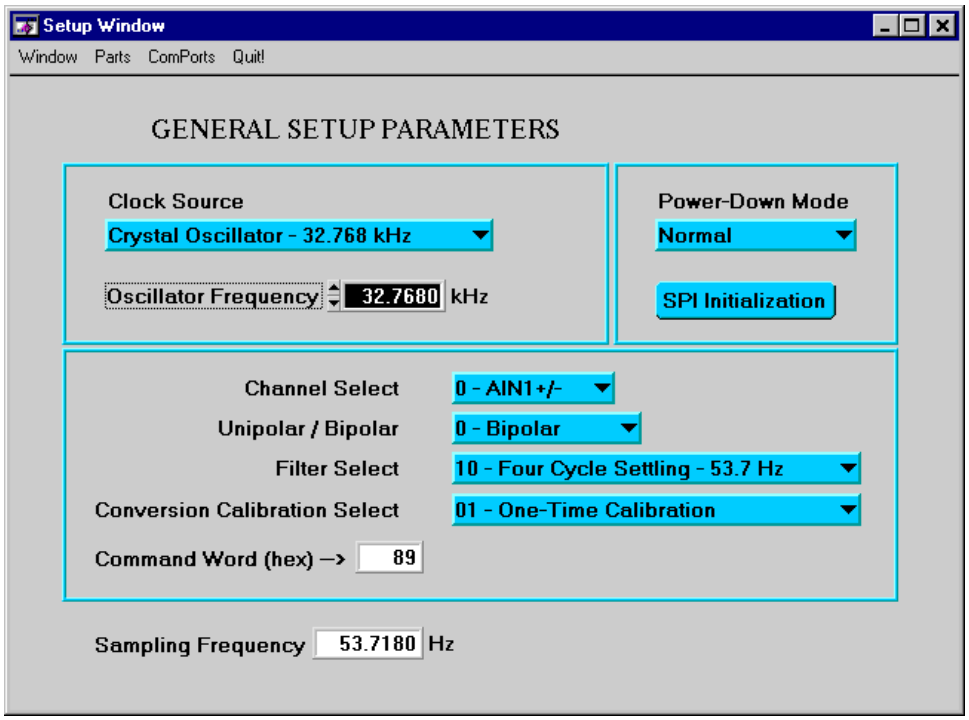


Figure 2. Setup Window

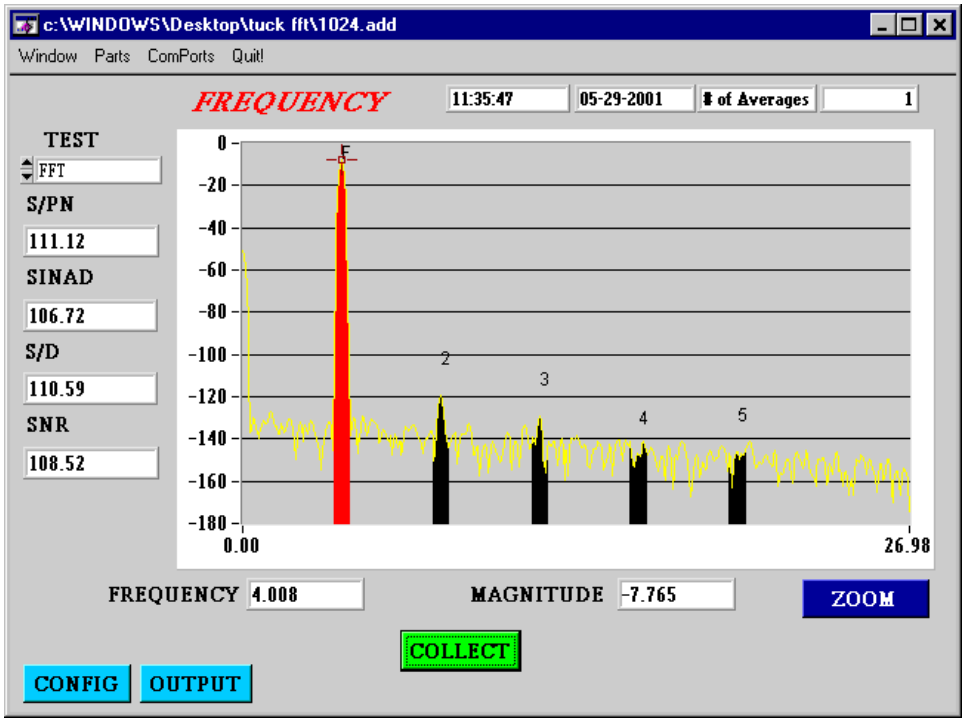


Figure 3. Frequency Domain Analysis

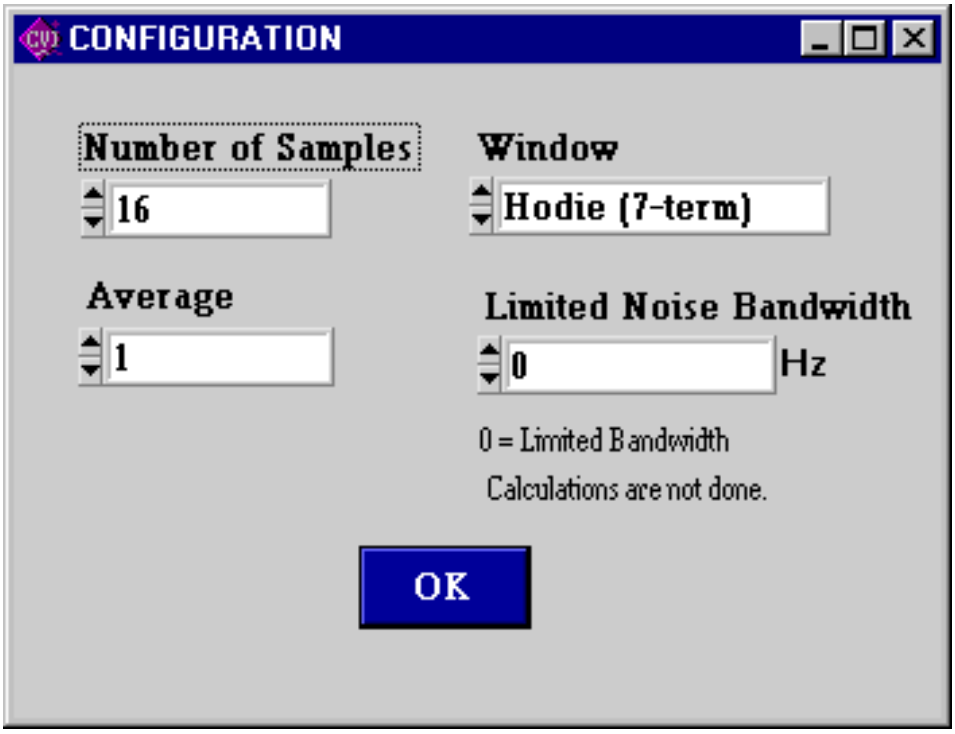


Figure 4. Configuration Panel

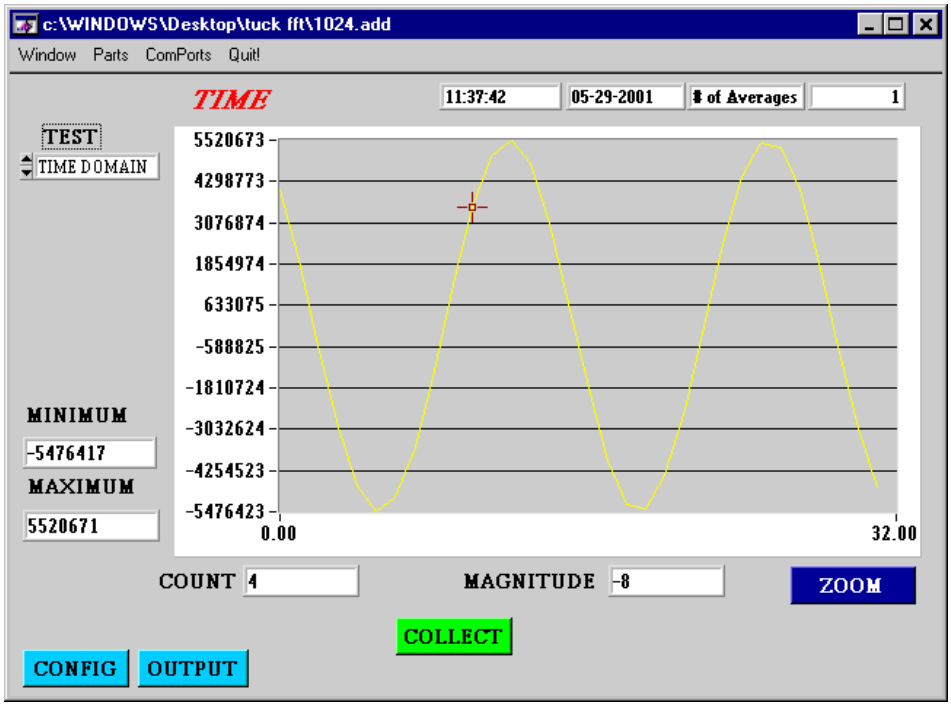


Figure 5. Time Domain Analysis

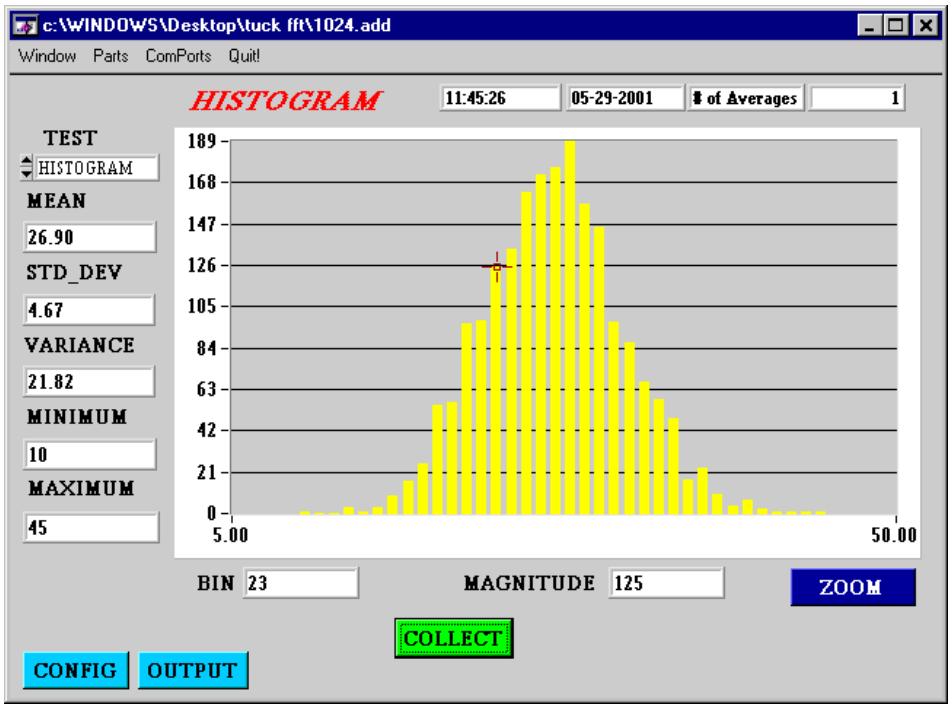


Figure 6. Histogram Analysis

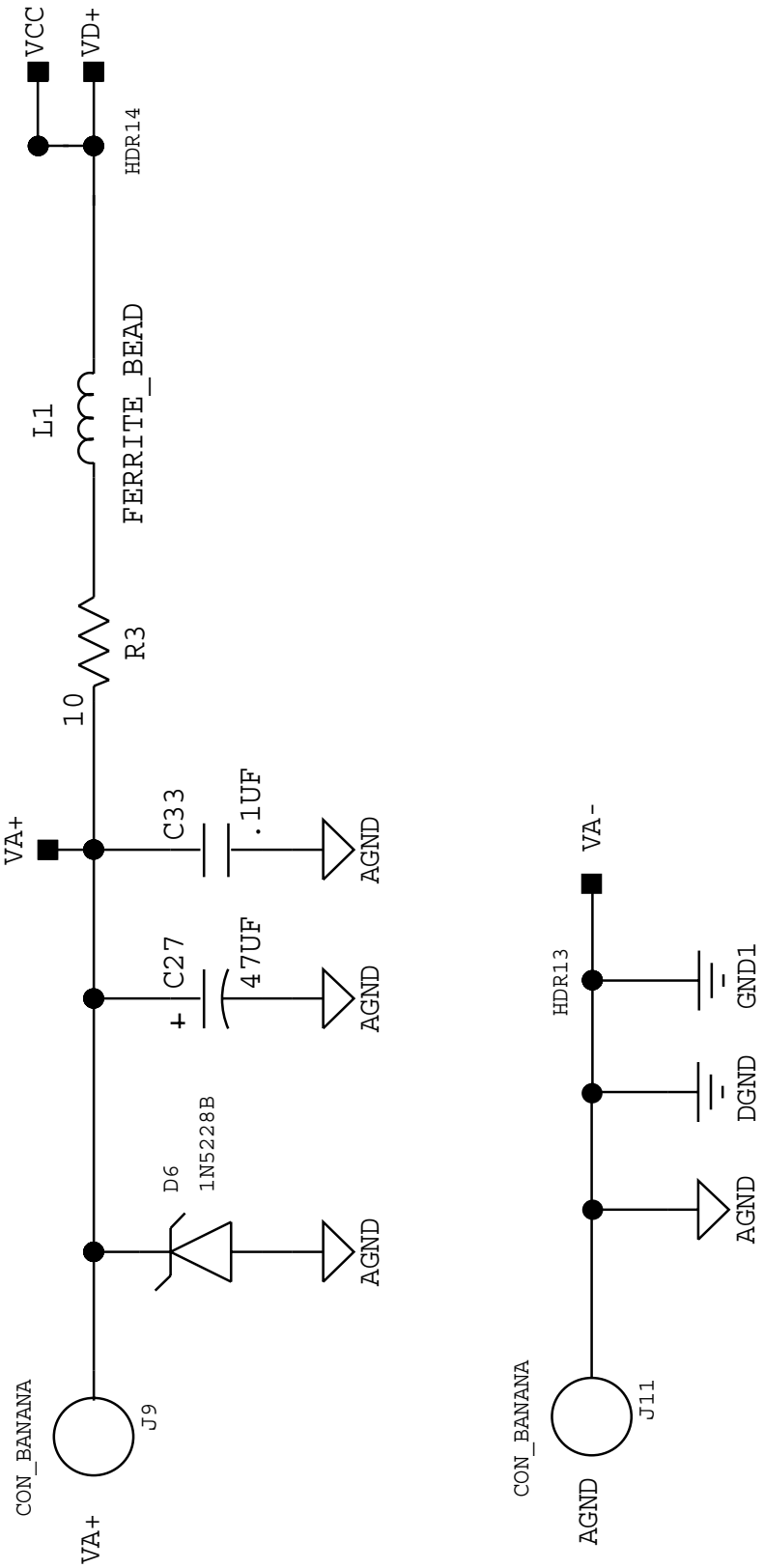
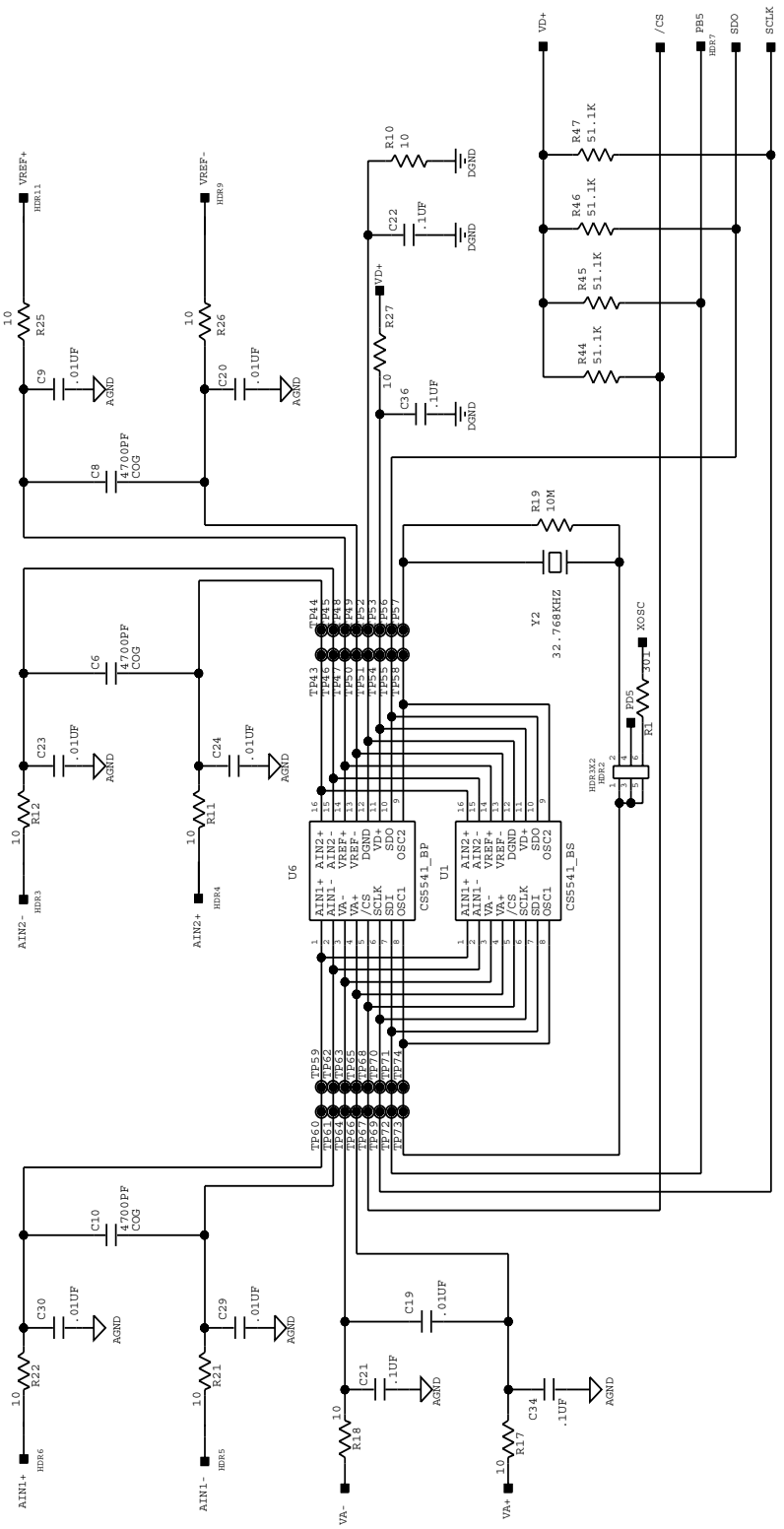
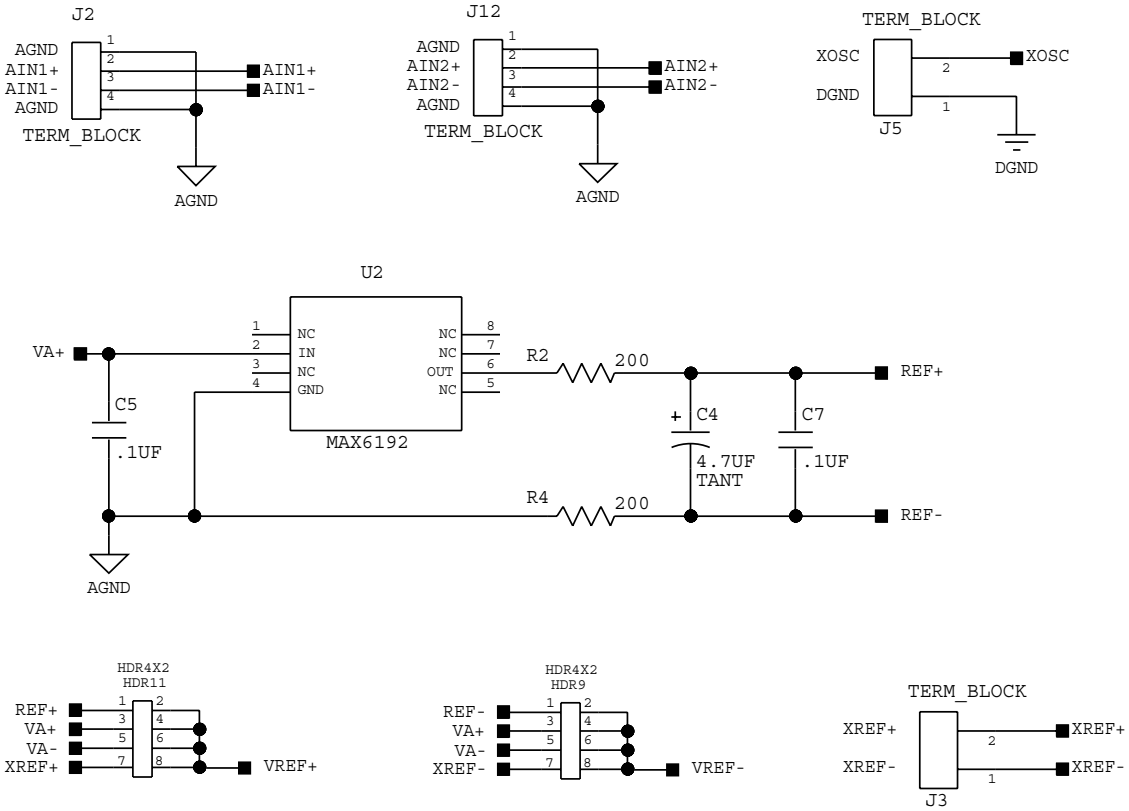


Figure 7. Power Supply Configuration



Reference	Description	HDR2
XTAL.	Selects On-Board Crystal	MCLK ● ● XTAL MCLK ○ ○ uC MCLK ○ ○ XOSC
uC.	Selects Micro-controller Clock	MCLK ○ ○ XTAL MCLK ● ● uC MCLK ○ ○ XOSC
XOSC.	Selects Exter-nal MCLK	MCLK ○ ○ XTAL MCLK ○ ○ uC MCLK ● ● XOSC

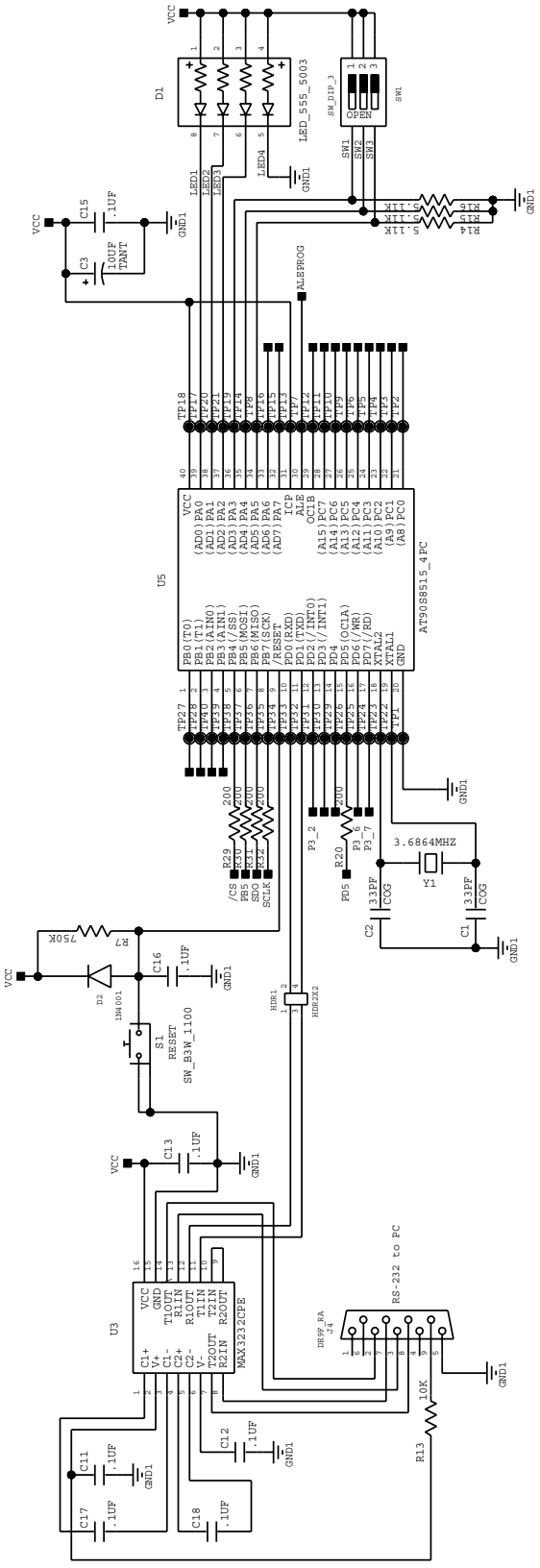
Figure 8. CDB5540/41 ADC Section

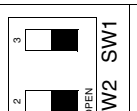
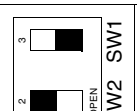
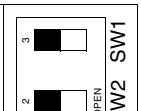


Reference	Description	HDR11	HDR9
REF.	Selects On-Board Reference	XREF+ O O VREF+ VA- O O VREF+ VA+ O O VREF+ REF+ O—O VREF+	XREF- O O VREF- VA- O O VREF- VA+ O O VREF- REF- O—O VREF-
Supply.	Selects Power Supply Voltage	XREF+ O O VREF+ VA- O O VREF+ VA+ O—O VREF+ REF+ O O VREF+	XREF- O O VREF- VA- O—O VREF- VA+ O O VREF- REF- O O VREF-
XREF.	Selects External Reference	XREF+ O—O VREF+ VA- O O VREF+ VA+ O O VREF+ REF+ O O VREF+	XREF- O—O VREF- VA- O O VREF- VA+ O O VREF- REF- O O VREF-

Voltage Reference Settings

Figure 9. Voltage Reference and External Connectors



Eval Board Mode	SW1 Settings
CS5540 SW1 is OPEN SW2 is OPEN SW3 is OPEN	
CS5541 SW1 is OPEN SW2 is CLOSED SW3 is OPEN	
RS-232 Test Mode SW1 is CLOSED SW2 is CLOSED SW3 is CLOSED	

DIP Switch SW1 Settings

Figure 10. Microcontroller, Test Switches and LED's

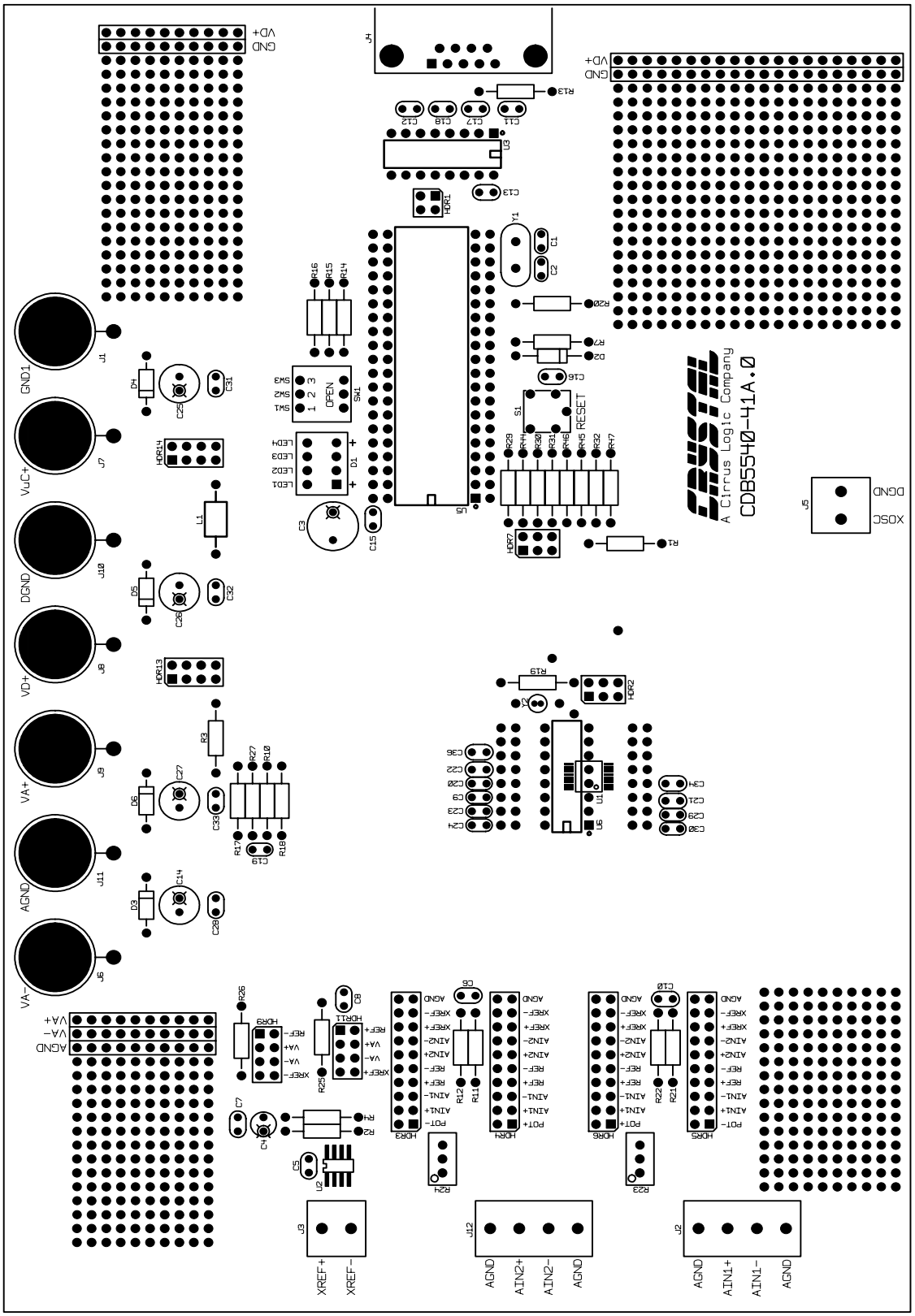


Figure 11. CDB5540/41 Layout (Silkscreen)

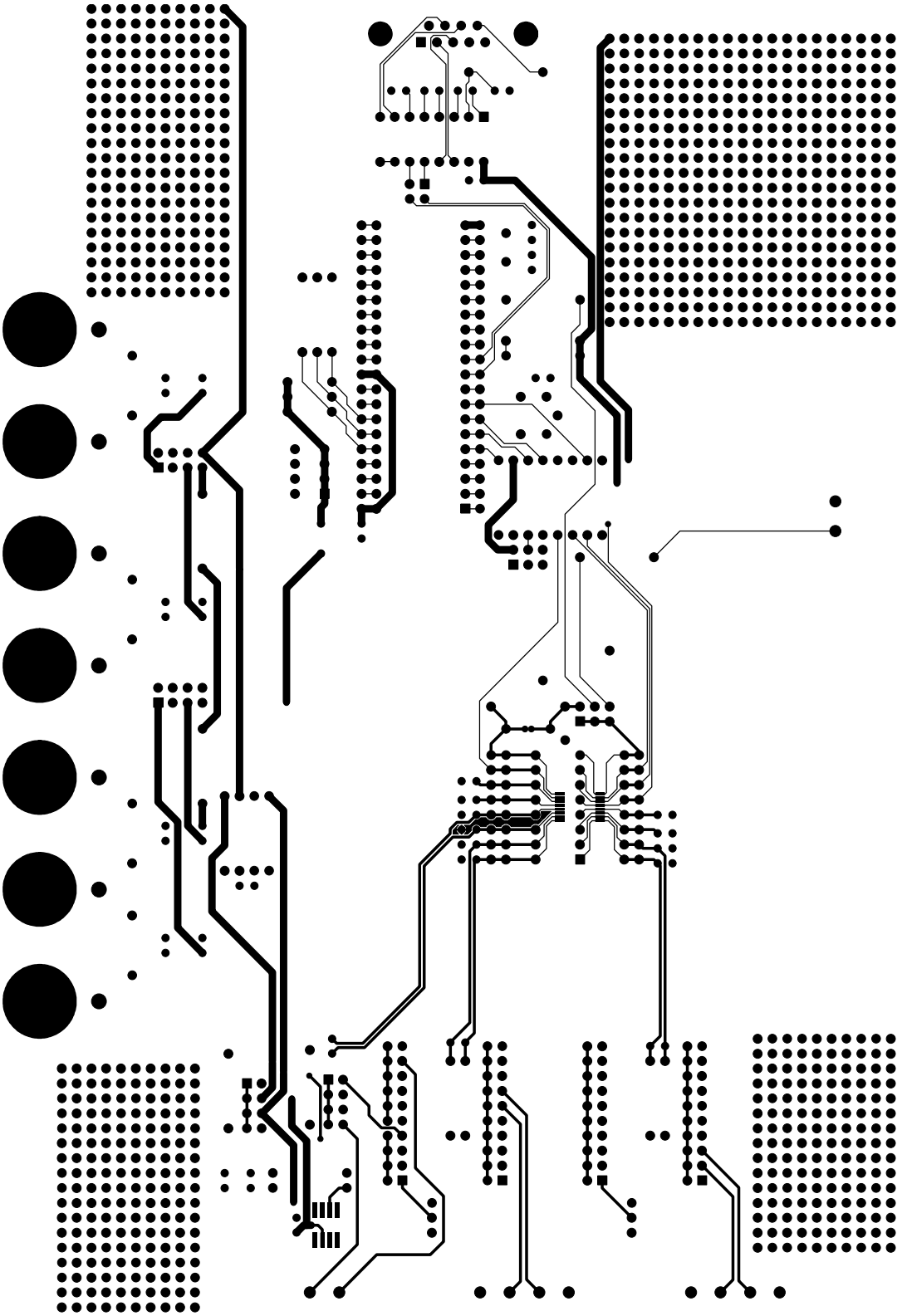


Figure 12. CDB5540/41 Layout (Top)

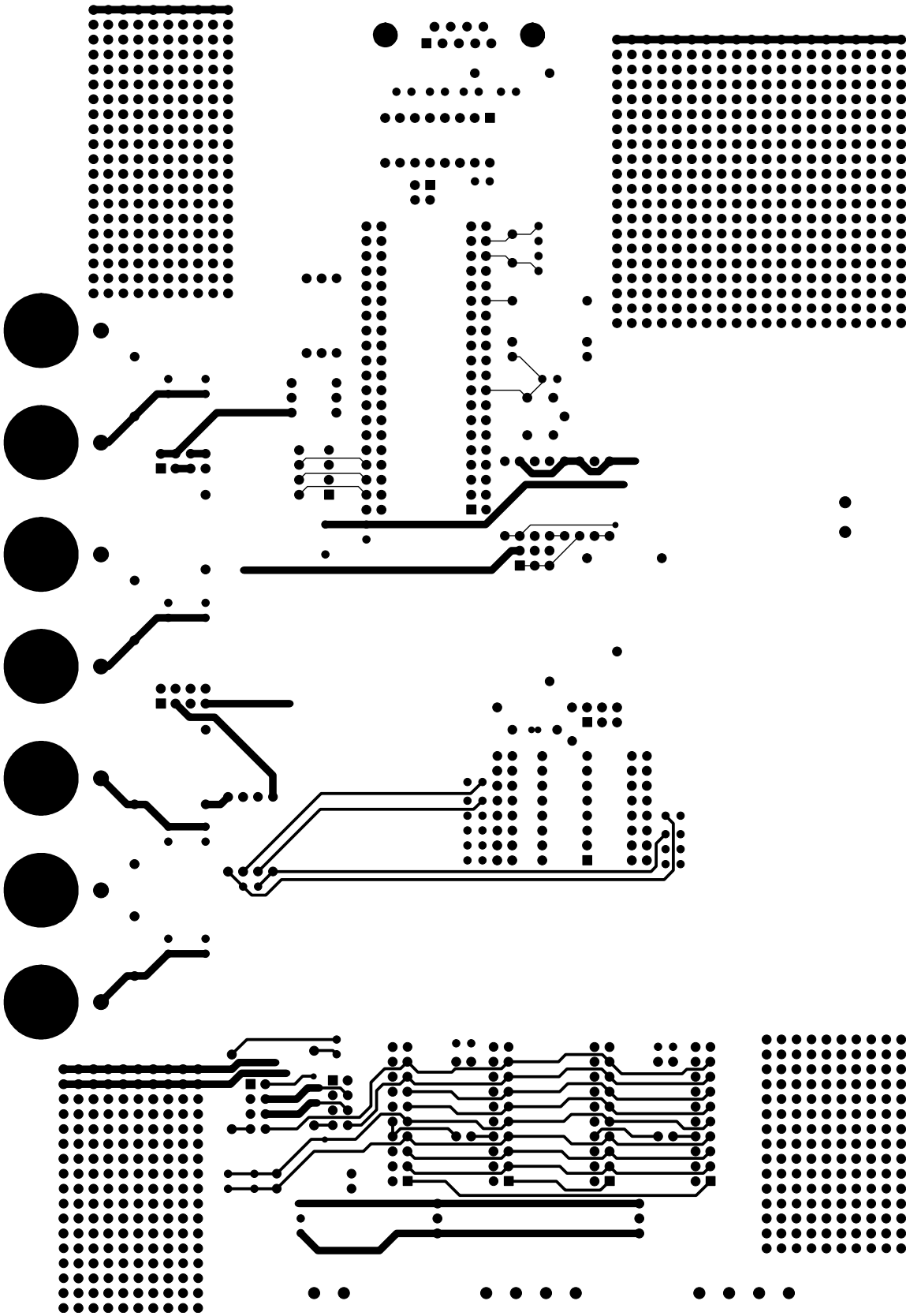


Figure 13. CDB5540/41 Layout (Bottom)

• Notes •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