CDB61881

Octal E1 Analog Front End

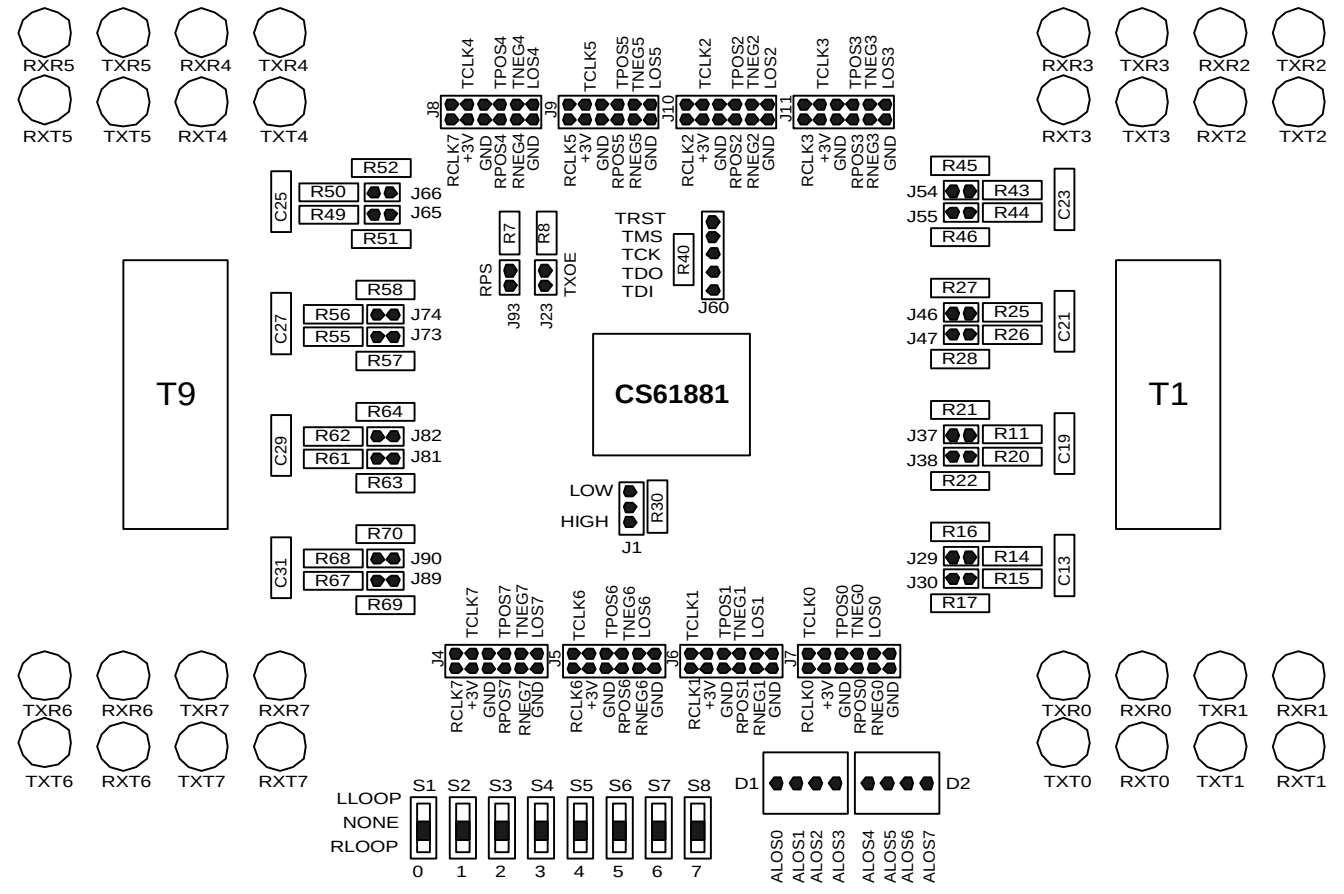
Features

- CS61881 Universal Line Interface
- All Required Components for CS61881 Evaluation
- LED Status Indications for Alarm Conditions and Operating Status
- JTAG Boundry Scan compliant to IEEE 1149.1
- Remote Loopback
- Local Loopback

Description

The evaluation board includes a CS61881 line interface device and all support components necessary for evaluation. The board is powered by an external +3.3 Volt supply.

The board may be configured for 75 Ω coax E1, or 120 Ω twisted-pair E1 short haul operation. Binding posts are provided for the line interface connections. Stake bed connectors provide clock and data I/O at the system interface. Eight LED indicators display the Loss of Signal (LOS) condition on each channel.



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. POWER SUPPLY

Power is supplied to the board from an external +3.3 Volt supply connected to the two binding posts labeled +3V and GND. There is also a +5V connector that can be used to drive external logic in the protoyping areas. The +3V binding post is shorted to the VLogic, RV+, TV+ and VCCIO pins of the device, under the J13 through J16 stake headers.

2. BOARD CONFIGURATION

Slide switches S1 through S8 selects Remote Loopback, Local Loopback, or Normal mode for each channel. Slide switch S11 sets the internal matched impedance of the receivers and transmitters for the 61881 device to either E1 75 or E1 120.

3. TRANSMIT CIRCUIT

The transmit clock and data signals are supplied on stake header pins labeled TCLK0-7, TPOS0-7, and TNEG0-7.

The transmitter output is coupled to the line through the transmit paths of the two transformers (T1 and T9). The signal is available at the Transmit binding posts labeled TXT0-7 and TXR0-7.

4. RECEIVE CIRCUIT

The receive signal is input at the Receive binding posts. The receive signal is transformer coupled to the CS61881 through the receive paths of the two transformers.

The receive line is terminated by resistors that supplement the on chip impedance matching circuits. They are socketed so the values may be changed according to the application. The evaluation board is supplied from the factory with 15 Ω resistors for terminating 120 Ω twisted-pair E1 lines, and 9.31Ω resistors for terminating 75 Ω coaxial E1 lines.

The recovered clock and data signals are available on stake pin headers labeled RCLK0-7, RPOS0-7, and RNEG0-7.

5. LED INDICATORS

The two four-LED packs D1 and D2 indicate signal states on LOS0-7. The LOS0-7 LED indicators illuminate when the line interface receiver has detected a loss of signal.

6. TRANSFORMER SELECTION

The evaluation board is supplied from the factory with TG63-S003NX transformers by Halo Electronics. The transformer T1 is for channels 0 through 3 and T9 is for channels 4 through 7.

7. PROTOTYPING AREA

Two prototyping areas are provided. each has a row of pads dedicated to power and ground. The power row is connected to VLOGIC, which can be connected to either +3.3V or +5V. This area can be used to develop and test a variety of additional circuits such as framer devices, system synchronizer PLLs, or specialized interface logic.

8. EVALUATION HINTS

1) The orientation of pin 1 for the CS61881 is marked by a small arrow on the bottom left side of the device U1.
2) Components for the receive and transmit circuits must have the correct values installed according to the application. All the necessary components are included on the evaluation board.
3) Properly terminate TTIP/TRING when evaluating the transmit output pulse shape. For more information concerning pulse shape evaluation, refer to the Crystal application note entitled "Measurement and Evaluation of Pulse Shapes in T1/E1 Transmission Systems." (AN007)

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Jumper	Position	Junction Selected
J1	High	Receiver operational
	Low	Receiver powered down
J4-J11	RCLKn-TCLKn	Connects RCLK to TCLK for channel n.
	+3V-TCLKn	Sets TCLK high on channel n.
	GND-TCLKn	Sets TCLK low on channel n.
	RPOSn-TPOSn RNEGn-TNEGn	Connects RPOS to TPOS and RNEG to TNEG for an external loopback on channel n.RPOSn/RNEGn can also be used to sense received data, while TPOSn/TNEGn can be used to drive transmit data to CS61881.
	LOSn	LOS output for channel n.
	GND	Ground
J13-J16	+3V	Connects either of the indicated circuitry to either the +3.3V or the +5V connector. VLOGIC powers the prototyping area, the pullup resistors on RPD, RPS, TXOE, and the LED driver U2. RV+ powers the receivers on the CS61881. TV+ powers the transmitters. VCCIO drives the VCCIO pin on the CS61881, which should be set to +3.3V for either 3V or 5V logic. Shorted to the +3V binding post under these stake headers
	+5V	
J23	Installed	Transmitter outputs disabled
	Open	Transmitter outputs enabled
J29,J30, J37,J38, J46,J47, J54,J55, J65,J66, J73,J74, J81,J82, J89,J90	Installed	Bypasses series resistors on receive lines, enabling matched impedance circuitry in receiver. Using this option, no component changes are necessary when changing between 75 Ω and 120 Ω lines. Latchup immunity is sufficient for most applications.
	Open	Enables series resistors for increased latchup immunity. Requires user to change resistor values depending on line impedance.
J93	Installed	Receiver Polarity = active high
	Open	Receiver Polarity = active low

Table 1. Jumper Selections

• Notes •


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