

CIRRUS LOGIC[®]

CS8420

Digital Audio Sample Rate Converter

The following information is based on the
technical datasheet:

CS8420 DS245PP2 AUG'99

Please contact Cirrus Logic for further
information.

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PRODUCT INFORMATION

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Digital Audio Sample Rate Converter

Features

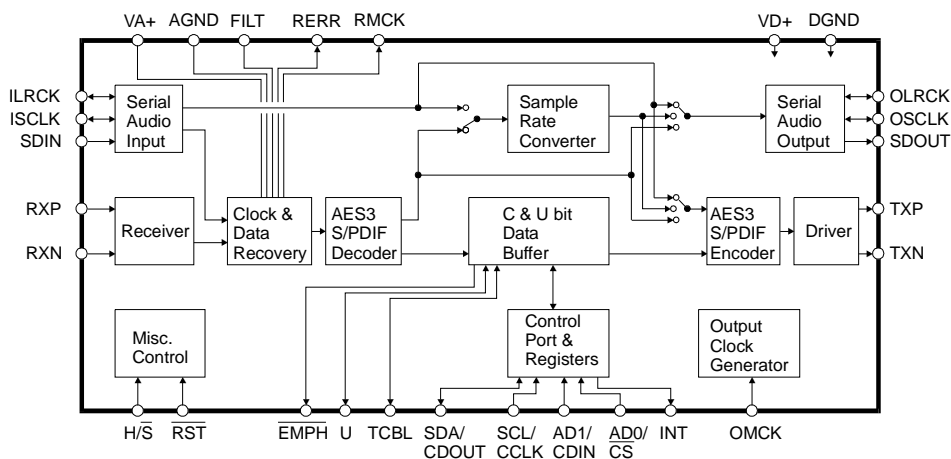
- Complete IEC60958, AES3, S/PDIF, EIAJ CP1201 compatible transceiver with asynchronous sample rate converter
- Flexible 3-wire serial digital i/o ports
- 8 kHz to 108 kHz sample rate range
- 1:3 and 3:1 maximum input to output sample rate ratio
- 128 dB dynamic range
- -117 dB THD+N at 1 kHz
- Excellent performance at almost a 1:1 ratio
- Excellent clock jitter rejection
- 24 bit i/o words
- Pin and micro-controller read/write access to Channel Status and User Data
- Micro-controller and stand-alone modes

Description

The CS8420 is a stereo digital audio sample rate converter (SRC) with AES3 type and serial digital audio inputs, AES3 type and serial digital audio outputs, along with comprehensive control ability via a 4-wire microcontroller port. Channel status and user data can be assembled in block sized buffers, making read/modify/write cycles easy.

Digital audio inputs and outputs may be 24, 20 or 16 bits. The input data can be completely asynchronous to the output data, with the output data being synchronous to an external system clock.

Target applications include CD-R, DAT, MD, DVD and VTR equipment, mixing consoles, digital audio transmission equipment, high quality D/A and A/D converters, effects processors and computer audio systems.



Overview

The CS8420 is a fully asynchronous sample rate converter plus AES3 transceiver intended to be used in digital audio systems. Such systems include digital mixing consoles, effects processors, tape recorders and computer multimedia systems. The CS8420 is intended for 16, 20, and 24-bit applications where the input sample rate is unknown, or is known to be asynchronous to the system sample rate.

On the input side of the CS8420, AES3 or a 3-wire serial format can be chosen. The output side produces both AES3 and a 3-wire serial format. An I²C/SPI compatible microcontroller interface allows full block processing of channel status and user data via block reads from the incoming AES3 data stream and block writes to the outgoing AES3 data stream. The user can also access information decoded from the input AES3 data stream, such as the presence of non-audio data and pre-emphasis, as well as control the various modes of the

device. For users who prefer not to use a micro-controller, six hardware modes have been provided, documented towards the end of this data sheet. In these modes, flexibility is limited, with pins providing some programmability.

When used for AES3 in, AES3 out applications, the CS8420 can automatically transceive user data that conforms to the IEC60958 recommended format. The CS8420 also allows access to the relevant bits in the AES3 data stream to comply with the serial copy management system (SCMS).

The diagram on page 2 shows the main functional blocks of the CS8420.

Familiarity with the AES3 and IEC60958 specifications are assumed throughout this document. The Application Note: “Overview of Digital Audio Interface Data Structures”, contains a tutorial on digital audio specifications. The paper “An Understanding and Implementation of the SCMS Serial Copy Management System for Digital Audio Transmission”, by Clif Sanchez, is an excellent tutorial on SCMS. It may be obtained from Crystal Semiconductor, or from the AES.

To guarantee system compliance, the proper standards documents should be obtained. The latest AES3 standard should be obtained from the Audio Engineering Society or ANSI, the latest IEC60958 standard from the International Electrotechnical Commission and the latest EIAJ CP-1201 standard from the Japanese Electronics Bureau.

FAQs

1) Q: I am using the chip in SRC mode. Why are there sounds at the outputs when the AES input is removed?

A: The receiver holds the last value that it receives before it loses lock. The sample rate ratio then becomes a large value because RMCK drops to a low frequency when the PLL is unlocked. This means that a constant input value is sample rate converted by coefficients that are extreme values. The result is a series of tones at the outputs that may be of any amplitude. This is a characteristic of early revisions of the part. In Revision D, a feature is being added to allow you to mute the outputs upon loss of lock.

2) Q: The part is used in SRC transceiver mode or transceiver mode and the transmitter does not start to Transmit until the receiver has received data?

A: There is a state machine that starts up the functions of the part after reset. It does not complete its process until the PLL has locked. Contact our applications group for possible workarounds.

3) Q: How can I optimize the phase lock loop filter for my application?

A: Application note 159 contains equations to allow you to optimize the PLL filter for different applications.

4) Q: Can I run the output serial port and the AES transmitter at different rates?

A: No. The clock system for these two output ports is shared, and they both must run at the same sample rate.

5) Q: I want to input a signal to the SRC at almost the same rate as the output sample rate. How will the part perform under those conditions?

A: There is no performance degradation when functioning at an almost 1:1 ratio.

6) Q: How do I determine the delay through the sample rate converter?

A: The group delay (tgd) through the SRC is $41/F_{si} + 43/F_{so}$.

Ordering Information

CS8420-CS	28-pin SOIC	-10 to 70 °C
CDB8420	Evaluation Board	



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