Introducing Maverick EP9312

Jeff Klaas - Director of Engineering

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Optional

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Create a cost-effective solution for a digital audio jukebox meeting the following goals:

➡ Quick time-to-market

➡ 10x Real-time MP3 encoding

➡ Hardware based content security

➡ High-quality audio

➡ Home network enabled

➡ Robust I/O for OEM flexibility

➡ Low cost storage options

➡ Flexible user interface

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✔ ARM 920T Core

✔ MaverickCrunch^{TM} Engine

✔ MaverickLock^{TM} Security

✔ EIDE Controller

✔ Ethernet MAC

✔ I^{2}S 24-bit audio Interface

✔ USB, UARTs, IrDA

✔ LCD Controller

✔ Touchscreen Controller

✔ Keypad Interface

The right feature set and performance level at the right price-point!

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ARM920T Processor
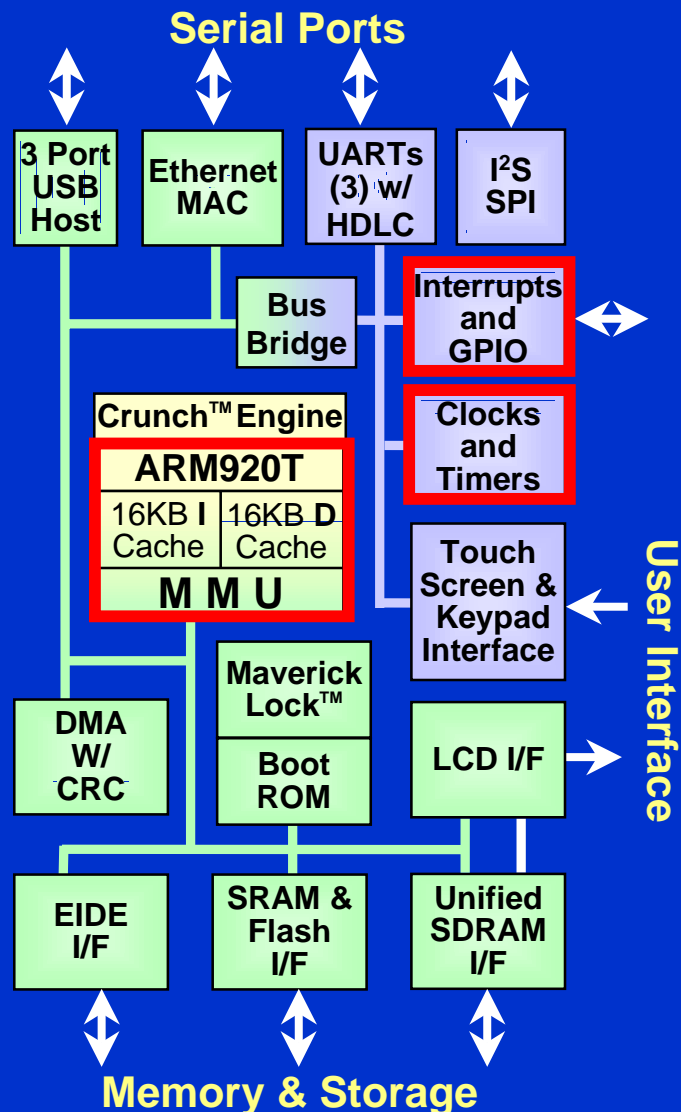
✔ 200 MHz Processor Clock
✔ 16KB instruction & data caches
✔ 64 entry instruction & data TLB
✔ Independent lockable pages
✔ Windows CE compatible MMU

Flexible interrupts & GPIO

✔ Up to 64 interrupts
✔ 32 priority levels
✔ 16 expanded GPIO signals

Clocks & Timers

✔ Dual PLL produces all clocks
✔ 6 timers & clocks + RTC

Serial Ports

| 3 Port USB Host | Ethernet MAC | UARTs (3) w/ HDLC | I²S SPI |

Bus Bridge · Interrupts and GPIO

Crunch™ Engine
ARM920T
16KB I Cache · 16KB D Cache
M M U

Clocks and Timers

Touch Screen & Keypad Interface

DMA W/ CRC · Maverick Lock™ · Boot ROM · LCD I/F

EIDE I/F · SRAM & Flash I/F · Unified SDRAM I/F

User Interface

Memory & Storage

General Architecture for Market Specific Extensions

✔ Balanced approach to algorithm efficiency

✔ Floating point, integer and signal processing instruction set

✔ Hardware Interlocks to remove implementation details

✔ Full tools support from Cygnus

It ain't PICCOLO!

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Bus Bridge

Interrupts and GPIO

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DMA W/ CRC

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User Interface

EIDE I/F	SRAM & Flash I/F	Unified SDRAM I/F

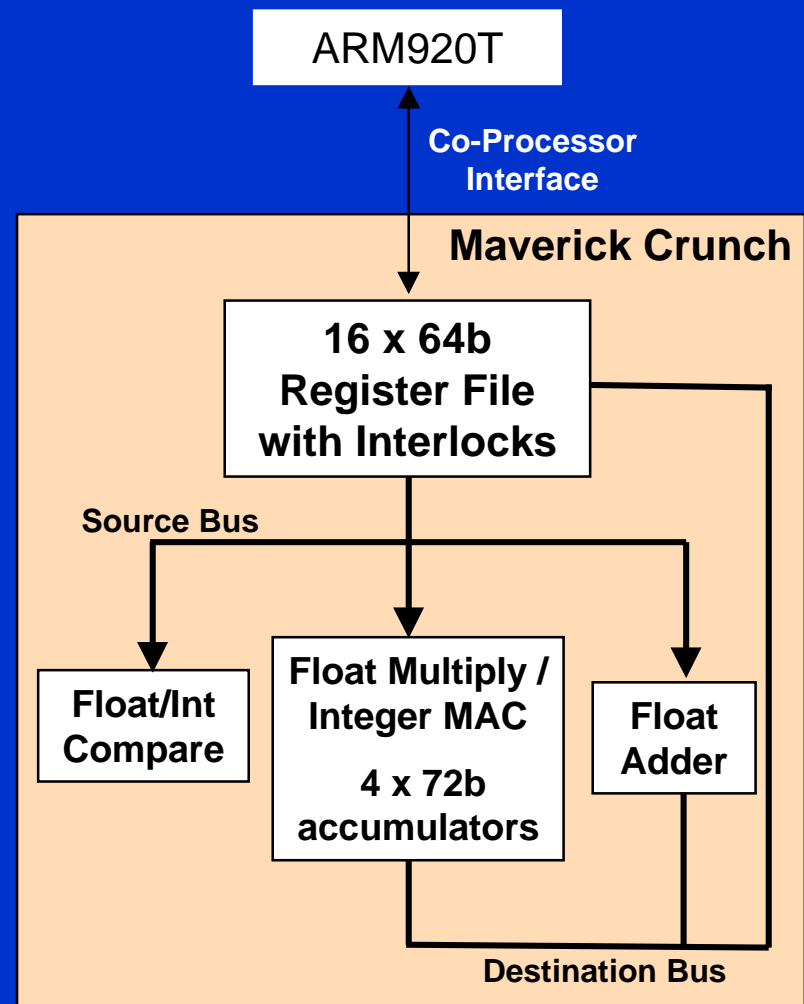**Memory & Storage**

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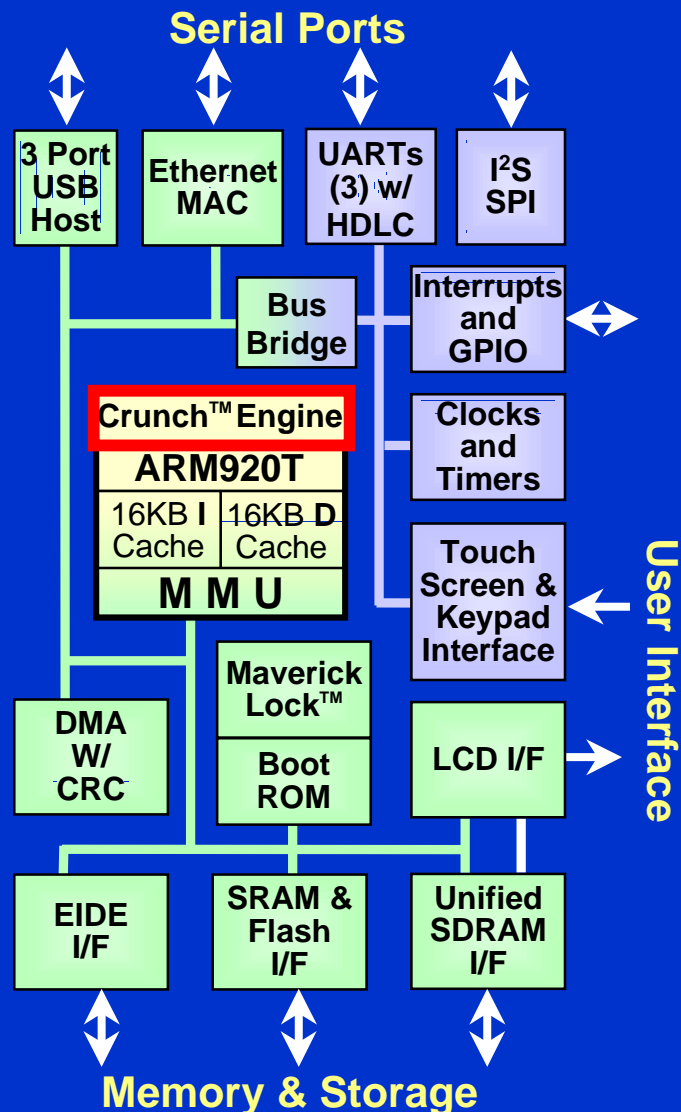
Hardware Support

- ✔ IEEE Single/Double Floating Point
- ✔ 32/64 Bit Integer
- ✔ Add/Multiply/Compare
- ✔ Integer MAC 32-bit input with 72 bit accumulate
- ✔ Integer Shifts
- ✔ Float ⬌ Integer Conversion

Implementation

- ✔ Register file is 0 stall at CPU speed
- ✔ < 2mm^2 in 0.25u
- ✔ Hardware forwarding and interlock

ARM920T

Co-Processor Interface

Maverick Crunch

16 x 64b Register File with Interlocks

Source Bus

Float/Int Compare

Float Multiply / Integer MAC

4 x 72b accumulators

Float Adder

Destination Bus

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Single Code Stack for Control and Computation

✔ ARM handles loop and addressing

✔ Maverick Crunch handles compute

✔ Integer MAC (32bit X 32bit + 72bit --> 72bit) for high MIP filters

✔ IEEE-754 floating point provides dynamic range

✔ 16x64b register file plus 4x72b accumulators

High Precision FIR Followed by Scale

✔ 17 * (N/4) + 26 with Maverick Crunch
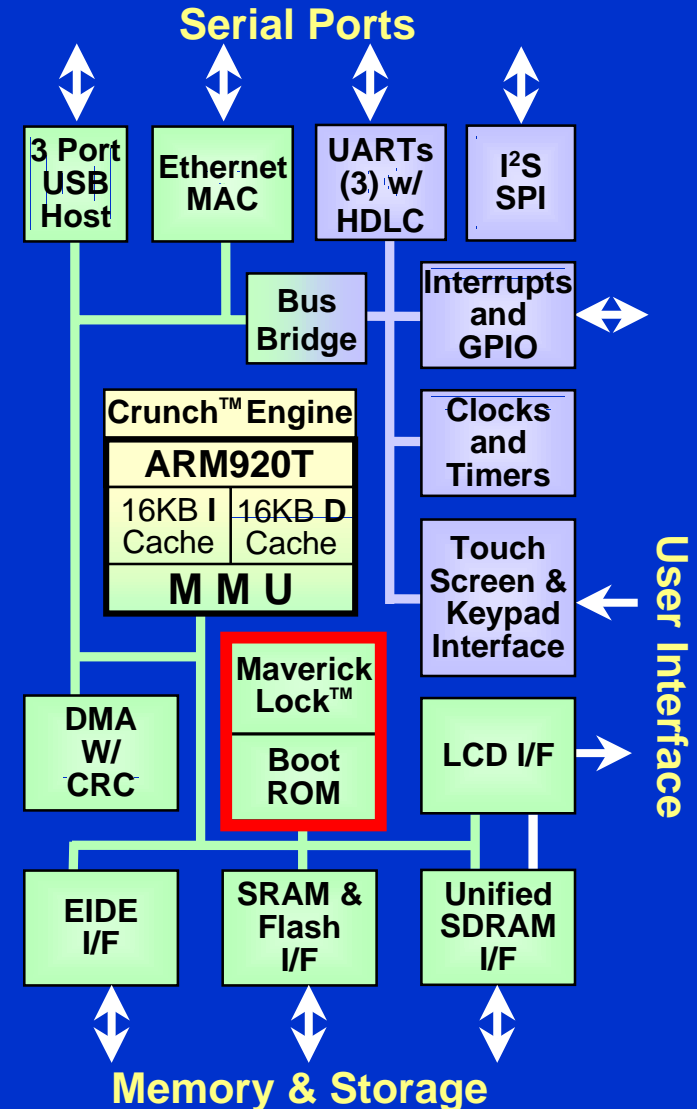
✔ >6X improvement over ARM9 CPU

```
;Floating point example
;R2 points to start of filter data block
;R3 points to start of filter coefficient block
;R4 points to scale factors
;R5 points to stored value

;Loop setup
;N/4 Loop Software unrolled for minimum stalls
loop:
  SUBS      R0, R0, #1                  ;decrement loop count
  CMP       R0, #0                      ;Test loop counter
  CFLDR32    MVFX0, [R2] ,#4            ;Load Coprocessor regs w/data
  CFLDR32    MVFX1, [R3] ,#4            ;Load Coprocessor regs w/data
  CFLDR32    MVFX2, [R2] ,#4            ;Load Coprocessor regs w/data
  CFLDR32    MVFX3, [R3] ,#4            ;Load Coprocessor regs w/data
  CFLDR32    MVFX4, [R2] ,#4            ;Load Coprocessor regs w/data
  CFMADDA32  MVAX0, MVAX0, MVFX0, MVFX1 ;FX0*FX1+AX0->AX0
  CFLDR32    MVFX0, [R3] ,#4            ;Load Coprocessor regs w/data
  CFMADDA32  MVAX0, MVAX0, MVFX2, MVFX3 ;FX2*FX3+AX0->AX0
  CFLDR32    MVFX1, [R2] ,#4            ;Load Coprocessor regs w/data
  CFLDR32    MVFX2, [R3] ,#4            ;Load Coprocessor regs w/data
  CFMADDA32  MVAX0, MVAX0, MVFX4, MVFX0 ;FX4*FX0+AX0->AX0
  CFMADDA32  MVAX0, MVAX0, MVFX1, MVFX2 ;FX1*FX2+AX0->AX0
  BNE       loop                        ;Exit if equal

;Finish calculations
  NOP                                   ;Any Non-coprocessor Inst
  NOP                                   ;Any Non-coprocessor Inst
  CFMV64A    MVDX10, MVAX0              ;Convert i72A->i64, sat & rnd
  CFLDRS    MVF13, [R4]                 ;Load coprocessor scale factor
  CFCVT64S   MVF11,  MVDX10            ;Convert i64->f32
  CFMULS     MVF14,  MVF11, MVF13      ;Multiply two f32's
  CFSTRS     MVF14,  [R5]              ;final result stored to mem
```
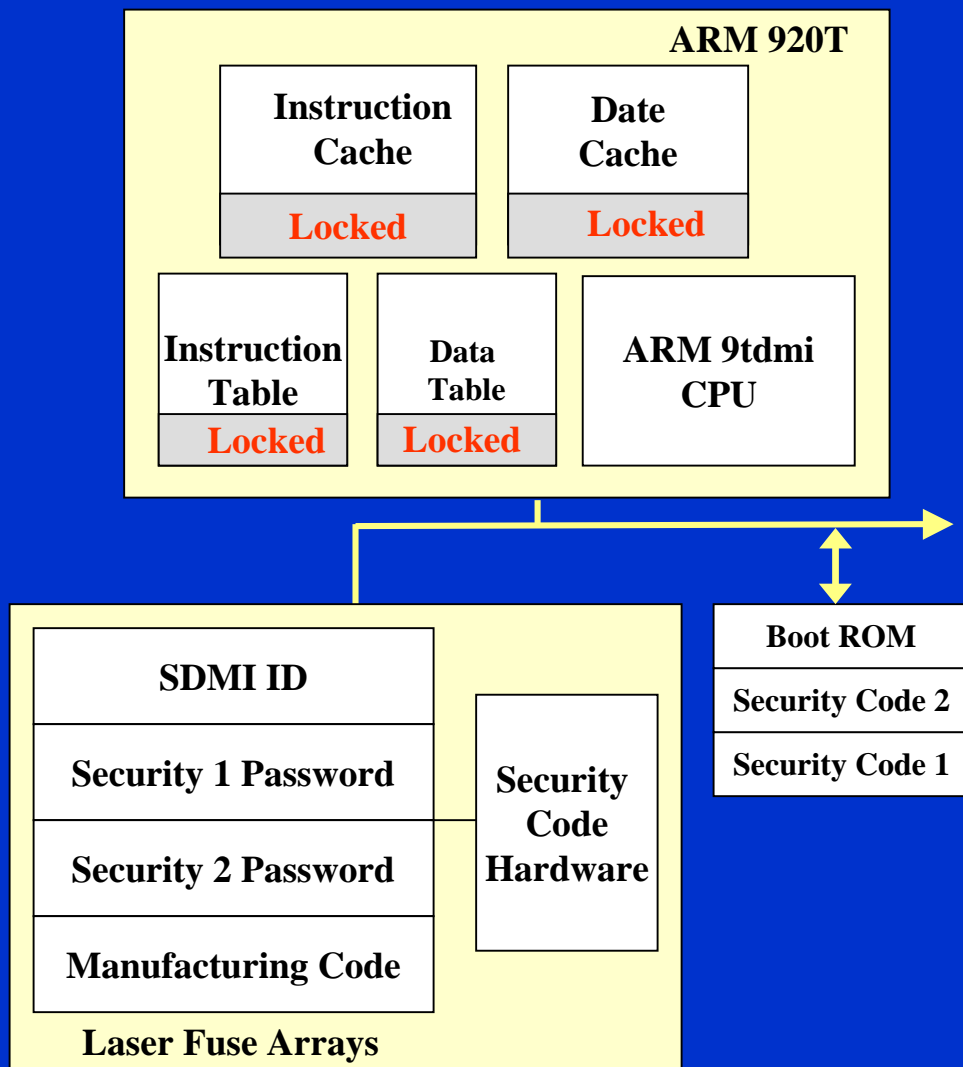
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MaverickLock™ Security

Secrets stay Secret

- ✔ Unique emulation technology allows CPU to create locked Cache/MMU entries without internal or external memory

- ✔ 256 bits of laser fuses provide on chip permanent IDs and passwords

- ✔ Security boot firmware and private passwords are "invisible" except when IC is "Locked"

- ✔ Debug and manufacturing test modes disabled when IC is "Locked"

- ✔ Encrypted Firmware

Serial Ports

| 3 Port USB Host | Ethernet MAC | UARTs (3) w/ HDLC | I²S SPI |

Bus Bridge · Interrupts and GPIO

Crunch™ Engine — ARM920T — 16KB I Cache · 16KB D Cache — M M U

Clocks and Timers · Touch Screen & Keypad Interface

Maverick Lock™ — Boot ROM · LCD I/F

DMA W/ CRC

User Interface

| EIDE I/F | SRAM & Flash I/F | Unified SDRAM I/F |

Memory & Storage

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Single IC provides secure hardware environment

✔ General architecture that can be used by partner security vendors

✔ Combination of boot ROM, laser fuses and gate level IP

✔ Multiple security vendors can co-exist in same system

ARM 920T

Instruction Cache	Date Cache
Locked	**Locked**

Instruction Table	Data Table	ARM 9tdmi CPU
Locked	**Locked**	

SDMI ID

Security 1 Password

Security 2 Password

Manufacturing Code

Security Code Hardware

Laser Fuse Arrays

Boot ROM

Security Code 2

Security Code 1

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Maverick 9312

## Wide choice of input sources

- ✔ 3.6864 MHz
- ✔ 4.0 MHz
- ✔ 12.288 MHz
- ✔ Many other viable options

Multiple clock requirements

- ✔ Independent processor & video clocks
- ✔ 48 MHz - USB and IrDA
- ✔ 18.432 MHz - IrDA
- ✔ 25 MHz - Ethernet
- ✔ 3.6864 MHz- UARTs
- ✔ 48 KHz Audio (3.072 MHz * 2, 3, or 4)

Implementation

- ✔ Dual cascadable PLLs
- ✔ Glitch-free enable/disable
- ✔ Programmable frequency control
- ✔ Programmable phase control

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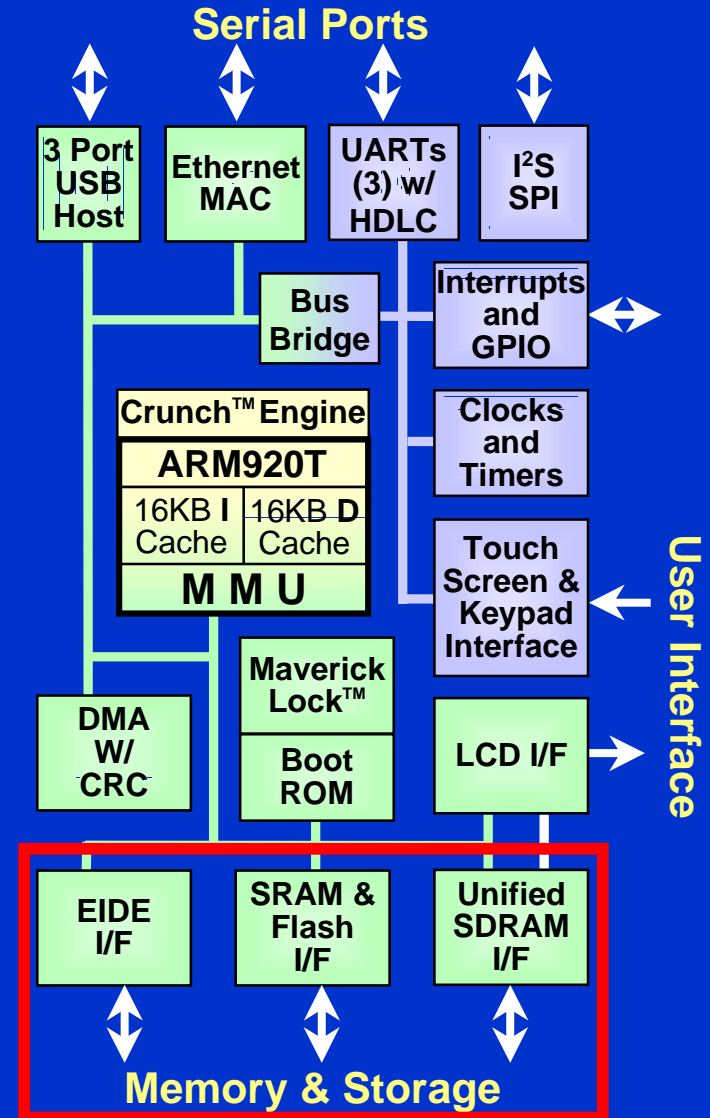# Memory & Storage Interfaces
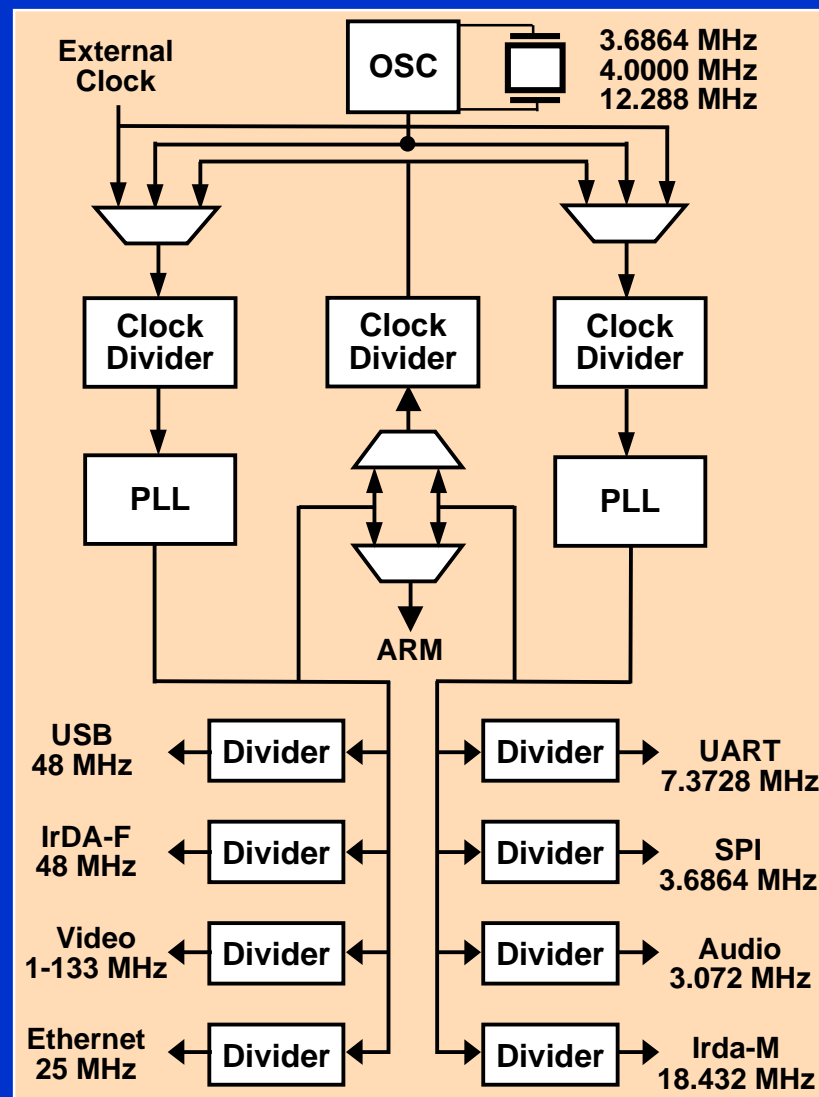
SDRAM interface (unified memory)

✔ 1-4 banks of 66 or 100 MHz SDRAM

✔ 16 or 32-bit data path

✔ Separate display refresh port

EIDE interface

✔ Up to UDMA-33 performance

✔ Supports two devices (CD & hard drive)

General purpose memory interface

✔ ROM

✔ SRAM

✔ Flash Memory

✔ 8 chip selects

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Memory & Storage

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Ethernet Media Access Controller

✔ Media independent interface to external PHY
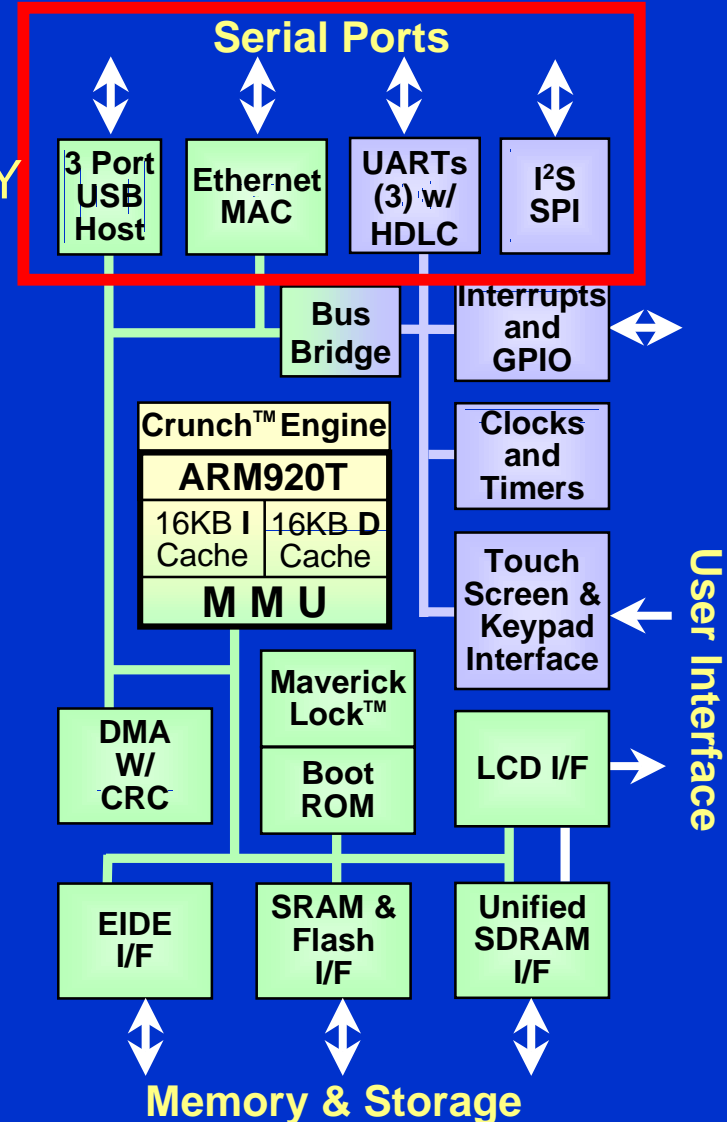✔ 1, 10, 100 Mbps operation
✔ HPNA 1.0 compatible

3 port USB host

✔ Integrated USB PHYs
✔ USB 1.0 protocol

Audio & telephony

✔ Interfaces directly to I^2S codec
✔ Interfaces directly to serial soft modem
✔ Alternate configuration as SPI

Three 16550 compatible UARTs

✔ UART with HDLC
✔ UART with modem & HDLC
✔ UART with slow, medium, and fast IrDA

Serial Ports

3 Port USB Host	Ethernet MAC	UARTs (3) w/ HDLC	I^2S SPI

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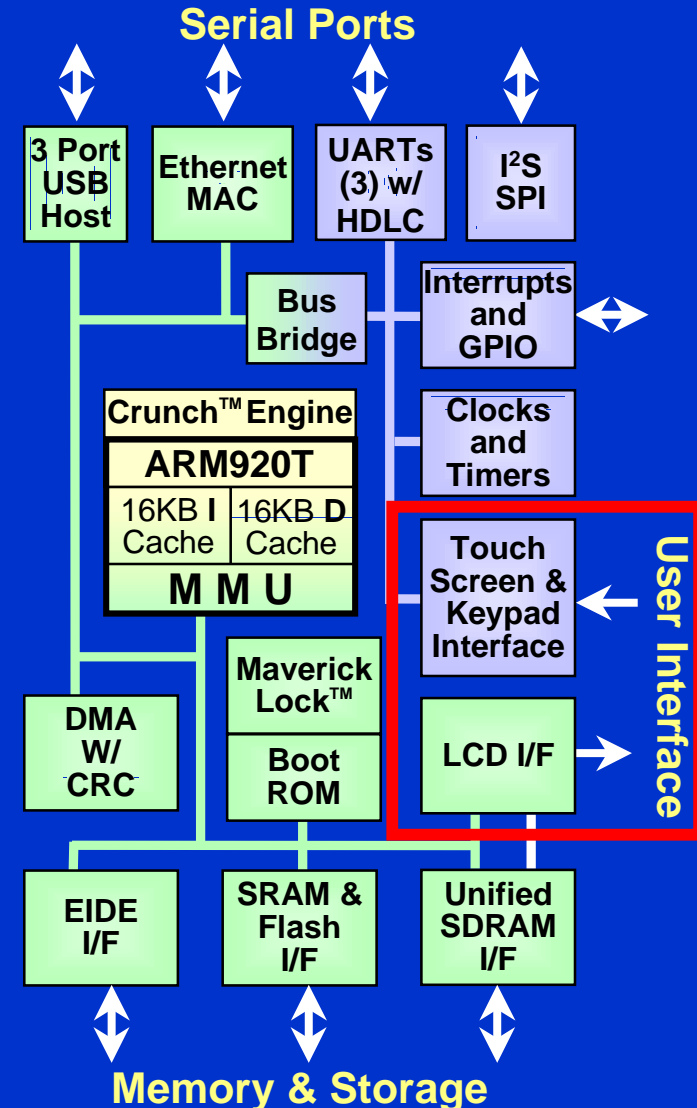**Memory & Storage**

User Interface

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LCD interface

- ✔ 4, 8, 16, 18 bits per pixel
- ✔ Dedicated SDRAM memory port
- ✔ Pulse width modulated brightness control
- ✔ 6-bit DAC for LCD contrast control

Touchscreen interface

- ✔ 4, 5, or 8-wire resistive screen
- ✔ Touchscreen interrupt provided
- ✔ Onboard ADC input

8 x 8 keyboard scan

- ✔ Interrupt generated on each new key stroke
- ✔ Keyscan register cleared each time it is read
- ✔ Hardware debouncing

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User Interface

Memory & Storage

- **Transistor count ~ 5.7 million**

- **Process - 0.25u, single poly, 4 metal (6SF)**

- **Supply voltages - 2.5V core, 3.3V pads**

- **Processor speed - 200 MHz**

- **Bus speed - 100 MHz**

- **Package - 20x20 PBGA, 352 pin**

- **Pads - 332 on 65u pitch**

- **Power dissipation - <1.5W**

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Serial Ports

I²S Codec ↔ SPI DAA

HPNA

IR Keyboard or Remote Control

Maverick EP9312

Front Panel Keypad

LCD Panel

SDRAM
EEPROM
FLASH

3 Port USB Host

Ethernet MAC

UARTs (3) w/ HDLC

I²S SPI

Bus Bridge

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