10/27/98

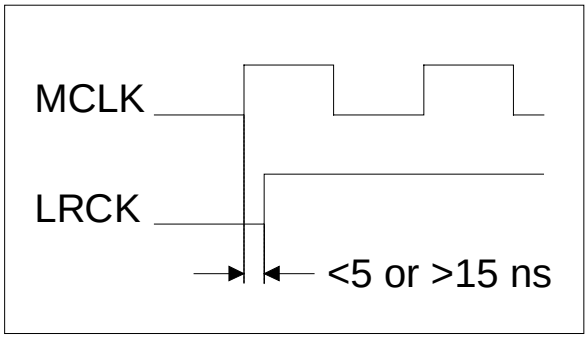
Errata: CS4222 Rev. C

(Reference CS4222 Data Sheet — DS236PP3 JAN '97)

CS4222 Revision C known problems. These problems also affect Rev. A plus the other known problems in that revision.

1) The Converter Status Report Byte contains the left and right channel ADC level monitor bits. These bits are supposed to reset when read. Due to an error in the design of the chip they reset when byte 5, the DSP Port Mode Byte is read. To read and reset the bits, read byte 6 then read byte 5 to do the reset.

2) The following timing constraint was omitted from the data sheet: The rising edge of LRCK must be less than 5 ns or more than 15 ns after the rising edge of MCLK. This constraint can be met by synchronizing the LRCK with either the rising or falling edge of MCLK.



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3) The data sheet defines bit 6 of the DAC Control Byte (MUTC) as

MUTC Controls mute on consecutive zeroes function

0 - 512 consecutive zeroes will mute DAC

1 - DAC output will not mute on zero

however, Rev C silicon is implemented such that

MUTC Controls mute on consecutive zeroes function

0 - DAC output will not mute on zero

1 - 512 consecutive zeroes will mute DAC

the register default remains 00h.

4) ADC input full scale specification is 2.0Vrms +/-9%..

If there are any questions concerning this information,
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