A DIVISION OF CIRRUS LOGIC

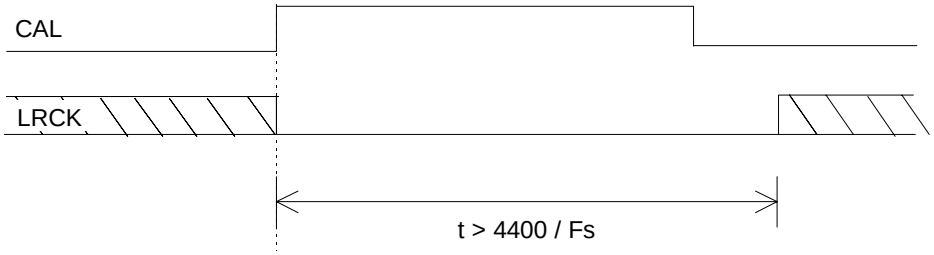
10/7/97

Errata: CS5394 Revision B

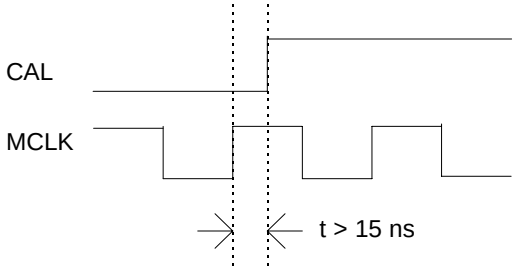
CS5394 : 117 dB, 48 kHz Audio A/D Converter (DS258PP3 NOV '96)

This information is provided to document the performance of the CS5394 revision B silicon. These items will be fixed in revision C silicon.

- When in slave mode, the part must be calibrated with the LRCK low as in the following diagram:



- The rising edge of the CAL pin must lag the rising edge MCLK by at least 15 ns as in the diagram below:



Datasheet Changes/Additions

- Power consumption is 740 mW typical.
- MCLK max fall time is 8 ns.
- Pin 15 is connected to DGND.

If there are any questions concerning this information please call:
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