07/22/99

Errata: CS5460 Rev. A

(Reference CS5460 Data Sheet revision DS279PP3 dated APR '99)

1. Power Supply Rejection PSRR (x10 gain ranges)

Specified 70 dB at Gains x10 and x50

New Spec. 56 dB at Gain x10 and 70 dB at Gain x50

Comments The CS5460 Data Sheet will be revised to indicate the different PSRR at the different gain settings.

2. CPUCLK Duty Cycle

Specified No specification.

New Spec. To maintain a 40% to 60% duty cycle on CPUCLK, a 45% to 55% duty cycle from an external clock is required.

Comments The CS5460 Data Sheet will be revised to indicate this requirement.

3. IEC Compliance

Specified The CS5460 complies with IEC 521/1036.

New Spec. The CS5460 complies with IEC 687/1036.

Comments The CS5460 Data Sheet will be revised to indicate the correct compliance.

4. SCLK High-level and Low-level Input Voltages, Respectively

Specified 0.6 VD+ Minimum and 0.3 VD+ Maximum, respectively.

New Spec. 0.8 VD+ Minimum and 0.2 VD+ Maximum, respectively.

Comments The CS5460 Data Sheet will be revised to indicate the correct limits.

5. Voltage Channel Noise (Referred to Input)

Specified 250 µV Maximum

Rev. A 350 µV Maximum

Comments The CS5460 will meet this specification in future revisions. The Current Channel has over 90% of the noise budget for the low-rate measurements and, therefore, the impact of the Voltage Channel noise will be virtually unnoticed in Energy and V_{RMS} measurements.

6. V_{RMS} and I_{RMS} Calculations overflow

Specified Internal Registers in the Power Calculation Engine should have enough range with maximum inputs and cycle count, N = 4000.

Rev. A V_{RMS} and I_{RMS} Internal Registers overflow when inputs exceed 50% of full-scale and N = 4000.

Comments The CS5460 will meet this specification in future revisions. When setting N = 4000, the gain calibration registers can be set to 0.5 to prevent overflow. RMS values of 0.5 will represent a full-scale input. This has minimal impact on accuracy or dynamic range.

7. Power Supply Configuration VA = ±2.5V; VD+ = +3V; DGND = 0V

Specified Internal or external clock.

Rev. A Internal clock mode only for supply configuration VA = ±2.5V; VD+ = +3V; DGND = 0V.

Comments The CS5460 will meet this specification in future revisions. External clock can be used with VA+ = +3V; VA- = –2V; VD+ = +3V; DGND = 0V.

8. Power Consumption in Sleep Mode

Specified 10 µW Typical

Rev. A 15 µW Typical and 50 µW Maximum

Comments The CS5460 will meet this specification in future revisions.

9. Internal Reference Temperature Coefficient

Specified 60 ppm/°C

Rev. A 100 ppm/°C

Comments The CS5460 will meet this specification in future revisions.

10. VREFOUT Load Regulation

Specified 6 mV Typical and 10 mV Maximum

Rev. A 8 mV Typical and 12 mV Maximum

Comments The CS5460 will meet this specification in future revisions.

If there are any questions concerning this information, please contact the Crystal Power Measurement team. For questions contact any of the team members or send email to powermeter@crystal.cirrus.com. Visit our web site http://www.crystal.com or call our literature department at +1 (800) 888-5016 ext. 3594 or +1 (512) 912-3594 for data sheets and application notes.

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