08/24/99

Errata: CS4341 Rev. B

CS4341 24-Bit, 96 kHz Stereo DAC with Volume Control

All references to the CS4341 mentioned below shall be taken to refer to revision B of the CS4341 product. The hardware revision code can be found in the 10 character field printed below the part number on each chip. The letter which appears as the fifth character from the right is the revision code (e.g. ZNAXYB9846 is a Revision B part).

Pin 6 (SCL/CCLK) of the CS4341 does not have sufficient hysteresis to meet the data sheet rise time specifications. The I^2C rise time t_r and the SPI rise time t_{r2} must be less than 30 ns for proper operation. This prevents the use of standard I^2C configurations with a resistor pull-up. This problem can be worked around by placing a Schmitt Trigger buffer, for example a 74HC14, on the SCL line just prior to the CS4341. This will not affect the operation of the I^2C bus as pin 6 is an input only.

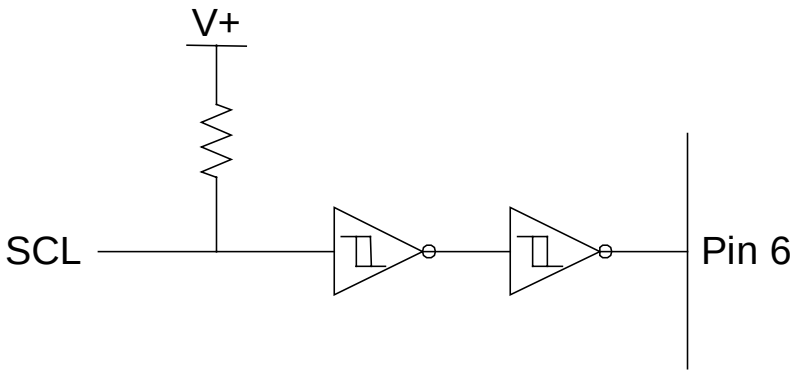

Figure 1. I^2C SCL Buffer Example

If there are any questions concerning this information,
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