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Errata: CS4294 Rev. E

(Reference CS4294 Data Sheet revision FEB '00 DS326PP4)

1. During PR4 powerdown, the rising edge of RESET# will always be interpreted as a cold reset, regardless of the state of the CRST bit before entering PR4. The new warm reset behavior, outlined in section D.4.3.1 of the AC '97 specification revision 2.1, is not supported in revision E of the chip. Therefore, if the power management controller attempts to wake up the codec in response to a GPIO event, it will be impossible to determine which GPIO pin caused the wakeup event since the GPIO Pin Status Register (Index 54h) will be reset to its default state following the cold reset. Furthermore, following a $D3_{cold}$ state, the codec context will be lost and must be fully restored by the controller before normal operation can resume.

2. The CS4294 requires a minimum SYNC pulse width of 1.13 µs in the absence of BIT_CLK for a warm reset to occur. AC '97 version 2.1 requires SYNC to be asserted for a minimum of only 1.0 µs.

   Note: this requirement refers to the behavior of SYNC during warm reset only. During normal operation, SYNC is asserted for the entire period of slot 0 (the tag phase) which is 16 cycles of BIT_CLK.

If there are any questions concerning this information,
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