6/2/00

# Errata: EP7209 Rev D

EP7209 Ultra Low Power Audio Decoder System-on-Chip (DS453PP2, DEC '99)

1) LRCLK Duty Cycle

**Description:** LRCLK is not a 50% duty cycle clock, the actual duty cycle of LRCLK is 63/128% low and 65/128% high. Data is aligned with LRCLK.

**Workaround:** None, Data is aligned with LRCLK, many standard ADC and DACs (CS43L40, CS43L42, CS43L43, and CS53L32) align data with LRCLK. Verify that the CODEC used aligns with LRCLK and does not require a 50% duty cycle.

2 DAI Input Timing

**Description:** When receiving data via the DAI port, the device will capture data one clock prior to LRCLK falling.

**Workaround:**

A) Perform a single bit left shift on the Right Channel Data (when LRCLK is low). The result will be 15 bits of valid data.

B) If interfacing with a CS53L32 ADC, the CS53L32 presents a zero followed by valid data after the rising edge of LRCLK. Once the data has been captured, a single bit left shift for both Left and Right Channel Data will provide 15 valid bits of data from the ADC.

3 SSI1 port operation

**Description:**, The SSI1 port will transmit incorrect data if bits 4:7 form an even number and bits 0:3 are **not** equal to 0xF. For example 0x12 will cause an error, but the values 0x1F and 0x22 will not cause an error.

**Workaround:** The SSI1 port can be used for receiving data with no errors. If transmitting data, avoid the condition in the Description above. Alternatively, you can use SSI1 in Extended mode.

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4 nURESET Operation

**Description:** If nURESET is asserted before the processor is operating after a wakeup from Standby mode, the system will enter into an unknown state. When this occurs, the only recovery is to assert the nPOR.

Workarounds:

A) Do not use the nURESET signal. Tie the nURESET to $V_{dd}$.

B) If nURESET must be used, make certain that it cannot be asserted until after the processor is running. It is necessary to gate uRESET with a run condition flag, which could be a GPIO pin that is asserted via software, or a Flip-Flop that is set from an external chip select such as nCSx. Under no circumstances should the RUN signal be used. The RUN signal goes high approximately 128 uS after WAKEUP is asserted. Instructions are not fetched from external ROM (nCS0) until approximately 150 ms to 350 ms after WAKEUP.

5 FASTWAKE operation:

**Description:** The FASTWAKE feature does not meet the performance described in the data sheet. When the FASTWAKE bit of SYSCON3 is set, the EP7209 runs at 256 Hz for approximately 10 instructions or approximately 39 ms after the processor speed is increased to 36 MHz.

**Workaround:** There is no workaround; therefore, the FASTWAKE feature is being removed from the data sheet.

For any questions regarding this Errata, please send email to: epdapps@crystal.cirrus.com