Errata: CS4392 Data Sheet revision DS459PP1 dated OCT '00

The following is a correction to the CS4392 Datasheet revision DS459PP1, OCT'00. These changes will occur in the next revision of the datasheet.

- The chip ID register (07 h) is a reserved register.
- There is an internal 100 Ohm source impedance for the four analog output pins AOUTA+, AOUTA-, AOUTB+, and AOUTB-. This source impedance must be taken under consideration when designing the output filter such that the full-scale output level is not attenuated below the desired level.
- By design, the DSD frequency response is +0, -0.1 dB from 20Hz to 20kHz and the -3dB corner frequency is 120kHz (for Fs = 64x 44.1kHz).
- The group delay specifications are as follows (note: filter response is not tested but guaranteed by design):

	Fast Roll - Off		Slow Roll -Off		Unit
	Typical	Max	Typical	Max	
Single speed mode					
Group Delay	12/Fs	-	6.5/Fs	-	s
Passband Group Delay Deviation 0 to 20 kHz	-	±0.41/Fs	-	±0.14/Fs	s
Double Speed Mode					
Group Delay	4.6/Fs	-	3.9/Fs	-	s
Passband Group Delay Deviation 0 to 20 kHz	-	±0.03/Fs	-	±0.01/Fs	s
Quad Speed Mode					
Group Delay	4.7/Fs	-	4.2/Fs	-	s
Passband Group Delay Deviation 0 to 20 kHz	-	±0.01/Fs	-	±0.01/Fs	s

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