05/12/00

# *Errata: CS8427-CS Rev. A Performance Update*

(Reference CS8427 Data Sheet revision DS477PP1 dated Nov '99)

1. On page 9 of the data sheet it is specified that in I2C mode, SCL and SDA have a maximum rise time of 1 µS and a maximum fall time of 300 nS. The actual rise and fall times should be less than 25 nS.

2. On page 7 it is specified that the Serial Audio Ports are capable of receiving or transmitting data in slave mode at 27 MHz, if the necessary setup timing is observed. This is true as long as an additional condition is observed. There may be no more that 128 SCLK cycles per frame. This means a high-speed burst clock can be used for SCLK, but a high-speed continuous clock cannot.

3. On page 7 of the data sheet, Figure 1 shows OSCLK, OLRCK, ISCLK, and ILRCK, in master mode, being clocked from the rising edge of RMCK. They are actually clocked from the falling edge of RMCK. When the same signals are derived from OMCK they are clocked from the rising edge

4. On page 6 of the data sheet the RMS cycle to cycle jitter of the received master clock is specified as less than 200 pS. This is correct when operating the part at a sample rate of 50 kHz or less. Above 50 kHz, the jitter performance deteriorates. This can have a significant impact on performance when the part is coupled to a D/A converter with a dynamic range of 105 dB or more.

If there are any questions concerning this information,
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