



## Errata: CS43L42 Rev. D

CS43L42 Low Voltage, Stereo DAC with Headphone Amp

All references to the CS43L42 mentioned below shall be taken to refer to revision D of the CS43L42 product. The hardware revision code can be found in the 10-character field printed below the part number on each chip. The letter which appears as the fifth character from the right is the revision code (e.g. ZNACSD9926 is a Revision D part).

- The PopGuard<sup>©</sup> Transient Control does not function properly and will produce audible artifacts on the headphone and line outputs during power-up. A hardware fix is available for this issue. Please see Figures 1 and 2 for the headphone output fix. For the line outputs, please use the optional mute circuit shown in the CDB43L42 schematic to mask this problem.
- The PopGuard<sup>©</sup> Transient Control power-down ramp requires 5 seconds to prevent audible artifacts on the headphone outputs at the next power-up. A hardware fix is available for this issue, see Figures 1 and 2 for details. This fix will reduce the ramp down time to approximately 300 milliseconds.
- The headphone outputs clip when the value of VA\_HP is below VA. It is recommended that these two supplies be tied together.
- The Peak Signal Limiter is not functional.
- When the Analog Headphone Attenuation Control registers (02h and 03h) are set for attenuation levels greater than -10 dB, the actual attenuation deviates from the register setting by more than 1 dB.





The Motorola MOSFETs shown have been tested to work properly, however, an equivalent device may be used.

Figure 1. Pop Guard Fix

low Ron (3 ohms or less).





Figure 2. Timing for Pop Guard Fix

If there are any questions concerning this information, please contact Applications Engineering at 512-445-7222.