CL-PS7111 Development Kit

Hardware User's Guide

Embedded Processors Division

This document describes the CL-PS7111 development board provided by Cirrus Logic Inc. No warranty is given for the suitability of this design for any purpose other than demonstrating functional operation of the CL-PS7111. The information contained in this document is subject to change without notice.

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1 Introduction

This document defines the baseline board-level hardware elements that comprise the CL-PS7111 development board. This document references other documents that contain more specific details of processors and other devices (ICs) used on the design. Scope is restricted to covering the printed circuit board, connections between components on that board, and between the board and external devices that connect to the development board.

2 Terms and Definitions

- ARM® Advanced RISC Machines Limited. The company that developed the ARM710a processor core.
- BPS Bits per second.
- bpp Bits per pixel.
- Codec Coder/decoder.
- COM1 Serial port #1 on the development board.
- COM2 Serial port #2 on the development board.
- DCD Data carrier detect.
- DMA Direct Memory Access.
- DRAM Dynamic Random Access Memory.
- EDO Extended Data Output. A more efficient means of DRAM data access than FPM.
- FIFO First In First Out. A memory block where data is read out from a single location in the exact sequence in which it was written.
- FLASH A type of non-volatile memory.
- FPM Fast Page Mode. Method of DRAM data access.
- GPIO General-purpose input/output.
- IrDA Infrared Data Association. This body sets the standard for infrared communication.
- JTAG Joint Test Action Group.
- LCD Liquid Crystal Display.
- PWM Pulse width modulation.
- RI Ring indicator.
- RTC Real-time clock.
- RTS Ready to send.
- SSI Synchronous Serials Interface.
- UART Universal Asynchronous Receiver Transmitter.

The prefix of a lower case 'n' to a signal name denotes that the signal is active low.

All numbers found within this document are decimal, unless otherwise stated. Hexadecimal numbers are preceded with '0x' and a colon (:) splits a 32-bit number to improve readability. Binary numbers are followed by a 'b' as shown below:

0x8000:02C0	-	Hex number
00110101b	-	Binary number

The symbol x within a binary number represents a "don't care".

3 Development Board

The development board is designed as a prototype with limited debug capabilities, including test headers for logic analyzer interfacing.

3.1 Main Feature Set

The development board has the following features:

- Microprocessor
  - CL-PS7111 processor running at 18.432MHz

- Memory
  - 16Mbytes of zero wait-state EDO DRAM memory
  - 16MBytes of two wait-state FLASH memory

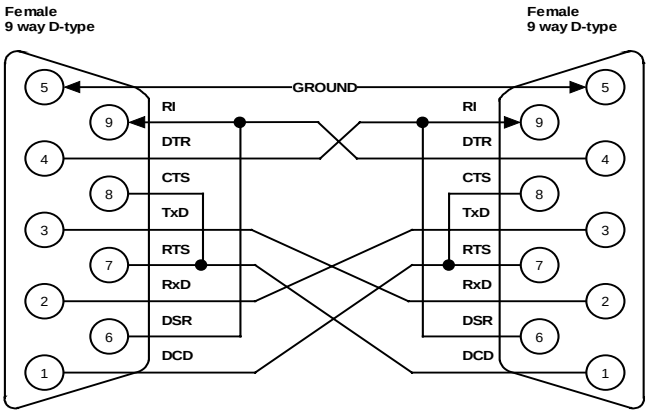
- Peripherals
  - Monochrome 640x240 LCD, 16 gray shades
  - Touch screen digitizer
  - ASCII keyboard, 83 keys
  - Six user key switches
  - 12-way keypad connector
  - Two serial ports
  - Primary serial interface may be switched between RS-232 and IrDA
  - Analog to digital converter, 10 bit 8 channels
  - DC-DC converters
  - CS8900A 10-BaseT Ethernet interface
  - Power management switches
  - PC Card V2.01 compliant interface
  - Audio CODEC
  - On-board speaker amplifier
  - Microphone input supporting standard PC external microphones
  - SSI interface
  - Power supply
  - Logic analyzer connectors
  - I/O expansion connector
  - Debug area

3.2 Board Set-up

A null modem cable is supplied to allow communication between the development board and the host PC. Communication is setup by connecting UART2 of the development board to any available COM port on the host PC.

Note: Null model cables differ substantially from a straight-through cable. See Figure 1 below:

Figure 1: Null Modem Cable



3.3 Power

A 12V 500mA AC adapter is provided to plug into the board via a connector labeled EXT DC. The adapter plugs into J9.

3.4 Jumpers

There are four jumpers on the development board. Their functions are summarized below:

JP2: Boot enable. This jumper is switch between booting from the internal boot ROM and the external FLASH. The board will boot from the external FLASH when this jumper is not shunted (normal operation).

JP4: Disable UART2. This jumper is used to disable the RS-232 line driver on UART2. The driver will be enabled when this jumper is not shunted (default configuration).

JP9: Codec operation. This jumper is used to select between A-Law and μ-Law operation of the codec. The codec will operate on A-Law samples when this jumper is not shunted (default configuration).

JP18: CL-PS6700 interrupt enable. This jumper is used to enable the CL-PS6700 interrupt to the CL-PS7111. The interrupt is not connected when this jumper is not shunted (default configuration).

3.5 Headers

Following are the header assignments:

JP5: Microphone - Used to provide a microphone input to the codec.

JP7: TTL UART2 - Provides the TTL level Rx and Tx signals from UART2.

JP8: A-D In - Used to provide an input signal to channel 0 of the ADC.

JP10: Logic analyzer - HP-compatible logic analyzer header containing the memory control signals.

JP11: Touch-screen input - Used for connecting to a 4-wire touch-screen interface.

JP12: Generic LCD - Used for connecting an external LCD interface board.

JP13: SSI - Used for connecting an external SSI interface board.

JP14: UART1 DTR - Used to control the UART1 DTR signal.

JP15: Expansion header - Used for connecting an external I/O interface board.

JP16: 3X4 keyboard - Used for connecting a 12-way keypad.

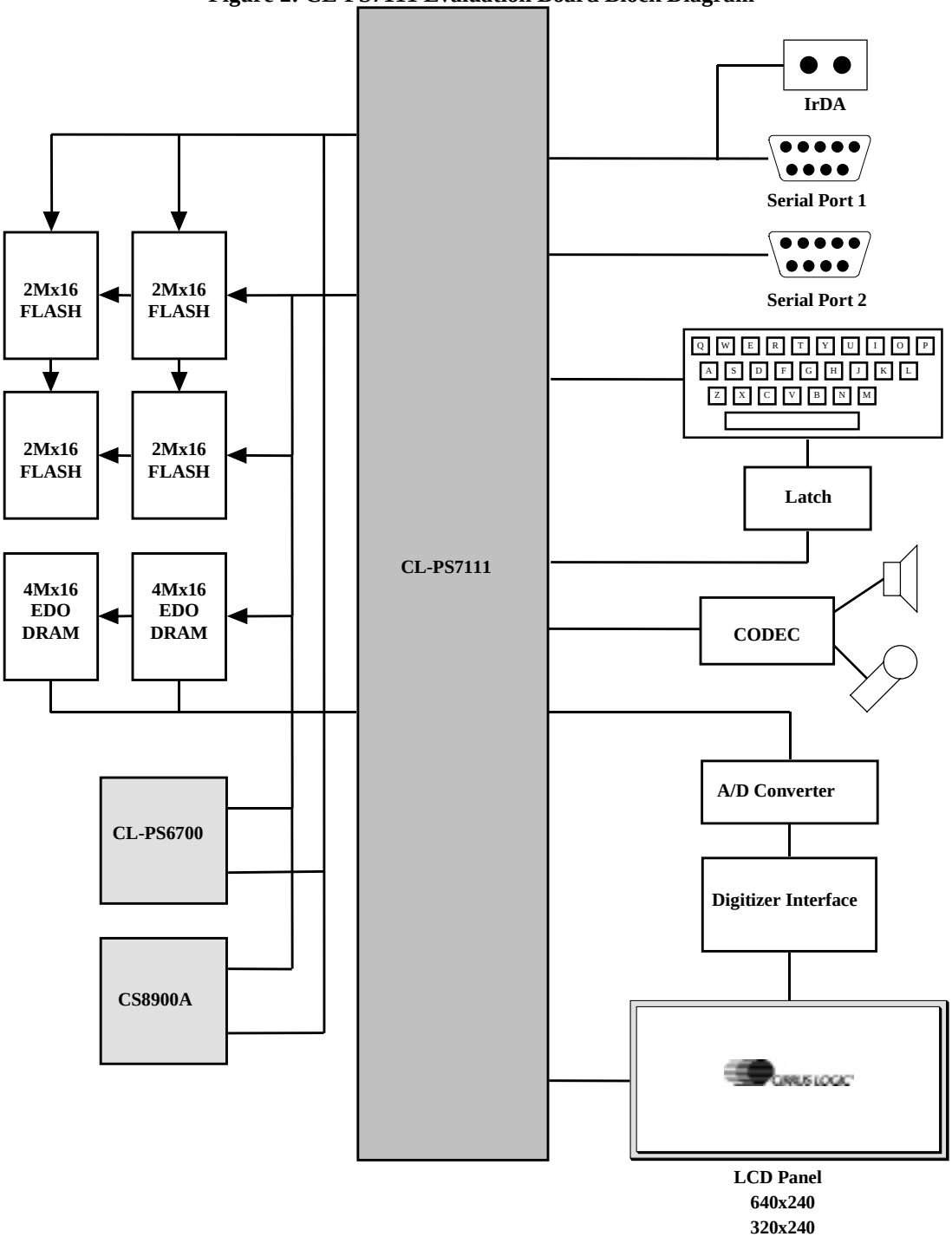
JP17: ASCII keyboard - Used for connecting the supplied ASCII keyboard.

JP19-JP22: Logic analyzer - HP-compatible logic analyzer header containing the address and data buses.

4 Hardware Design Details

Figure 2 shows a block diagram of the development board.

Figure 2: CL-PS7111 Evaluation Board Block Diagram



4.1 Memory Map

Table 1: Memory Map

Physical Address Space	*Description*	*Decode*
0x0000.0000 – 0x007F.FFFF	FLASH bank 0, 8MB	nCS0
0x1000.0000 – 0x107F.FFFF	FLASH bank 1, 8MB	nCS1
0x2000.0000 – 0x2FFF.FFFF	CS8900A Ethernet	nCS2
0x3000.0000 – 0x3FFF.FFFF	Keyboard row latch	nCS3
0x4000.0000 – 0x43FF.FFFF	CL-PS6700 attribute memory	nCS4
0x4400.0000 – 0x47FF.FFFF	CL-PS6700 common memory	nCS4
0x4800.0000 – 0x4BFF.FFFF	CL-PS6700 I/O memory	nCS4
0x4C00.0000 – 0x4FFF.FFFF	CL-PS6700 registers	nCS4
0x5000.0000 – 0x5FFF.FFFF	Expansion	nCS5
0x6000.0000 – 0x6000.07FF	On-chip SRAM, 2KB	nCS6
0x7000.0000 – 0x7000.007F	On-chip boot code, 128B	nCS7
0x8000.0000 – 0x8000.1800	CL-PS7111 registers	
0xC000.0000 – 0xC07F.FFFF	DRAM, 8MB	
0xC100.0000 – 0xC17F.FFFF	DRAM, 8MB	

4.2 GPIO Assignment

Table 2: GPIO Assignment

Port	*Reset State*	*Signal*	*I/0*	*Description*
PA(0-7)	Input	PA(0-7)	I	Keyboard Row Data
PB0	Input	PRDY	I	CL-PS6700 PRDY
PB1	Input	PB1_RTS	O	Sets UART1 RTS
PB2	Input	PB2_RI	I	Returns UART1 RI
PB3	Input	PB3_SPARE	O	Spare GPIO
PB4	Input	PB4_PXEN	O	Enable Digitizer TSPX
PB5	Input	PB5_MXEN	O	Enable Digitizer TSMX
PB6	Input	PB6_PYEN	O	Enable Digitizer TSPY
PB7	Input	PB7_MYEN	O	Enable Digitizer TSMY
PD0	Output – low	PD0_DIAG	O	Diagnostic LED
PD1	Output – low	PD1_LCD_DC-DC	O	Enable LCD DC-DC converter
PD2	Output – low	PD2_LCDEN	O	Enable LCD Display
PD3	Output – low	PD3_LCDBL	O	Enable LCD Backlight
PD(4-7)	Output – low	PD(4-7)_VEE	O	VEE Level Control
PE0	Input	PE0_CODECEN	O	Audio Codec Control =0, disable Codec =1, enable Codec
PE1	Input	PE1_5VEN	O	PCMCIA Voltage Vpc =0, enable +5v =1, disable
PE2	Input	PE2_ADCEN	O	A/D Converter Control =0, disable A/D =1, enable A/D

4.3 Interrupt Assignment

Table 3: Interrupt Assignment

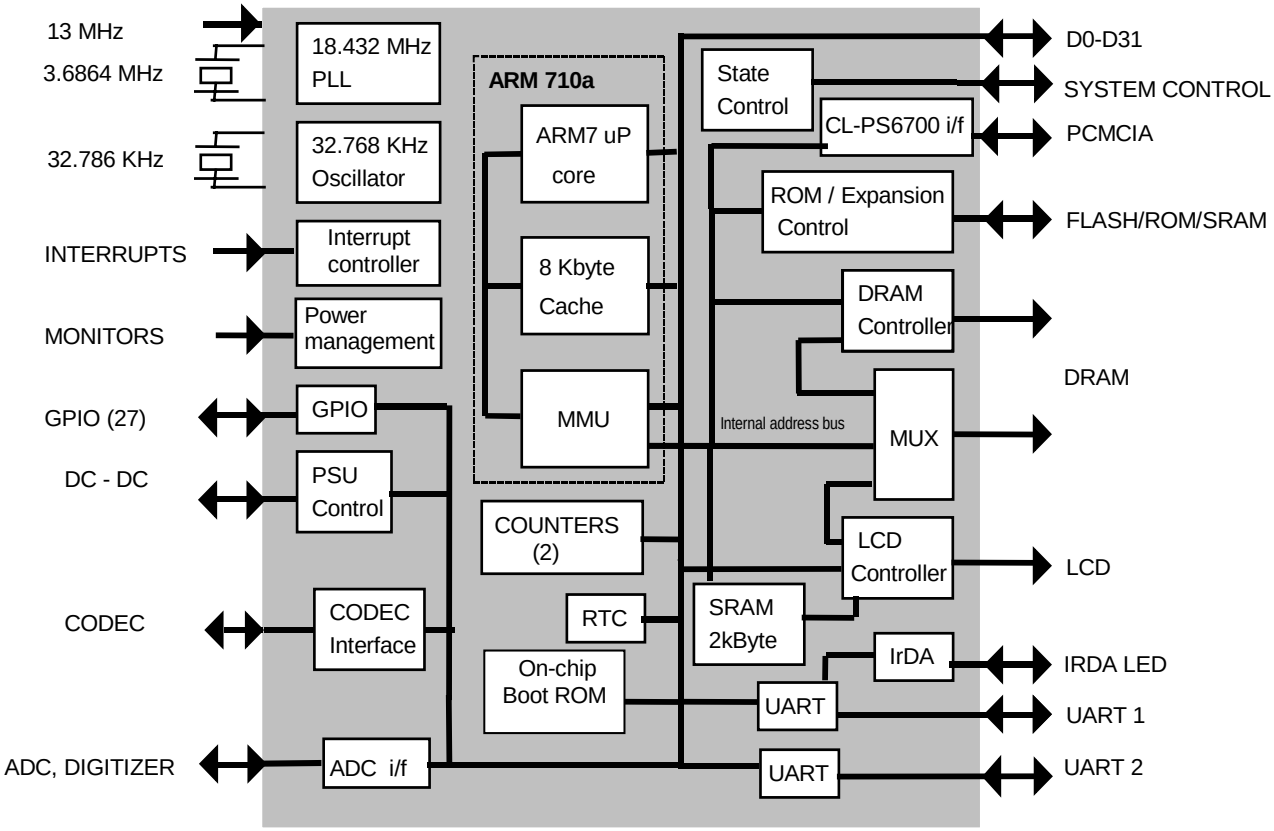
CL-PS7111 Pin	*Signal*	*Description*
nEXTFIQ	-EXTFIQ	• CL-PS6700 interrupt request, or • Expansion interrupt request, or • External SSI interrupt request
nEINT1	-EINT1	CL-PS6700 interrupt request
nEINT2	-EINT2	Touch-screen interrupt request
EINT3	EINT3	CS8900A interrupt request

For internal interrupts consult the CL-PS7111 data book.

4.4 CL-PS7111 Processor

The CL-PS7111 contains an ARM 32-bit RISC microcontroller and a wide range of on-chip peripherals. The core of the CL-PS7111 is designed with an ARM710a processor unit comprised of an ARM7 microprocessor, MMU, and 8Kbytes of 4-way set associative cache. The CL-PS7111 is a 3.3V device running at 18.432Mhz. This creates performance levels equivalent to 15 MIPS with a maximum power consumption of 66mW. An internal functional block diagram is shown in Figure 3.

Figure 3: Internal Functional Block Diagram



4.5 DRAM

The 16MB DRAM memory is a single 32-bit bank with an access time of 60ns. This bank is implemented using a pair of 4Mx16 EDO chips. Although EDO memory cycles are not implemented by the CL-PS7111, this type of memory is used because of its availability and future considerations for this design.

4.6 FLASH

The FLASH memory is provided in two banks, 8Mbytes of 32 bit wide devices in each bank. Both banks are designed using two 32Mbit Intel Boot Block devices with an access time of 110ns. The CL-PS7111 is programmed for 2 wait-state operation in this memory space.

4.7 Clocks

The CL-PS7111 requires the main system clock and the real-time clock for normal operation. The real-time clock oscillates at a frequency of 32.768KHz and provides the time-base for the integrated real-time clock.

There are two possible options for the main processor clock. The first, and most typical, is to drive the clock from a 3.6864MHz crystal connected to the master oscillator pins. Alternatively, the clock may be driven directly from a crystal oscillator module. The maximum frequency for this clock is 13MHz.

By default, the board uses the 3.6864MHz crystal. To configure the board so that the CL-PS7111 can be driven from a 13MHz oscillator, remove the following components from the board:

X2 - 3.6864MHz crystal
R103 - 10K 0805 resistor

Replace the above with the following components:

U3 - 13MHz oscillator (3.3V)
R102 - 10K 0805 resistor

4.8 Power Management Modes

The power management modes enable complete control of the system power consumption. While the development board does not actually implement the power management features, it does provide access to the power management signals. This allows the operation of power management to be tested and verified.

The four signals that control the power management are:

1) BATOK

   When active, it simulates a battery fail condition. A falling edge on BATOK signal generates a FIQ. The CL-PS7111 only transitions to the operating state if both BATOK and nPWRFL are inactive.

2) nBATCHG

   When active, it simulates a 'no battery' condition, or battery voltage has fallen below operating threshold.

3) nPWRFL

   When active, it simulates a power fail condition. Active low on this signal will force a transition to the standby state.

4) nEXTPWR

   This switch must be active when external power is applied.

The CL-PS7111 supports the following three power states:

1) Operating

   All functions and integrated peripherals of the CL-PS7111 are running.

2) Standby

   Standby state effectively turns off the CL-PS7111. The 18.432MHz PLL is turned off, there is no display, and the internal peripherals are off. The RTC is active, and all system states and memory contents are maintained (DRAM is placed in self-refresh mode). The RUN signal is driven low.

   Standby state is entered when power is applied or a system reset is activated.

3) Idle

   Similar to the operating state except that the processor clock is turned off (PLL is still active).

Table 4 lists the status of the CL-PS7111 peripherals in the different power states.

Table 4: Peripheral Power States

Function	*Operating*	*Standby*	*Idle*	*nPOR Reset*	*nuReset*
CPU	On	Off	Off	Reset	Reset
PLL/CLKEN	On	Off	On	Off	Off
DRAM Ctrl	On	Self Refresh	On	Off	Self Refresh
UARTs	On	Off	On	Reset	Reset
RTC	On	On	On	On	On
TIMERS	On	Off	On	Reset	Reset
LCD	On	Off	On	Reset	Reset
ADC I/F	On	Off	On	Reset	Reset
CODEC I/F	On	Off	On	Reset	Reset
PIC	On	On	On	Reset	Reset
DC – DC	On	Off	On	Reset	Reset

4.9 Reset

There are three asynchronous reset signals supported by the CL-PS7111: nPOR, nURESET and nPWRFL.

nPOR is the initial reset signal that is activated only when power is first applied to the board. The development board implements this signal with a simple resistor and capacitor network with a time constant of approximately 10mS.

nURESET is a user reset that allows the system to be initialized by either an external event such as a watchdog timeout or a user reset. The development board implements only the user reset option by using a momentary switch labeled URESET located at the front of the board.

nPWRFL is an active low input signal to the CL-PS7111 that indicates a power failure. This signal, when active, will generate an internal reset and place the CL-PS7111 into standby state. A switch labeled PWFRL generates it.

4.10 Wakeup

Once the CL-PS7111 has been reset, it enters the standby state. The transition from the standby state to the operating state is triggered by the rising edge of the WAKEUP signal using a momentary switch labeled WAKEUP located at the front of the board.

4.11 Logic Analyzer Headers

Four, 20-way headers allow a logic analyzer to be connected to the board for debug and software analysis. The pin-outs for the headers are shown in the following tables.

Table 5: JP10 Logic Analyzer Header Definition

Description	#	#	*Description*
No Connection	1	2	No Connection
EXPCLK (expansion bus clock)	3	4	EXPCLK (expansion bus clock)
No Connection	5	6	No Connection
No Connection	7	8	No Connection
No Connection	9	10	nCS4 (processor chip select)
nCS0 (processor chip select)	11	12	nMOE (memory output enable)
nMWE (memory write enable)	13	14	nCAS3 (DRAM CAS)
nCAS2 (DRAM CAS)	15	16	nCAS1 (DRAM CAS)
nCAS0 (DRAM CAS)	17	18	nRAS1 (DRAM RAS)
nRAS0 (DRAM RAS)	19	20	Ground

Table 6: JP19 Logic Analyzer Header Definition

Description	#	#	*Description*
No Connection	1	2	No Connection
No Connection	3	4	D15 (processor data)
D14 (processor data)	5	6	D13 (processor data)
D12 (processor data)	7	8	D11 (processor data)
D10 (processor data)	9	10	D9 (processor data)
D8 (processor data)	11	12	D7 (processor data)
D6 (processor data)	13	14	D5 (processor data)
D4 (processor data)	15	16	D3 (processor data)
D2 (processor data)	17	18	D1 (processor data)
D0 (processor data)	19	20	Ground

Table 7: JP20 Logic Analyzer Header Definition

Description	#	#	*Description*
No Connection	1	2	No Connection
No Connection	3	4	No Connection
No Connection	5	6	No Connection
No Connection	7	8	A27 (processor address)
A26 (processor address)	9	10	A25 (processor address)
A24 (processor address)	11	12	A23 (processor address)
A22 (processor address)	13	14	A21 (processor address)
A20 (processor address)	15	16	A19 (processor address)
A18 (processor address)	17	18	A17 (processor address)
A16 (processor address)	19	20	Ground

Table 8: JP21 Logic Analyzer Header Definition

Description	#	#	*Description*
No Connection	1	2	No Connection
No Connection	3	4	A15 (processor address)
A14 (processor address)	5	6	A13 (processor address)
A12 (processor address)	7	8	A11 (processor address)
A10 (processor address)	9	10	A9 (processor address)
A8 (processor address)	11	12	A7 (processor address)
A6 (processor address)	13	14	A5 (processor address)
A4 (processor address)	15	16	A3 (processor address)
A2 (processor address)	17	18	A1 (processor address)
A0 (processor address)	19	20	Ground

Table 9: JP22 Logic Analyzer Header Definition

Description	#	#	*Description*
No Connection	1	2	No Connection
No Connection	3	4	D31 (processor data)
D30 (processor data)	5	6	D29 (processor data)
D28 (processor data)	7	8	D27 (processor data)
D26 (processor data)	9	10	D25 (processor data)
D24 (processor data)	11	12	D23 (processor data)
D22 (processor data)	13	14	D21 (processor data)
D20 (processor data)	15	16	D19 (processor data)
D18 (processor data)	17	18	D17 (processor data)
D16 (processor data)	19	20	Ground

4.12 Expansion Interface

The expansion interface is intended to support the addition of small add-on boards. Its features include:

- 8-bit data
- 4-bit address. This allows for 16 discrete I/O locations
- Fully decoded chip select (0x5000:0000 – 0x5FFF:FFFF)
- Output enable and write enable strobes
- Interrupt to the CL-PS7111
- GPIO bit from the CL-PS7111
- Power

Table 10: Expansion Interface

Description	#	#	*Description*
DO	1	2	VDD (3.3V)
D1	3	4	A0
D2	5	6	A1
D3	7	8	A2
D4	9	10	A3
D5	11	12	nMWE (write enable)
D6	13	14	nEXTFIQ (interrupt)
D7	15	16	PB3 (GPIO)
nCS5 (chip select)	17	18	GND
nMOE (output enable)	19	20	GND

Note that the interface is 3.3V only.

4.13 Keyboard

There are a number of keyboard options.

4.13.1 QWERTY Keyboard

This is a full function 83-key QWERTY keyboard connected to the board by the connector labeled ASCII keyboard, located at the front. The CL-PS7111 only supports the direct scanning of 64 keys. To allow all the keys to be scanned an additional 8-bit port has been added to the development board design.

The additional port is decoded by nCS3, and is the only device enabled in this address range. Because the port will alias the entire addressing range of the nCS3 memory region, it is strongly recommended that only the first appearance of this port be used. The memory location of this 8bit port is 0x3000:0000.

The table below shows a complete scan bit and port bit mapping for this keyboard:

Table 11: Keyboard Scan Codes

Key Name	*Column*	*Port*
Esc	0	A0
F1	5	A0
F2	4	A0
F3	3	A0
F4	2	A0
F5	1	A0
F6	6	A0
F7	7	A0
F8	7	Ext1
F9	6	Ext1
F10	1	Ext1
Num Lock	2	Ext1
Prt Sc	3	Ext1
Scroll Lock	4	Ext1
Break	5	Ext1
1	0	A1
2	5	A1
3	4	A1
4	3	A1
5	2	A1
6	1	A1
7	6	A1
8	7	A1
9	7	Ext0
0	6	Ext0
-	1	Ext0
=	2	Ext0
Back Space	3	Ext0

Key Name	*Column*	*Port*
Home	5	Ext0
Tab	0	A2
Q	5	A2
W	4	A2
E	3	A2
R	2	A2
T	1	A2
Y	6	A2
U	7	A2
I	7	A7
O	6	A7
P	1	A7
[	2	A7
]	3	A7
#	4	A7
Pg Up	5	A7
Caps Lock	0	A3
A	5	A3
S	4	A3
D	3	A3
F	2	A3
G	1	A3
H	6	A3
J	7	A3
K	7	A6
L	6	A6
;	1	A6
‘	2	A6

Key Name	*Column*	*Port*
Enter	4	A6
Pg Dn	5	A6
Shift	0	Ext2
Z	5	A4
X	4	A4
C	3	A4
V	2	A4
B	1	A4
N	6	A4
M	7	A4
,	7	A5
.	6	A5
/	1	A5
Shift	0	Ext7
Arrow Up	0	A7
End	5	A5
Ctrl	0	Ext3
Fn	0	Ext4
Alt	0	Ext5
\	0	A4
Space Bar	0	A5
Alt Gr	0	Ext6
Ins	3	A5
Del	2	A5
Left Arrow	0	A6
Down Arrow	0	Ext0
Right Arrow	0	Ext1

When performing a keyboard matrix scan, software must drive a column and then read both the row on GPIO port A and the extended row register at location 0x3000:0000.

4.13.2 12-Way Keyboard

The 12-way keyboard is equivalent to a telephone keypad. It consists of keys labeled 0-9, *, and #. This keyboard is supported without the additional keyboard port and cannot be used if the ASCII keyboard is connected. The key mapping is shown in the following table:

Table 12: 12 Way Keypad

	Row		
Column	*0*	*1*	*2*
0	1	2	3
1	4	5	6
2	7	8	9
3	*	0	#

4.13.3 Board Mounted Switches

There are six switches labeled USER1-USER6 mounted on the development board to provide general-purpose inputs when neither of the keyboards are used, or as a compliment to the 12-way keyboard. When the QWERTY keyboard is used, these switches are in parallel with 6 of the switches on the keyboard; therefore, it is suggested that these switches not be used when the QWERTY keyboard is in use.

The table below shows the mapping of these keys:

Table 13: Key Switches

	User1	*User 2*	*User 3*	*User 4*	*User 5*	*User 6*
Column	5	5	5	5	5	5
Row	0	1	2	3	4	5

4.14 Analog to Digital Converter

The analog to digital converter used on the development board is a Maxim MAX148, 10bit, 8 channel converter with a maximum sample rate of 133kbps. It connects to the CL-PS7111 through its integrated SSI interface and performs conversions for the touch-screen interface, on-board voltage monitoring, and an external analog input.

4.14.1 Digitizer

The digitizer on the development board is a simple four-wire version that allows for the use of a two-plate resistive touch screen digitizer.

Each terminal of the x-plate and y-plate are connected to a transistor that allows the terminal to be connected to a supply rail. This means that each plate can be biased between 3.3V and 0V. A potential divider is formed when the user makes contact between the two plates by pressing on the screen. The output voltage is measured by the analog to digital converter and is proportional to the position pressed.

The table below shows the mapping of the analog to digital channels used for the digitizer:

Table 14: Digitizer Definitions

Signal Name	*Plate Terminal*	*Enable Control*	*Active State*	*Voltage*	*A/D Channel*
TSPY	Y upper	Port B6	Low (0)	3.3V	Channel 7
TSPX	X left	Port B4	Low (0)	3.3V	Channel 4
TSMY	Y lower	Port B7	High (1)	0V	Channel 5
TSMX	X right	Port B5	High (1)	0V	Channel 6

4.14.2 Generic Channels

Four channels of the analog to digital converter are implemented as show in the following table:

Table 15: Generic Analog to Digital Channels

A/D Channel	*Function*	*Description*
0	General Purpose	Connected to jumper JP8. General purpose input
1	Potentiometer	Connected to VR1 reading 0V to 3.3V
2	VDD	Connected to VDD through a potential divider
3	VREF	Connected to VREF through a potential divider

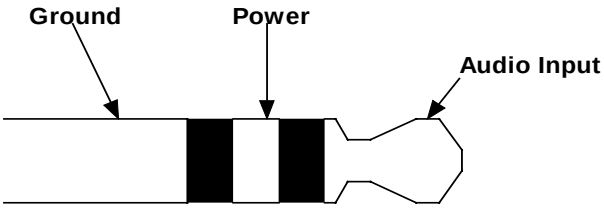
Care should be taken when applying a signal to JP8. The voltage is not protected and should not exceed 3.3V.

4.15 Audio

The CL-PS7111 integrates a FIFO buffered CODEC interface. The interface is designed to support 8-bit, mono audio input and output at a sampling frequency of 8KHz. The development board incorporates an 8-bit telephony CODEC, the OKI MSM7702-01, for the recording and playback of audio samples.

The CODEC may be configured to support either u-law or A-law operation by selecting jumper JP9. The output driver is capable of operating an 8Ω speaker, while the input is to be used with a standard PC external microphone.

Figure 4: PC Microphone Connector



4.16 Event Switches

There are four toggle switches (S1-S4) on the development board. These switches are connected to the following subsystems on the board:

Table 16: Event Switch Functions

Switch	*Function(s)*
S1	NBATCHG – Simulates low battery condition when ON. Default is OFF.
S2	NPWRFL – Forces CL-PS7111 into Standby state when ON. Default is OFF
S3	BATOK – Indicates the battery is OK. Default is No battery installed.
S4	NEXTPWR – External power OFF. Default is external power ON.

There are two momentary switches on the development board. These switches are connected to the following subsystems on the board:

Table 17: Momentary Switch Functions

Switch	*Function(s)*
S5	WAKEUP – When activated, it forces the CL-PS7111 into the operating state.
S6	NURESET – When activated, it resets the CL-PS7111, CS8900A, and CL-PS6700.

4.17 SSI Interface

The SSI interface connector allows the development board to control peripheral boards that may implement the SSI interface. However, there are a number of limitations with this implementation. First, the interface operates at 3.3V only and second, there is already a SSI peripheral (analog to digital converter) connected to the interface. This means that any additional peripherals must decode the SSI chip-select in addition to the GPIO bit provided.

Table 18: SSI Interface

Description	*Pin No.*	*Pin No.*	*Description*
SMPCLK (Sample clock for ADC)	1	2	Ground
ADCCLK (SSI clock)	3	4	Ground
ADCIN (SSI input)	5	6	Ground
ADCOUT (SSI output)	7	8	Ground
nADCCS (SSI chip select)	9	10	Ground
nEINT2 (Interrupt)	11	12	Ground
PB3 (GPIO bit)	13	14	Ground

4.18 Serial Ports

The CL-PS7111 is equipped with two Universal Asynchronous Receiver Transmitters (UARTS). Both UARTs support data rates up to 115kbps and have a 16 byte FIFO on both the receive and transmit channels.

UART1 also supports the IrDA protocol, which can be enabled under software control.

4.18.1 UART1

The primary serial port of the CL-PS7111 is UART1, which contains many of the modem control signals found in a standard UART. The signals not implemented by the CL-PS7111 are RTS, DTR, and RI. The development board implements RTS using GPIO signal PB1 and RI using GPIO signal PB2. DTR is generated using jumper JP14.

The UART1 signals are converted to and from RS-232 levels by a single Maxim device.

4.18.2 IrDA

The IrDA interface is multiplexed with UART1. The Tx and Rx signals of UART1 are routed to the IrDA encoder under the control of the SYSCON1 register.

The transceiver is located at U1 and includes the photo diode and infrared emitter. The interface us capable of up to 115.2Kbps operation.

4.18.3 UART2

UART2 only supports the Tx and Rx signals. It is available at connector J3 labeled UART2, or by a 3-pin header at JP7 labeled TTL UART2.

4.19 Ethernet Controller

The Ethernet controller on the development board is a Cirrus Logic CS8900A 10Base-T type controller. The device has an ISA compatible interface with the I/O mapped register set implemented on this design.

Note: A detailed discussion of how data is transferred to and from the Ethernet port is beyond the scope of this document. Developers wishing to know more about this are referred to the CS8900A data sheet. Also note that although the I/O mapped registers are outlined, the internal register set of the CS8900A (PacketPage register set) is not discussed in thorough detail in this document. Refer to the CS8900A data sheet for full details.

4.19.1 I/O Mapped Interface

The I/O mapped interface on the CS8900A is a set of eight registers, each 16-bits wide. Definitions of each register are given here, but for a more thorough explanation, please consult the CS8900A data sheet. I/O registers are mapped into the address space of the CL-PS7111 as follows:

Table 19: CS8900A I/O Mapped Registers

Name	*Address*	*R/W*	*Description*
RTDAT0	0x2000:0000	R/W	Receive/Transmit data (Port 0). Port holds transmitted and received data in 16-bit words.
RTDAT1	0x2000:0004	R/W	Receive/Transmit data (Port 1). Port holds most significant half-word of data in 32-bit mode. The CL-PS7111 treats this interface as strictly 16-bit, so don't use this register.
TxCMD	0x2000:0008	W	Transmit command. This register is written to indicate data is to be transmitted, and how it is to be transmitted. This register controls how many bytes must be in the CS8900A buffer before transmission begins, whether CRC data is to be sent with the transmission, tolerance for data collisions, whether data currently in the buffer memory should be flushed, and whether data should be padded.
TxLength	0x2000:000C	W	Transmit length. This register is written immediately after the transmit command. The length of the frame to be transmitted, in bytes, is written to this register.
ISQ	0x2000:0010	R	Interrupt Status Queue. See the section on exceptions.
PPPTR	0x2000:0014	R/W	PacketPage Pointer. The CS8900A has an internal set of registers called a PacketPage. The PacketPage pointer points to the current address in the page. Writing to this location also optionally sets up an auto-incrementing mode where each read or write of the PacketPage registers increments the pointer.
PDAT0	0x2000:0018	R/W	PacketPage Data (Port 0). Reading or writing this register will access the internal PacketPage register pointed to by the PPPTR register. This register is used for both 16-bit and 32-bit data transfers. As mentioned above, the interface to the CL-PS7111 is 16-bit only and as such, this register should be the only one used when addressing the CS8900A's internal registers.
PDAT1	0x2000:001C	R/W	PacketPage Data (Port 1). This register is only used when communicating with the CS8900A in 32-bit mode, and is not used on the development board.

When reading through the CS8900A data sheet, location 0x0300 is listed as the default base address. Although these registers can be moved around, due to the connection scheme to the CS8900A, a base address of 0x0300 is the only valid setting.

4.19.2 Exceptions from the CS8900A

The CS8900A is capable of producing interrupt requests on any one of its four IRQ lines. IRQ0 is the only interrupt used, and is connected to the CL-PS7111 pin EINT3. All programming of internal registers on the CS8900A should reflect this.

When an event requiring interrupt service occurs, the CS8900A will activate the appropriate interrupt to the CL-PS7111 and place a 16-bit value in the ISQ register. The CL-PS7111 is then able to read this value and perform the appropriate action. This register is similar to a FIFO in that the CS8900A may write several interrupt events to this queue. Interrupts are read from the queue in an order of priority, not occurrence. The CL-PS7111 should continue to read this register until the contents are set to zero by the CS8900A, signaling that all interrupts have been serviced.

4.20 DC to DC Conversion

The CL-PS7111 supports two PWM outputs that are used to implement DC to DC converters. The first converter provides the +12V supply to the PC Card interface. The other converter provides the operating voltage (nominal setting of +21V) for the 320x240 LCD panel.

4.21 Diagnostic LED

A single LED is driven by software as a visual indicator of activity. A power on reset will turn off the LED.

4.22 PC Card

The development board supports a single PC Card slot that is compliant with the PC Card V2.01 specification. The interface is controlled by the CL-PS6700. The complete interface is implemented with the CL-PS6700 and a MAX9712 to control the routing of the PC Card supply voltages.

4.22.1 Power Control Mapping

The table below shows the mapping between the CL-PS6700 power controls PCTL0, 1, 2 and the selected supply voltages, VCC, and VPP to the PC Card interface:

Table 20: CL-PS6700 Power Control

PCTL2	*PCTL1*	*PCTL0*	*VCC*	*VPP*
0	0	0	0V	0V
0	0	1	+5V	+5V
0	1	0	+3.3V	+3.3V
0	1	1	0V	0V
1	0	0	0V	0V
1	0	1	+5V	+12V
1	1	0	+3.3V	+12V
1	1	1	0V	0V

4.22.2 Programming

There are three distinct areas of programming required of the CL-PS6700 for correct operation of the PC Card interface. They are:

- The initialization of the interface within the CL-PS7111
- The configuration of the CL-PS6700
- The timing and operation of the PC Card interface controlled by the CL-PS6700

This section will only cover the first two of these areas. The timing and operation of the PC Card interface are dependent on the card in the slot and is determined from the voltage selection signals provided by the card and the CIS information stored on the card. For further details please refer to "PC Card Standard V2.01".

The following table describes the programming required of the CL-PS7111 to correctly enable the interface to the CL-PS6700:

Table 21: CL-PS7111 Programming for the CL-PS6700 Interface

CL-PS7111 Function	*Register Name*	*Value*	*Description*
Port E bit 1 Data Direction	PEDDR	1	Switch on the +5V Regulator
Port E bit 1 Data	PEDR	1	Switch on the +5V Regulator
Drive 0	PMPCON	0x2	Switch on the +12V DC-DC converter
EXPCLKEN	SYSCON1	1	Enable EXPCLK output
PCMCIA1	SYSCON2	1	Enable PC Card Interface

The following table describes the programming required of the CL-PS6700 to correctly initialize its operation:

Table 22: CL-PS6700 Initialization Programming

CL-PS6700 Function	*Register Name*	*Value*	*Description*
Endian Conversion	System Interface Configuration Register	0	Disable byte swapping
Input Pull-up Enable	Power Management Register	10b	Weak pull-up on Card Detects, except when in standby

4.23 LCD

The CL-PS7111 provides all the signals required to interface directly to a single scan monochrome LCD panel up to a maximum of 1024 pixel line width. However, most panels in this classification have specific interface requirements for timing, voltage generation, and pin assignments.

The development board supports three connection types each intended for a particular panel.

4.23.1 Supported Panels

The panels supported by the development board are:

- ALPS LH – This is a 640x240, 16 gray level, transreflective panel. It has an integrated touch screen, backlight and contrast control. Connection to this panel is via connector J5 labeled 640x240 LCD.
- ALPS – This is a 320x240, 16 gray level, transreflective panel. This panel requires external bias voltages to be supplied. Connection to this panel is via connector J6 labeled 320x240 LCD.
- GENERIC – A method of connection to a user-supplied panel interface board. Connection is made via the header located at JP12 labeled GENERIC LCD.

4.23.2 Panel Connector Assignments

Table 23: LCD Panel Connectors

Pin	*640x240 (J5)*	*320X240 (J6)*	*GENERIC (JP12)*
1	GND	V5	V5
2	DDO	V2	V2
3	DD1	VEE	VEE
4	DD2	VDD	VDD
5	DD3	FRM	FRM
6	VDD	GND	GND
7	PD2_LCDEN	CL1	CL1
8	CL2	GND	GND
9	GND	M	M
10	CL1	PD2_LCDEN	PD2_LCDEN
11	FRM	CL2	CL2
12	PD3_LCDBL	V4	V4
13	PD1_LCD_DC_DC_EN	V3	V3
14	VADJ	DD3	DD3
15	GND	DD2	DD2
16	TSPY	DD1	DD1
17	TSPX	DD0	DD0
18	TSMY	N/C	-
19	TSMX	-	-
20	GND	-	-

Signal descriptions:

1) 640x240 (J5)
   - VDD is 3.3V
   - PD1_LCD_DC_DC_EN is the LCD DC-DC converter on/off signal
   - PD2_LCDEN is the Display On/Off signal
   - PD3_LCDBL enables the backlight
   - VADJ is the contrast voltage control. Value set by pot VR2.
   - TSPY, TSPX, TSMY and TSMX are the digitizer signals

2) 320x240 (J6)
   - VDD is 3.3V
   - V2-V5 are bias voltages
   - PD2_LCDEN is the display enable
   - M is the AC modulation

4.23.3 Panel Programming

Each of the two main supported panels needs specific programming. The details for each panel are as follows:

Table 24: Register Settings for 640x240 Panel

Register Name	*Register Offset*	*Register Value*
SYSCON1	0x8000:0100	set bit 12
PALLSW	0x8000:0540	0x7654:3210
PALMSW	0x8000:0580	0xFEDC:BA98
LCDCON	0x8000:02C0	0xF01C:F2BF

Table 25: Register Settings for 320x240 Panel

Register Name	*Register Offset*	*Register Value*
SYSCON1	0x8000:0100	set bit 12
PALLSW	0x8000:0540	0x7654:3210
PALMSW	0x8000:0580	0xFEDC:BA98
LCDCON	0x8000:02C0	0xF03A:695F

4.24 Power

There are two primary power supplies implemented on the development board: 3.3V provides power for much of the board and +5V provides power for the +5V PC Cards.

5 Physical Specification

5.1 PCB Form Factor

The PCB form factor is 8.5" x 10.5". The board is self-contained and has the keyboard and LCD mounted on it.

5.2 PCB Construction Materials

The PCB is constructed from materials with a flame rating of 94V0. This rating meets the self-extinguishing characteristics required by safety agencies in countries of sale.

5.3 Connector Details

Logic Analyzer headers (JP10, JP19-22) The logic analyzer headers on this design are 2x10, 0.100" spacing, 0.025" square posts. For an example of the strip-header used for this port, see 3M part # 2520-6002.

LCD (J5) The LCD connector is a FFC/FPC 20-way ZIF connector, 0.5mm spacing. For an example of this connector, see HIROSE part # FH12-20S-0.5SH.

LCD (J6) The LCD connector is a FFC/FPC 18-way ZIF connector, 1mm spacing. For an example of this connector, see MOLEX MOL52207-1890.

Serial Ports (J3, J4) Serial port connectors are male, right angle, standard density, 9-contact DSUBs. For dimension information on these connectors, see AMP part # 787203-1.

PCMCIA (J8) PCMCIA right angle connector. For an example of this device, see FUJITSU FCN-565PO68-G/XC-V4.

Power (J9) Mini power connector, 0.1 pin. For an example, see Switchcraft RAPC712.

Ethernet (J7) The Ethernet connector used in this design is a standard right angle 10Base-T RJ45. For dimensional details of this connector, see CorCom part # RJ45-8L2-S.

Microphone (J1) The microphone connector is a standard 3.5mm phone-jack. Electret style microphones such as Telex's Voice Commander microphone may be connected to this port. For dimension data, see A/D ELEC AD3056-50.

Speaker (J2) The speaker connector is a standard 3.5mm phone-jack. For dimension data, see A/D ELEC AD3056-50.

6 Operating and Storage Environments

6.1 Temperature

The CL-PS7111 development board can be stored safely at temperatures ranging from -20-85°C, inclusive. The CL-PS7111 development board will function reliably in an ambient operating temperature of 0-70°C, inclusive.

6.2 Humidity

The CL-PS7111 development board is reliable in storage and operating in relative humidity of 10% to 95% (non-condensing) in the appropriate temperature ranges specified above.

6.3 Air Flow

The CL-PS7111 development board is reliable in storage and operating in static air at temperatures and relative humidity specified above.

6.4 Regulatory Compliance (FCC Part 15 Class B, and Part 68)

As this product is sold as an evaluation platform only, no EMI testing was performed.

7 Sources of Additional Information

Web page addresses for suppliers of parts used on the development board:

3M	http://www.mmm.com/interconnects/
ARM	http://www.arm.com/
AMP	http://connect.amp.com/
Coiltronics	http://www.coiltronics.com/
Cirrus Logic, Inc.	http://www.cirrus.com/
Crystal Semiconductor	http://www.cirrus.com
Hitachi	http://www.halsp.hitachi.com/
Molex	http://www.molex.com/
Intel	http://www.intel.com/
OKI	http://www.oki.com/
Maxim	http://www.maxim-ic.com/