CIRRUS LOGIC ®

FEATURES

- ■ **Ultra low power**
  — Designed for applications that require long battery life while using standard AA/AAA batteries
  — Average 20 mA in normal operation (everything on)
  — Average 5 mA in idle mode (clock to the CPU stopped, everything else running)
  — Average 3 µA in standby mode (realtime clock on and everything else stopped)

- ■ **Performance matching 33-MHz Intel® '486-based PC**
  — 15 Vax™-MIPS (Dhrystone®) at 18 MHz

- ■ **ARM710A microprocessor**
  — ARM7 CPU
  — 8 Kbytes of four-way set-associative cache
  — MMU with 64-entry TLB (transition look-aside buffer)

- ■ **DRAM controller**
  — Connects up to four banks of DRAM, with each bank being 32 bits wide and up to 256 Mbytes in size

(cont.)

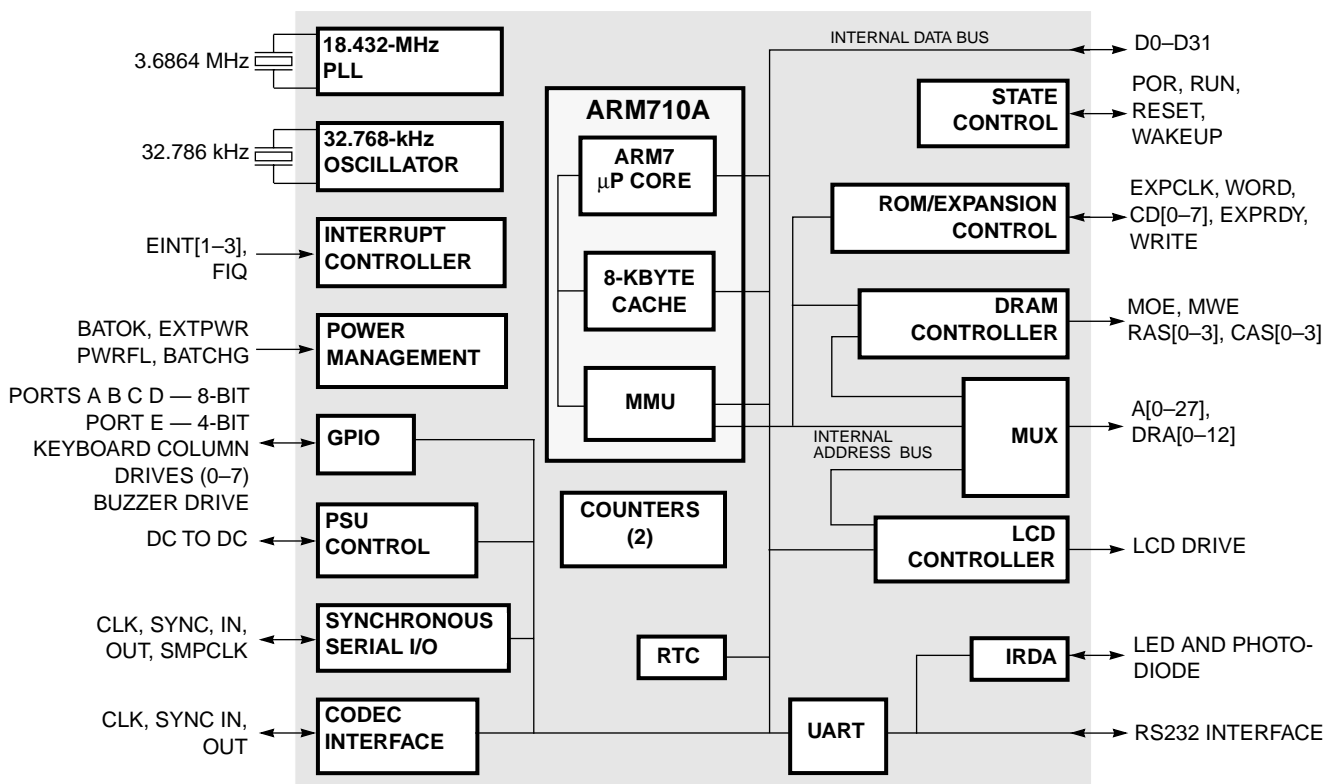## Ultra-Low-Power Device for Hand-Held Applications

OVERVIEW

The CL-PS7110 is designed for ultra-low-power applications such as organizers/PDAs, two-way pagers, smart phones, and hand-held internet browsers. The device's core-logic functionality is built around an ARM710A microprocessor with 8 Kbytes of four-way set-associative unified cache.

At 18.432 MHz (for 3-V operation), the CL-PS7110 delivers nearly 15 Vax-MIPS of performance (based on Dhrystone® benchmark) — roughly the same

(cont.)

Functional Block Diagram

FEATURES (cont.)

- **ROM/SRAM/flash memory control**
  - Decodes eight separate memory segments of 256 Mbytes
  - Each segment can be configured as 8, 16, or 32 bits wide and support page-mode access
  - Programmable access time for conventional SRAM/ROM/flash memory
  - Expansion device can also be a PC Card (PCMCIA) controller

- **Codec interface**
  - Provides all necessary clocks and timing pulses and performs serialization of the data stream (or vice versa) to or from standard telephony codecs
  - Data transfer at 64 kbps

- **Synchronous serial interface**
  - Supports SPI®[1] or Microwire®[2]-compatible interface

- **36-bit general-purpose I/O**
  - Four 8-bit and one 4-bit GPIO port
  - Supports scanning keyboard matrix

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[1] SPI is a registered trademark of Motorola®.

[2] Microwire is a registered trademark of National Semiconductor®.

- **16C550-style UART**
  - Supports bit rates up to 115.2 kbps
  - Contains two 16-byte FIFOs for Tx and Rx
  - Supports modem control signals

- **SIR (slow (9600–115.2 kbps) infrared) encoder**
  - IrDA (Infrared Data Association) SIR protocol encoder can be optionally switched into Tx and Rx signals of the UART up to 115 kbps

- **DC-to-DC converter interface**
  - Provides two 96-kHz clock outputs, whose duty ratio are programmable (from 1-in-16 to 15-in-16)

- **LCD controller**
  - Interfaces directly to a single-scan panel monochrome LCD
  - Panel size is programmable and is any width (line length) from 16 to 1024 pixels in 16-pixel increments
  - Video frame size programmable up to 128 Kbytes
  - Bits per pixel programmable from 1, 2, or 4
  - Two 32-bit palette registers to support 4-, 2-, or 1-bit pixel values for mapping to any of the 16 grayscale values

- **Two timer counters**

- **Realtime clock (32-bit)**

OVERVIEW (cont.)

level of performance offered by a 33-MHz Intel® '486-based PC.

As shown in the system block diagram, simply adding desired memory and peripherals to the highly integrated CL-PS7110 completes a hand-held organizer/PDA system board. All the interface logic is integrated on-chip.

The CL-PS7110 is packaged in a 208-pin VQFP package, with a body size of 28-mm square, lead pitch of 0.5 mm, and thickness of 1.4 mm.

Memory Interface

There are two main external memory interfaces and a DMA controller that fetches video display data for the LCD controller from main DRAM memory.

The SRAM/ROM-style interface has programmable wait state timings and includes burst-mode capability, with eight chip selects decoding eight 256-Mbyte sections of addressable space. For maximum flexibility, each bank can be specified to be 8, 16 or 32 bits wide to enable the use of low-cost memory in a 32-bit

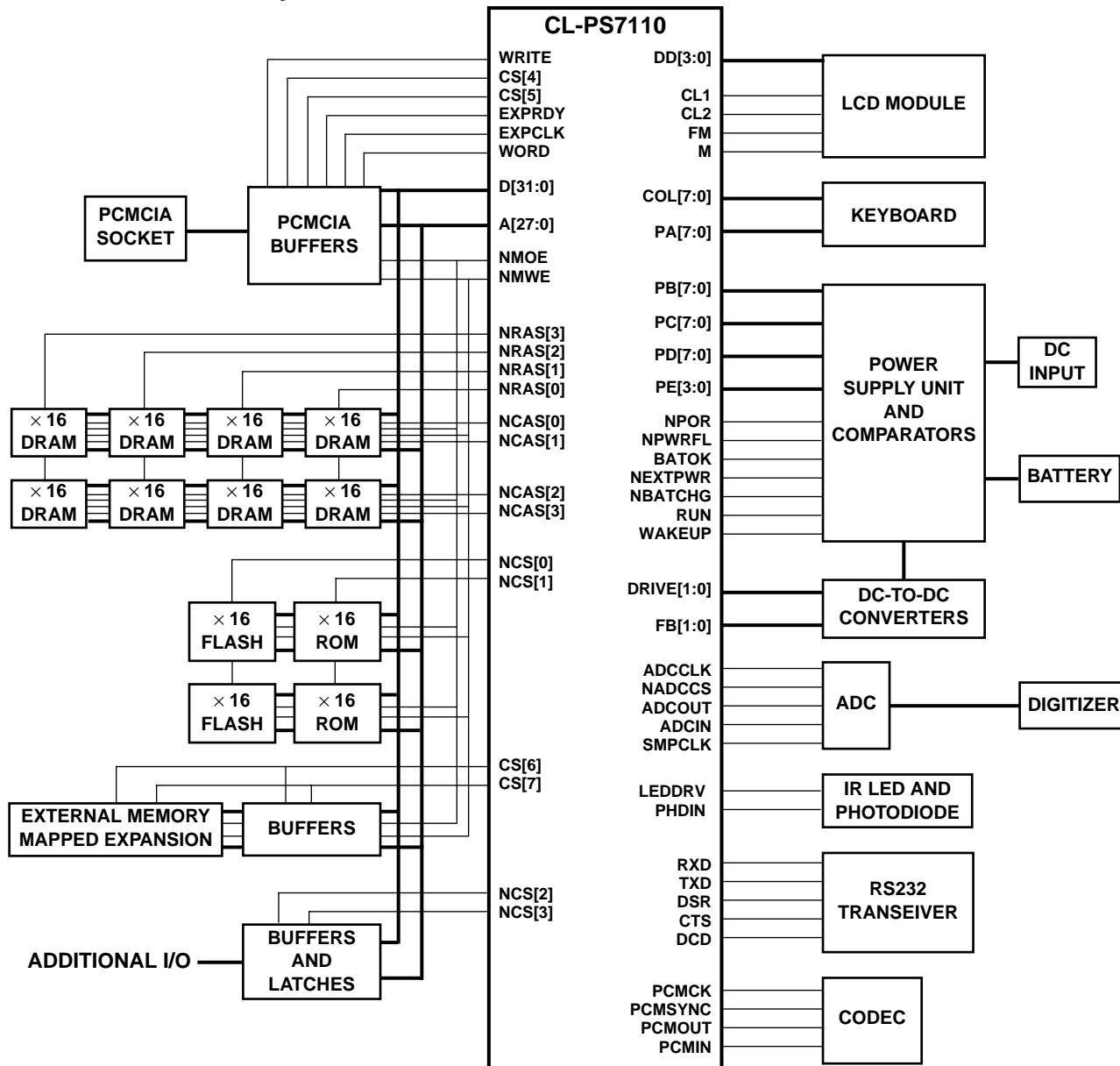system. The system can have an 8-bit-wide boot option to optimize memory size.

The DRAM interface allows direct connection of up to 4 banks of DRAM, each bank containing up to 256 Mbytes. To assure the lowest possible power consumption, the CL-PS7110 supports self-refresh DRAMs, which are placed a low-power state by the device when it enters its low-power standby mode.

Serial Interface

For RS232 serial communications, the CL-PS7110 includes a UART with two 16-byte FIFOs for receive and transmit data. The UART supports bit rates of up to 115.2 kbps. An IrDA SIR protocol encoder/decoder can be optionally switched into the Rx/Tx signals to/from the UART to enable these signals to drive an infrared communication interface directly.

A full-duplex codec interface allows direct connection of a standard codec chip to the CL-PS7110, allowing storage and playback of sound.

A CL-PS7110–Based System

CL-PS7110

WRITE
CS[4]
CS[5]
EXPRDY
EXPCLK
WORD

D[31:0]

A[27:0]

NMOE
NMWE

NRAS[3]
NRAS[2]
NRAS[1]
NRAS[0]

NCAS[0]
NCAS[1]

NCAS[2]
NCAS[3]

NCS[0]
NCS[1]

CS[6]
CS[7]

NCS[2]
NCS[3]

DD[3:0]

CL1
CL2
FM
M

COL[7:0]

PA[7:0]

PB[7:0]

PC[7:0]

PD[7:0]

PE[3:0]

NPOR
NPWRFL
BATOK
NEXTPWR
NBATCHG
RUN
WAKEUP

DRIVE[1:0]

FB[1:0]

ADCCLK
NADCCS
ADCOUT
ADCIN
SMPCLK

LEDDRV
PHDIN

RXD
TXD
DSR
CTS
DCD

PCMCK
PCMSYNC
PCMOUT
PCMIN

PCMCIA SOCKET

PCMCIA BUFFERS

× 16 DRAM   × 16 DRAM   × 16 DRAM   × 16 DRAM

× 16 DRAM   × 16 DRAM   × 16 DRAM   × 16 DRAM

× 16 FLASH   × 16 ROM

× 16 FLASH   × 16 ROM

EXTERNAL MEMORY MAPPED EXPANSION

BUFFERS

ADDITIONAL I/O

BUFFERS AND LATCHES

LCD MODULE

KEYBOARD

POWER SUPPLY UNIT AND COMPARATORS

DC INPUT

BATTERY

DC-TO-DC CONVERTERS

ADC

DIGITIZER

IR LED AND PHOTODIODE

RS232 TRANSEIVER

CODEC

A separate synchronous serial interface supports two industry-standard protocols (SPI® and Microwire®) for interfacing to standard devices such as an ADC, allowing for peripheral expansion such as the use of a digitizer pen.

Power Management

The CL-PS7110 is designed for low-power operation. There are three basic power states:

- **Standby — T**his state is equivalent to the computer being switched off (no display), and the main oscillator shut down

- **Idle —** In this state**,** the device is functioning and all oscillators are running, but the processor clock is halted while waiting for an event such as a key press.

- **Operating —** This state is the same as the idle state, except that the processor clock is running.

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The Company

Headquartered in Fremont, California, Cirrus Logic is a leading manufacturer of advanced integrated circuits for desktop and portable computing, telecommunications, and consumer electronics. The Company applies its system-level expertise in analog and digital design to innovate highly integrated, software-rich solutions.

Cirrus Logic has developed a broad portfolio of products and technologies for applications spanning multimedia, graphics, communications, system logic, mass storage, and data acquisition.

The Cirrus Logic formula combines innovative architectures in silicon with system design expertise. We deliver complete solutions — chips, software, evaluation boards, and manufacturing kits — on-time, to help you win in the marketplace.

Cirrus Logic's manufacturing strategy ensures maximum product quality, availability, and value for our customers.

Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.