CL-SH7660

Preliminary Product Bulletin

Advanced Architecture ATA Disk Controller

FEATURES

- **Ultra DMA66 support**
  - — Host data rates up to 66.6 Mbytes/sec.
- **ID-less architecture**
  - — SMASH™ engine — sector mark and split handling
  - — Defect management and logical sector mapping
- **Hardware and software compatibility with ATA-4 host interface standard**
- **SDRAM support**
  - — Maximum 115.5 Mbytes/sec. bandwidth
- **8-bit NRZ disk interface**
  - — 340 Mbits/sec. (42.5 Mbytes/sec.) maximum disk data rate
- **Advanced data integrity capabilities**
  - — ECC97 corrector
    - 3-way interleaved ECC with 21 bytes correctable per sector on the fly, and erasure pointer support
- **Automated ATA host interface processing**
  - — Hardware support for auto multi-sector write, auto sequential write, and auto sequential read commands
  - — Host selection interrupt generation without system clock
- **Supports 1023 sectors per track**
- **Frequency synthesizer**
  - — Generates internal buffer, host, system, and correction clocks

(cont.)

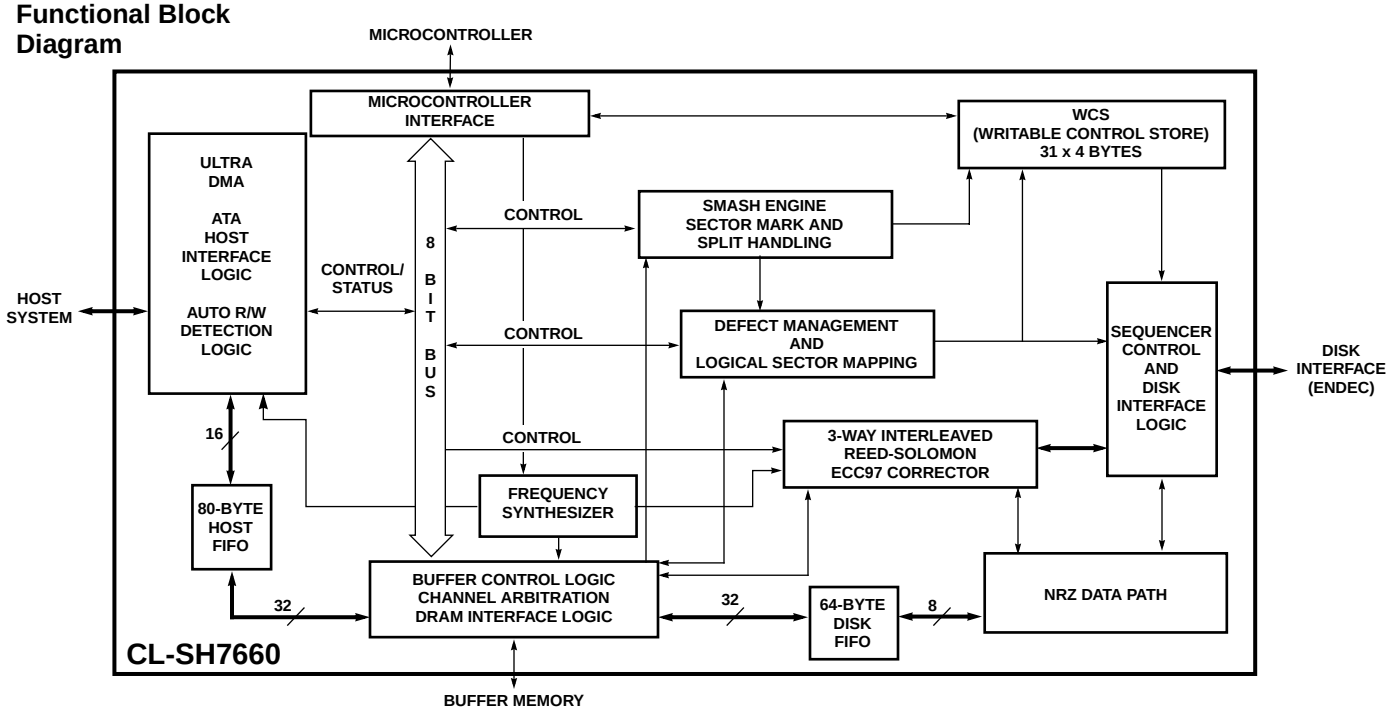
OVERVIEW

The CL-SH7660 is a member of the latest generation of advanced disk controllers from Cirrus Logic. The device offers the ID-less architecture plus advanced data integrity features required by the error characteristics of high-density disk drive technology. The CL-SH7660 provides a high-bandwidth solution using SDRAMs or EDO DRAMs to enable high-performance host and disk transfer rates.

The CL-SH7660 provides a large portion of the hardware necessary to build an ATA disk drive controller board. The CL-SH7660 is typically configured with buffer memory and a microcontroller (with system RAM and ROM) to create a complete ATA disk drive controller. The CL-SH7660 design combines ID-less architecture with advanced data integrity features, a sector formatter, eight-channel buffer arbitration logic, a high-speed microcontroller interface, and hardware ATA host interface support.

(cont.)

Functional Block Diagram



FEATURES *(cont.)*

ID-Less Architecture

- **SMASH™ engine — sector pulse and physical sector number generation**
- **SMASH™ frame tables reside in buffer memory**
- **Physical-to-logical sector number mapping**
- **Hardware mapping of logical and physical end-of-track flags, defect flags, and other flags**
- **Hardware defect management supports sector slipping and sector skipping**
- **Defect lists reside in buffer memory**

Microcontroller Interface

- **Support for high-speed processors (for example, 80196, 68HC11, 68HC16, HPC460X3, TMS320, ARM, and 16X)**
- **Support for multiplexed and non-multiplexed address and data bus interfaces**
- **Supports interrupt- or polled-processor interface**
- **Supports Intel®- or Motorola®-type byte ordering for word-wide microprocessor instructions**
- **Hardware wait states provided by LREADY signal with programmable or automatic wait state timing**
- **Supports direct microcontroller access to buffer memory and four external switches**
- **Supports access to buffer memory through scheduled or LREADY modes**
- **Provides six external switches**
- **Supports separate host and disk interrupt structures**
- **Four programmable power-down modes**

ATA Interface

- **High speed host data transfer modes supported:**
  - — Ultra DMA mode 4 (66.6 Mbytes/sec.)
  - — Multi-word DMA mode 2 (22 Mbytes/sec.)
  - — PIO mode 4 (16.6 Mbytes/sec.)
- **Supports automatic host transfer for multi-sector write, sequential write, and sequential read commands**
- **Supports automatic update of ATA task file and release of data blocks**
- **Programmable and auto wait state generation for compatibility with any host speed using IORDY**
- **Direct bus interface with on-chip programmable 4/12-mA data bus drivers**
- **Supports ATA master/slave protocol**
- **Receives host commands without system clock**

Buffer Manager

- **Maximum SDRAM buffer bandwidth**
  - — 115.5 Mbytes/sec.
- **Maximum EDO mode bandwidth**
  - — 64 Mbytes/sec.
- **Supports streaming mode**
  - — Hardware automation of concurrent host and disk transfers from different buffer segments, with a pacing mechanism to prevent buffer overrun/underrun conditions
  - — Host and disk streaming modes can be enabled separately, facilitating flexible streaming and disk caching functions
- **DRAM buffer memory configurations supported:**
  - — 64K x 16
  - — 256K x 16
- **Internal frequency synthesizer provided to generate buffer, host, system, and corrector clocks**
- **Eight-channel, fixed-priority arbitration scheme:**
  - — Disk, ECC correction, DRAM refresh, microcontroller, defect scan, defect list access, SMASH™ frame table access, and host
- **Variable buffer segmentation with byte resolution for user-defined caching and read look-ahead**

Disk Interface

- **Supports 1023 sectors per track**
- **Disk LBA checking and hardware defect management**
  - — Advanced branch commands automate retry algorithms
- **Maximum NRZ data rates**
  - — 340 Mbits/sec. (42.5 Mbytes/sec.)
- **Programmable Reed-Solomon ECC for the data field provides on-the-fly correction for: a single 161-bit error burst, two bursts of 81 and 73 bits, respectively, or three 49-bit bursts (the code can be programmed for lower ECC overhead and correction capability)**
- **ECC on-the-fly correction for each sector is guaranteed to complete within the next two sectors**
- **Programmable read synchronization timer and index counter allow flexible timeout control**
- **Sequencer can be stopped asynchronously by edge- or level-triggered inputs**
- **Programmable RAM-based sequencer WCS (writable control store) of 31 x 4 bytes**
- **Automatic handling of logical or physical end-of-track conditions**

OVERVIEW (cont.)

IID-less Architecture

There are two major components of the ID-less architecture. The first component is the SMASH engine (sector mark and split handling), which generates sector pulses for an embedded servo environment and generates a physical sector number for each sector pulse.

The second major component is the defect manager, which maps the physical sector number to a logical sector number, along with the appropriate defect and end of track flags. The defect manager supports the sector slipping and sector skipping defect management schemes in hardware.

Microcontroller Interface

The CL-SH7660 interfaces directly to a microcontroller and supports both multiplexed and nonmultiplexed, Intel®- and Motorola®-type architectures (for example, 80196, 68HC11, and 68HC16). Both interrupt-driven or polling mode firmware architectures are supported. Extensive interrupt masking capability is available for disk and host interface-related interrupts.

ATA Interface

The CL-SH7660 supports automatic handling of multisector write, sequential write, and sequential read commands using the host block transfer mode and automatic task file updating. The CL-SH7660 supports Ultra DMA transfers up to 66.6 Mbytes/sec. and meets multi-word DMA mode 2 and PIO (programmed I/O) mode 4 data transfer rates by supporting speeds up to 22 Mbytes/sec. and 16.67 Mbytes/sec., respectively.

Buffer Manager

The CL-SH7660 buffer manager supports SDRAM and EDO DRAM buffer memory devices, and controls up to 256K x 16 of DRAM buffer memory with eight-channel buffer arbitration logic. The eight channels supported are: disk, ECC correction, DRAM refresh, local microcontroller, defect scan, defect list, SMASH frame table, and host.

The buffer manager supports multisector data transfers without microprocessor intervention. It also allows flexible buffer segmentation for read and write caching implementations.

Sector Formatter

The CL-SH7660 sector formatter comprises a serializer/deserializer (SERDES), a flexible RAM-based sequencer (WCS), and CRC/ECC generation circuitry. It supports disk data rates up to 340 Mbits/sec. A proprietary split-data-field technique optimizes disk capacity by allowing the use of embedded servo positioning systems with zoned-recording formats. Support for 1023 sectors per track is also provided.

Streaming

The full streaming feature of the CL-SH7660 buffer manager allows the host and disk to transfer data from the same circular buffer simultaneously with a mechanism to prevent buffer overrun/underrun conditions. Registers, pointers, and timers are updated by hardware to control the transfer of data between the disk and buffer and between the buffer and host without microprocessor intervention.

Data Field ECC

Several advanced data integrity features are offered by the CL-SH7660. The data field ECC (error correction code) consists of a three-way interleaved Reed-Solomon code with programmable redundancy of between 4 and 14 ECC bytes per interleave for a total of between 12 and 42 bytes of ECC redundancy, respectively. The correction power can be programmed for between 1- and 7-byte error burst correction per interleave on the fly, and up to 14 bytes per interleave with erasure pointer support from the channel device. At 14 bytes of ECC redundancy per interleave, the CL-SH7660 guarantees correction of a single error burst up to 161 bits long, or two bursts of 81 and 73 bits.

Disk LBA Checking

The CL-SH7660 also provides disk LBA (logical block address) checking, which can provide additional data integrity in the ID-less environment. The disk LBA bytes are embedded in the CRC field during a disk write, and checked during a disk read.

General

The CL-SH7660 is designed in a 3.3-volt, advanced low-power, 0.35-micron technology. The device is available in 128-pin MQFP and 128-pin LQFP packages.

Direct Sales Offices

Domestic

N. CALIFORNIA
Fremont
TEL: 510/623-8300
FAX: 510/252-6020

S. CALIFORNIA
Los Angeles
TEL: 310/820-6849
FAX: 310/820-6180

Westlake Village
TEL: 805/371-5860
FAX: 805/371-5861

NORTHWESTERN AREA
Portland, OR
TEL: 503/620-5547
FAX: 503/620-5665

SOUTH CENTRAL AREA
Austin, TX
TEL: 512/255-8893
FAX: 512/255-0733

NORTHEASTERN AREA
Andover, MA
TEL: 978/794-9992
FAX: 978/794-9998

Columbia, MD
TEL: 410/740-5654
FAX: 410/740-6961

SOUTHEASTERN AREA
Raleigh, NC
TEL: 919/859-5210
FAX: 919/859-5334

Boca Raton, FL
TEL: 561/395-1613
FAX: 561/395-1373

International

CHINA
Shenzhen
TEL: 86/755-3779637
FAX: 86/755-3779734

FRANCE
Paris
TEL: 33/1-48-12-2812
FAX: 33/1-48-12-2810

GERMANY
Herrsching
TEL: 49/81-52-92460
FAX: 49/81-52-924699

HONG KONG
Tsimshatsui
TEL: 852/2376-0801
FAX: 852/2375-1202

JAPAN
Tokyo
TEL: 81/3-3340-9111
FAX: 81/3-3340-9120

KOREA
Seoul
TEL: 82/2-565-8561
FAX: 82/2-565-8565

SINGAPORE
TEL: 65/743-4111
FAX: 65/742-4111

TAIWAN
Taipei
TEL: 886/2-2718-4533
FAX: 886/2-2718-4526

UNITED KINGDOM
Bucks, England
TEL: 44/01628-472211
FAX: 44/01628-486114

High-Value Systems in Silicon

Cirrus Logic is a premier supplier of advanced integrated circuits that combine mixed-signal processing, precision analog techniques, embedded processors, and application-specific algorithms into system-on-a-chip solutions for existing and emerging growth markets. Enhanced by strong systems expertise in selected markets, the company's products add high value to major brands worldwide in magnetic and optical storage, networking communications, consumer/professional audio, video and imaging, and ultra-precision data acquisition.

Cirrus Logic's manufacturing strategy ensures maximum product quality and availability, as well as access to world-class processing technologies through joint ventures with IBM® and Lucent Technologies®.

Contact one of our systems and applications specialists to see how your company can benefit from the high value Cirrus Logic adds to its customers' products.

Cirrus Logic, Inc.
3100 West Warren Ave., Fremont, CA 94538
TEL: 510/623-8300 FAX: 510/252-6020

Publications Ordering: 800/359-6414 (USA) or 510/249-4200
Worldwide Web: http://www.cirrus.com
257660-001