



OpenSPARC™

OpenSPARC Slide-Cast

In 12 Chapters

Presented by OpenSPARC
designers, developers, and
programmers

- to guide users as they develop
their own OpenSPARC designs
and
- to assist professors as they
teach the next generation

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OpenSPARC™

Chapter Twelve

OPENSPARC COMMUNITY PARTICIPATION

David L. Weaver
Principal Engineer, UltraSPARC Architecture
Principal Evangelist, OpenSPARC
Sun Microsystems



OpenSPARC in Academia

University Programs for OpenSPARC

- Sun supports academic use of OpenSPARC
 - > Collaborations
 - > Centers of Excellence (CoEs)
 - > For university:
 - > access to real, modern industrial microprocessor designs and full verification test suites!
 - > publicity and prestige that aids in obtaining grants
 - > Sharing of course material on OpenSPARC website
 - > Hosting of projects on OpenSPARC website
 - > For additional information, send email to:
OpenSPARC-UniversityProgram@Sun.com

University Uses for OpenSPARC:

- Starting point for lab courses
 - s a working design that can be modified for lab projects in computer architecture or VLSI design courses
- Real-world input to test robustness of CAD tools and simulators developed at Univ.
 - t major industry CAD tool vendors already doing this!
- Burn derivative processors into FPGAs
 - B quick design iterations
 - q high-speed emulation
- Trigger spin-off/start-up ventures?

University Uses for OpenSPARC (con'd):

- Experimental processor designs
 - E highly threaded, high-bandwidth network processor
 - h add more FPUs, for highly threaded HPC processing node
 - n add cryptographic processing elements, for high-bandwidth crypto engine
 - b add coprocessors for specialized functions
 - a research into optimizing useful work done per watt of power consumed (efficiency)
 - p computer architecture research - add/remove instructions, new operating modes

Hardware

Computer Architecture
Micro-Architecture
VLSI Design
(frontend and backend)
FPGA implementation
I/O, memory interface
Networking
Security

Hardware/Software

Hypervisor
Operating System Port
HW/SW Co-Design
Performance Studies

Software

CMT programming
Developer Tools
Application Tuning
Compilers
Optimization Tools
Cool Tools
Algorithm development
Virtualization

Blend of Teaching, Lab and Research work

Enabling the World's Largest Market

China Ministry
of Education



Announced
2/27/2008



OpenSPARC™

Who is using OpenSPARC?

China Universities Go Open



- Developing 10 courses using OpenSPARC
- Translating OpenSPARC books to Chinese

OpenSPARC Center of Excellence – Tsinghua University, Beijing, China



Dr. Wang Dongsheng
Professor of Computer Science
Department,

Director of Microprocessor and SoC Center

OpenSPARC Center of Excellence – Peking University, Beijing, China



**Professor Zhang Xing,
Deputy Executive Director of Microelectronics Institute and
Deputy Dean of School of Software and Microelectronics
Professor Yu Dunshan
School of Software and Microelectronics**

Who else is using
OpenSPARC?

Building for the Future

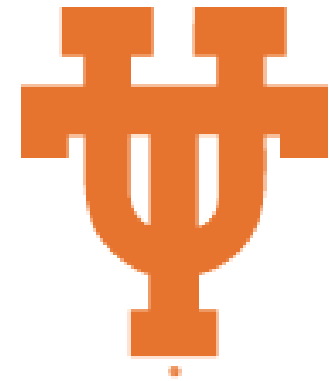
Seven OpenSPARC Centers of Excellence



Carnegie Mellon



ILLINOIS



Taiwan Universities Join OpenSPARC



Sun Microsystems, Inc., with the support of the Embedded Software Consortium under the Ministry of Education announced today the partnership with National Taiwan University, National Tsing Hua University (NTHU), and National Chiao Tung University to promote OpenSPARC technology development.

In an announcement held on July 7th, in Taipei, Sridhar Vajapey, Sun Microsystems, gave the opening and talked about OpenSPARC program followed by Dr. Shyu, Dean of EECS of NTHU, representing MOE's SoC program, and Dr. Lee, Professor of NTHU and Director for MOE's ESW program.

University of Sao Paulo, Brazil



- Feb. 2008 Courses and Research in OpenSPARC
- Mar. 2008, 2 day IEEE Workshop on OpenSPARC Architecture
- Aug. 2008, Ph.D. student at USP, presented two topics related to OpenSPARC work being done at USP.
 - r Random regression test for OpenSPARC T1
 - R Communication structure performance analysis based on transaction level modeling for OpenSPARC processors

Other University Highlights:

- **Australia:** High Performance Scientific Computation Courses
- **Canada:** Modeling Throughput of Fine-grained Multi-threaded Architectures & Multi-processor Scheduling
- **India:** Architecture, CMT & VLSI CAD courses
- **Israel:** Concurrent algorithms & Compilation, Multiprocessor programming
- **Mexico:** Coursework in concurrent computing
- **Spain:** Computer architecture masters course; "Improving Search Engines Performance on Multi-threading Processors" paper accepted at VECPAR 2008

Other University Highlights (2):

- **Spain:** Computer architecture masters course; "Improving Search Engines Performance on Multi-threading Processors" paper accepted at VECPAR 2008
- **Sweden:** CMT courses & research
- **Switzerland:** SW Transactional memory
- **UK:** Multiprocessing & concurrent programming courses
- **USA:** VLSI design, Coverage-directed test generation, NSF network test bed, Reliability Aware Computer Architecture course, thread scheduling and power, memory models, concurrent data structures, work on findbugs (for heavily threaded programs)

Curriculum Examples

Community Members

Brown

- [CS176: The Art of Multiprocessor Programming](#)
 - Fall 2007: Taught by [Maurice Herlihy](#)

Dresden University of Technology

- [Foundations of Concurrent and Distributed Systems](#)
 - Summer 2007: Taught by [Christof Fetzer](#)

Harvard

- [CS165 Introduction to Information Management](#)
 - Spring 2008: Taught by [Margo Seltzer](#)
 - [Fall 2006 web page](#)

MIT

- [6.170: Laboratory in Software Engineering](#)
 - Fall 2007: Taught by [Martin Rinard](#) & Sivan Toledo

Purdue University

- Point of contact: [Tony Hosking](#)
- [CS 490M: Multicore Architecture](#)
 - Spring 2008: Taught by [Zhiyuan Li](#)
- [CS 390C - Principles of Concurrency and Parallelism](#)

Rice University

- [COMP 422: Introduction to Parallel Computing](#)
 - Spring 2008: Taught by Vivek Sarkar & [Bill Scherer](#)
 - Previous version: Spring 2007: <http://www.owl.net.rice.edu/~comp422/>

Simon Fraser University

- [Multicore bibliography portal](#)
- [CMPT 886: Special Topics in Operating Systems and Computer Architecture](#)
 - Spring 2007: Taught by [Sasha Fedorova](#)
- [CMPT 886: Special Topics in Operating Systems and Computer Architecture](#)
 - Spring 2008: Taught by [Sasha Fedorova](#)
 - This web site has a homework assignment that teaches students how to use teaching students how to use Simics, and a good collection of papers on mu

SUNY Oswego

- [CS375: Concurrent Programming](#)
 - Fall: Taught by [Doug Lea](#)
- [CS445: Computer Networks](#)
 - Spring: Taught by [Doug Lea](#)

Technion

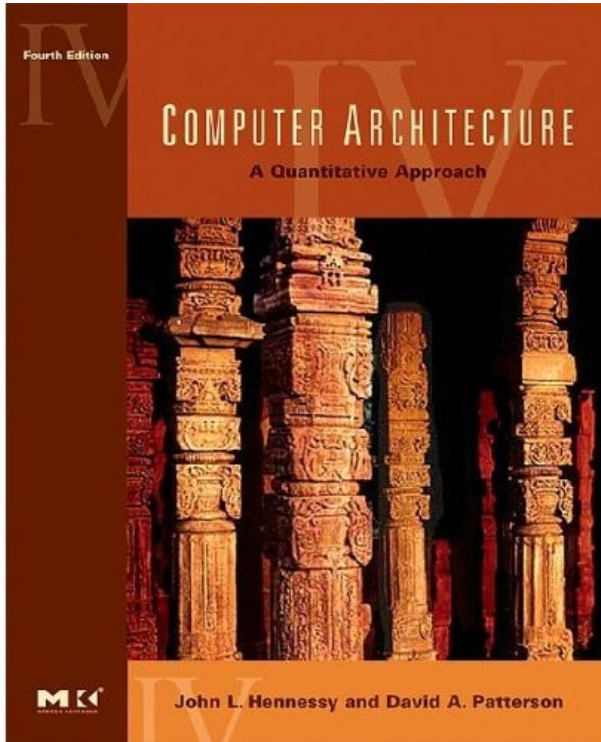
- [Assaf Schuster](#) will be teaching ...

Tel Aviv University

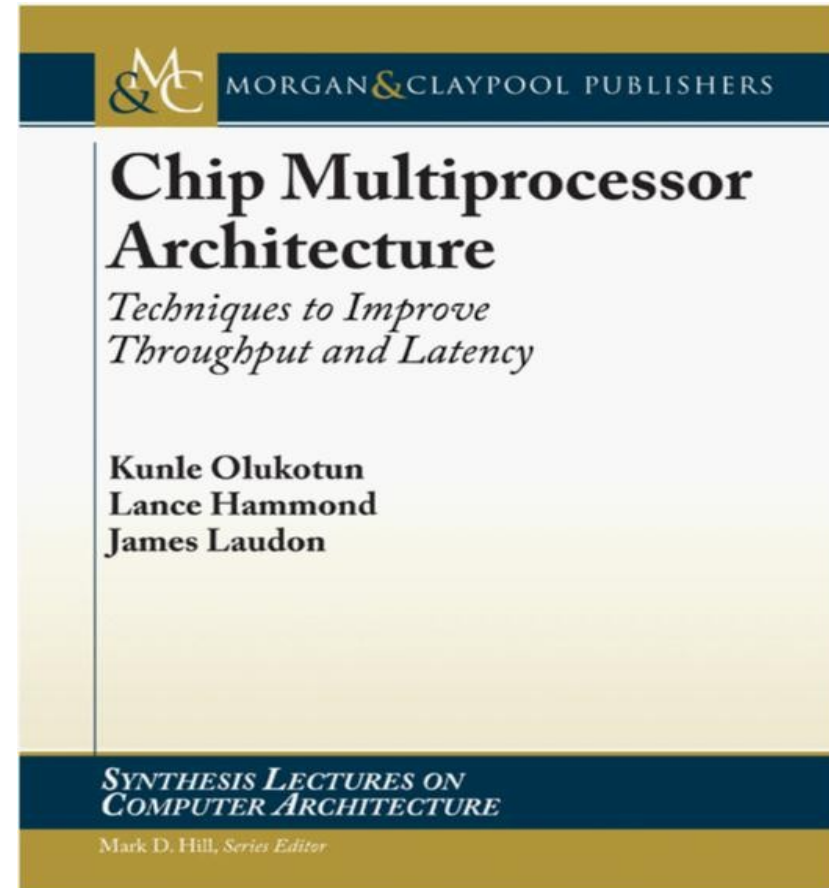
- [0368-3469: The Art of Multiprocessor Programming](#)
 - Spring 2007: Taught by Nir Shavit

<http://wiki.opensparc.net/bin/view.pl/CourseMaterial>

OpenSPARC/Niagara in textbooks



*Computer Architecture:
A Quantitative Approach, 4th ed.*
by John Hennessy and David Patterson
Oct. 2006



Published Nov. 2007

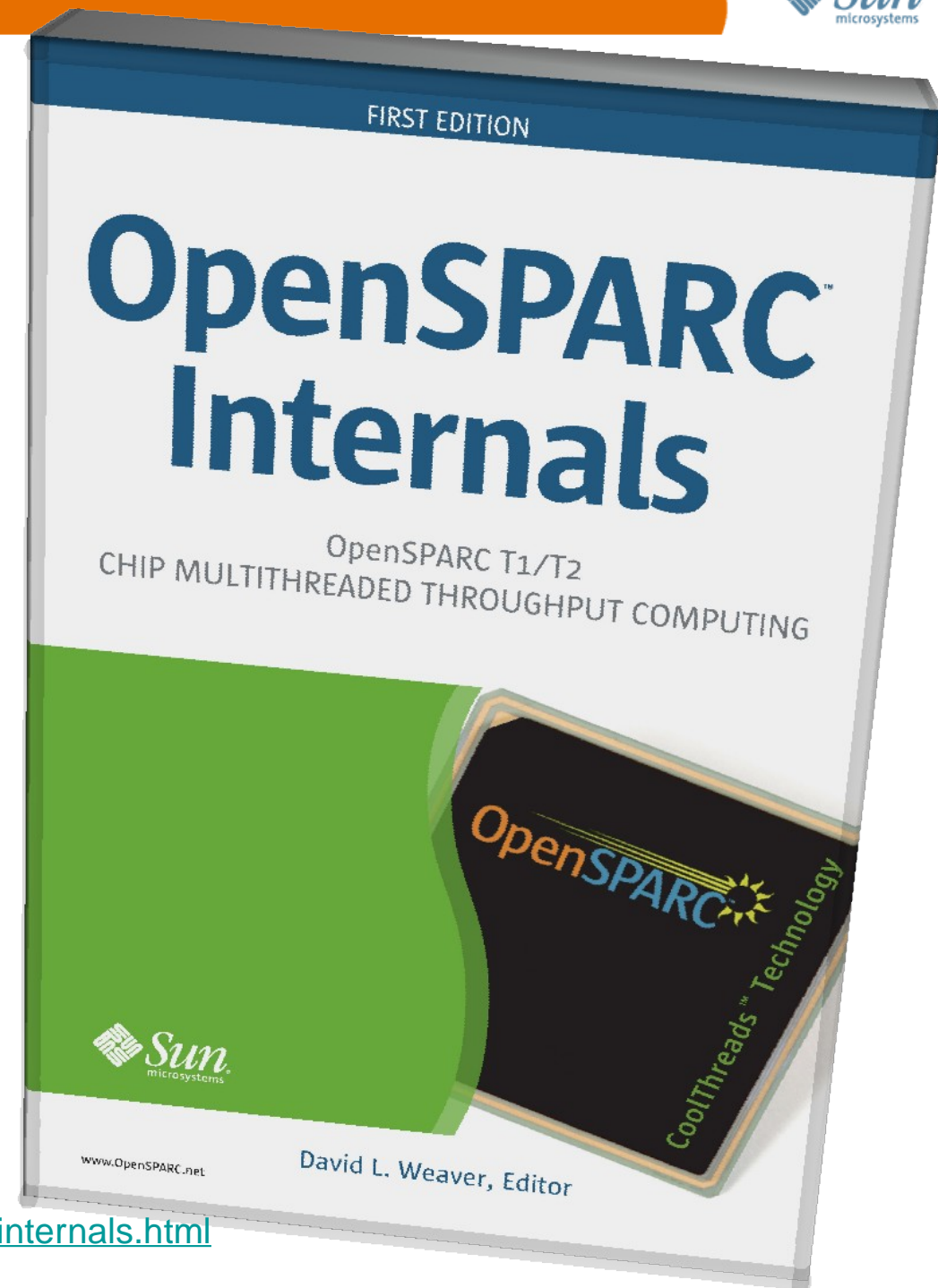
Newest Book Available Oct 08

Largely written by the team of OpenSPARC designers, developers and programmers, a “how to” book to guide users as they develop their own OpenSPARC designs.

Edited by David Weaver,
Principal Engineer,
UltraSPARC Architecture

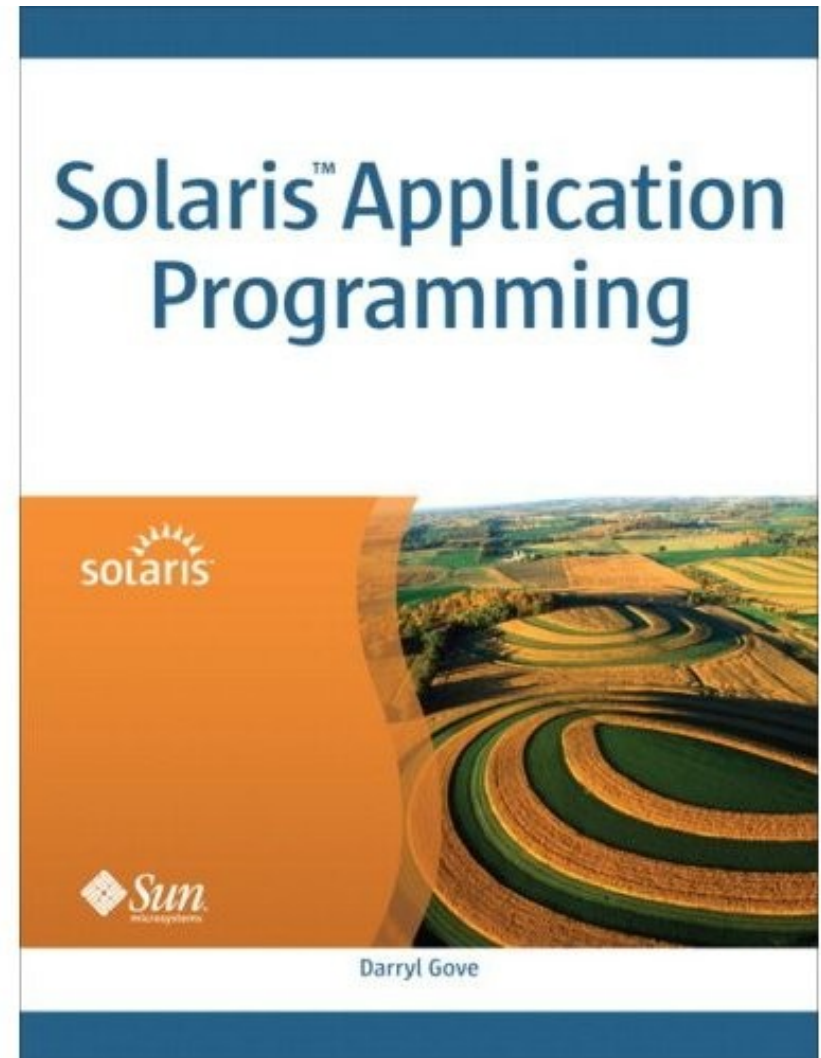
Free Download Available on

<http://www.opensparc.net/publications/books/opensparc-internals.html>



Solaris Application Programming

"Solaris Application Programming ... gives you the background information, tips, and techniques for developing, optimizing, and debugging applications on Solaris."

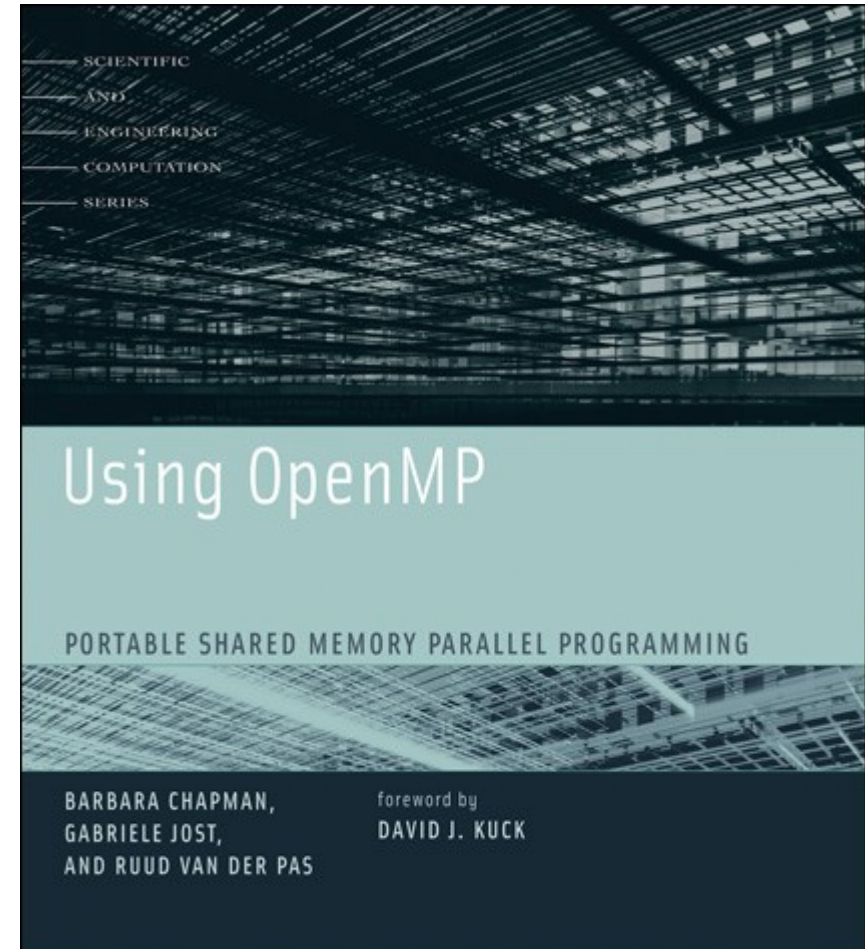


Published January 2008

http://www.sun.com/books/catalog/solaris_app_programming.xml

Existing UH Collaboration

*Using OpenMP
Portable Shared Memory Parallel
Programming
Barbara Chapman, Gabriele Jost and
Ruud van der Pas
Foreword by David J. Kuck
October 2007*



About the Authors

*Barbara Chapman is Professor of Computer Science at the University of Houston.
Gabriele Jost is Principal Member of Technical Staff, Application Server Performance Engineering, at Oracle, Inc.
Ruud van der Pas is Senior Staff Engineer at Sun Microsystems, Menlo Park.*

OpenSPARC – What's Available

OpenSPARC T1

- Complete Solution
 - > Full implementation -- CPU core, FPU, L2 in Verilog RTL
 - > Tools – Verification suite, Simulation, Performance, Compiler optimization tools
 - > Multiple OpenSource Operating Systems: Solaris 10, Linux, FreeBSD, etc
- All Open Source on the web
 - > from OpenSPARC.net and additional web sites
- Actively enabling community for Open Sourcing of hardware and software

What's Available – for HW Engineering

- RTL (Verilog) of OpenSPARC T1 design (8 cores, 32 threads – **14 million lines of code!**)
- RTL for *reduced* OpenSPARC, for FPGA
- Synthesis scripts for RTL
- Verification test suites
- UltraSPARC Architecture 2005 Specification
- UltraSPARC T1 Implementation Specification
- Full OpenSPARC simulation environment
- “CoolTools”, including Sun Studio software, SPARC-optimized GCC compiler, development tools, ATS, etc

What's Available – for SW Engineering

- Architecture and Performance Modelling Package, including:
 - SAS – Instruction-accurate SPARC Architecture Simulator (includes source code)
 - SAM – SPARC instruction-accurate full-system simulator (includes source code)
 - Solaris Images for simulation: Solaris 10, Hypervisor, OBP
 - Legion – SPARC full-system simulation model for software developers (includes source code)
 - Hypervisor source code
 - Documentation

What's Available – other sources

- OpenSolaris (OpenSolaris.org)
- Linux ports for T1-based systems:
 - > Ubuntu
 - > Gentoo
 - > Wind River Linux
 - > FreeBSD
- “Simply RISC” processor design based on OpenSPARC (SRisc.com)
- New Hennessy & Patterson book, Chap 4
- Chip Multiprocessor Architecture book by Kunle, Hammond, and Laudon
- ...etc...

What others are doing with this

- SimplyRISC released S1 core based on T1 v1.4
 - > Supports Wishbone interface
 - > Supports FPGAs
- Gaisler Research integrating single thread T1 in GRLIB
 - > Supports AHB bus interface
 - > Working through software integration issues
- Polaris Micro (China) taped out a chip in 130nm technology

What can you do with this?

- Experiments and Research
 - > Instruction set research: adding new instructions
 - > Cores versus threads
 - > Effects of Cache sizes
 - > Experiment with different coherence protocols
 - > Power-saving techniques
- Build large systems
 - > Many CPUs on linked FPGA boards
- Or use a single core for an embedded system

OpenSPARC Community Participation and Governance

OpenSPARC participation

- Community Registration:
 - > <http://www.sunsource.net/servlets/Join> After registration and confirming password, you can join the mailing lists:
<http://www.sunsource.net/servlets/ProjectMailingListsList>
- Forums:
 - > <http://forum.java.sun.com/category.jspa?categoryID=120>
(separate registration required for posting)

OpenSPARC participation

- Add your university (or company) to the marketplace:
<http://www.opensparc.net/community-marketplace/>
- Send us your profile and we'll post it:
<http://www.opensparc.net/profiles/>
- Add yourself to our Frappr!:
<http://www.opensparc.net/frappr.html>
- Contribute to our OpenSPARC Book:
<http://wiki.opensparc.net/bin/view.pl/Main/Webhome>
(separate registration required for editing)

OpenSPARC Community Groups

Academia/Universities

Architecture, ISA, VLSI course work
Threading, Scaling, Parallelization
Benchmarks

EDA Vendors

Benchmarking
Reference flow
FPGA
Emulation
Verification
Physical Design
Multi-threaded tools

CMT Tools

Compilers, Threading
Optimization
Performance Analysis

Operating Systems

OpenSolaris,
Linux, BSD variants,
Embedded OSs

Hardware IP Suppliers

PCI cores, SERDES etc.

Chip Designers

SoC designs, Hard macros
Telecom applications



OpenSPARC™

OpenSPARC Grows the Community

- Simply RISC “S1”
 - > Single-core version of UltraSPARC T1
 - > Targets small embedded devices
 - > Runs Solaris and Linux
 - > Design also released under GPL
- Allows Sun to grow the SPARC community by virtue of having great technology and not by handing out money

“Due to the collaborative nature of the GPL license Simply RISC plans to add new features to the S1 Core and test them extensively over the next months with the help of the community.”

<http://www.srisc.com>

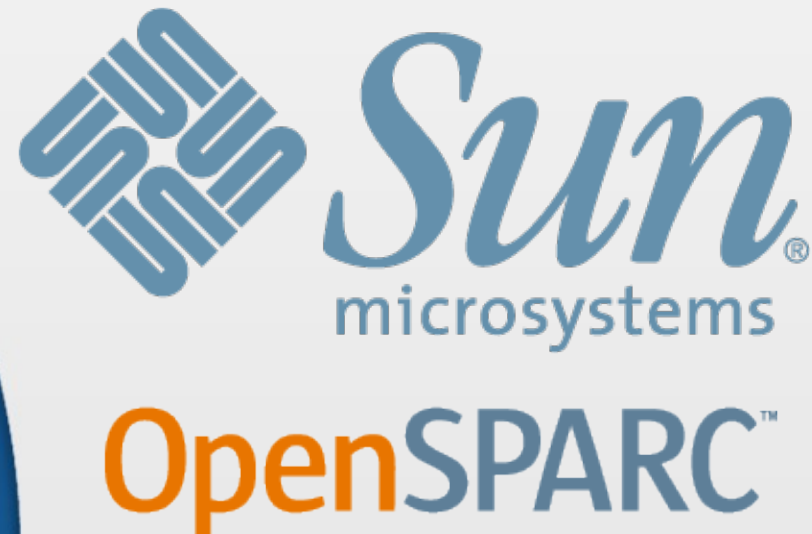


OpenSPARC Governance Board

- Initial Advisory Board announced Sept 2006
 - > 3 Community members:
 - > Nathan Brookwood, industry analyst (Insight64)
 - > Jose Renau, Univ. of California at Santa Cruz
 - > Robert Ober, Fellow, CTO Office, LSI Logic
 - > 2 members from Sun:
 - > Simon Phipps, Chief Open-Source Officer
 - > David Weaver, Principal Engineer, UltraSPARC Architecture
- Governance Board
 - > Advisory Board became initial Governance Board Jan'07
 - > New Board to be elected from Community in a year

Global OpenSPARC Program

- **World's Fastest Processors**
- **Leader in Chip Multi Threading**
- **The Only Open Source Processor on the Planet**
- **Commitment to R&D**



OpenSPARC participation

- Community Registration:
 - C <http://www.sunsource.net/servlets/Join>
After registration and confirming password, you can join the mailing lists:
<http://www.sunsource.net/servlets/ProjectMailingListsList>
- Forums:
 - F <http://forum.java.sun.com/category.jspa?categoryID=120>
(separate registration required for posting)

OpenSPARC participation

- Add your university (or company) to the marketplace:
<http://www.opensparc.net/community-marketplace/>
- Send us your profile and we'll post it:
<http://www.opensparc.net/profiles/>
- Add yourself to our Frappr!!:
<http://www.opensparc.net/frappr.html>
- Contribute to our OpenSPARC Book:
<http://wiki.opensparc.net/bin/view.pl/Main/Webhome> (separate registration required for editing)

Why OpenSPARC?

- View Excerpts from Education and Research Conference 2008, Carnegie Mellon University Professor Dr. James Hoe's highlights from the Panel Discussion at the ERC. (7:27) at

<http://www.opensparc.net/publications/videos/erc-highlights-dr.-james-hoe.html>



The screenshot shows the OpenSPARC website interface. At the top, the logo 'OpenSPARC™' is displayed in orange and blue, with the tagline 'World's First Free 64-bit CMT Microprocessors' in yellow and green. Below the logo is a navigation bar with buttons for 'Home', 'Get The Source', 'Get Informed' (highlighted), 'Get Connected', and 'Get Cool Tools'. Underneath, there are links for 'Get Involved' and 'Site'. A secondary navigation bar includes 'Home', 'Get Informed', 'Publications', 'Videos', and 'ERC Highlights - Dr. James Hoe' (highlighted). Below this are icons for 'Search', 'Contact Us', and 'About'. The main content area features the title 'ERC Highlights - Dr. James Hoe' in large orange text, with icons for PDF, print, and email on the right.

open

64 bit, 32 threads, free

<http://OpenSPARC.net>

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放
的
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OpenSPARC™

Thanks for Watching!
OPENSPARC SLIDE-CAST

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