microSPARC™-IIep Processor

OVERVIEW

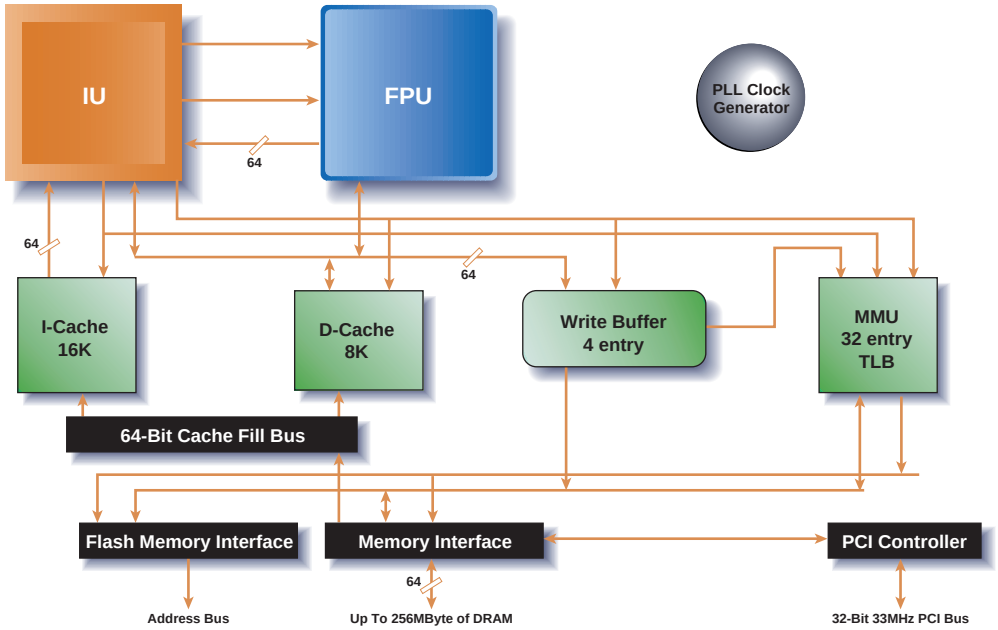
The microSPARC-IIep processor is a member of the SPARC™ processor family. Distingushed by its performance with low-cost applications and featuring a RISC architectural design, the microSPARC-IIep processor gives systems designers the advantage of a highly integrated SPARC system-on-a-chip.

The microSPARC-IIep processor integrates a 32-bit RISC processor with a floating-point unit. Its other features include: a memory management unit, separate instruction and data caches, a PCI bus controller, a DRAM and flash memory controller, and a clock generator using phase-locked loop on to a single device. Implemented with state-of-the-art CMOS technology, the microSPARC-IIep provides an ideal low-cost solution which is characterized by high-performance and low-power-consumption.

SPARC is the leading microprocessor technology supporting the hardware and software infrastructure of the Internet. As a member of the SPARC processor family, the microSPARC-IIep processor is supported by the industry's largest installed base of native RISC development environments, applications, and support tools. This makes the microSPARC-IIep an ideal microprocessor for your embedded and networked computing applications.

Features	Benefits
• Five stage SPARC 32-bit RISC pipeline	• Compatible with over 10,000 applications and existing development tools
• Support for little and big endian byte ordering	• Handles with ease PCI devices designed for DOS machines, along with UNIX® applications
• Operating frequency from 0-150 MHz (0.25µ) and 0-200 MHz (0.18µ)	• Targeted performance of 276K Dhrystone and 156 MIPS at 133 MHz
• 8-window, 136-word register file	• Fast interrupt response, procedure calls, and program execution
• Up to 16 Kbyte instruction cache and up to 8 Kbyte data cache	• Decouples processor operation from slow external memory
• Built-in floating-point unit	• Supports concurrent execution of floating-point and integer instructions
• Integrated 32-bit, 33 MHz PCI expansion bus controller	• Connection to industry-standard expansion bus
• Integrated DRAM controller	• High-bandwidth memory controller to reduce latency.
• Built-in 16 MByte flash memory controller	• Flash memory interface runs real-time operating systems; loading and running code out of ROM
• On-chip memory management unit	• Support for sophisticated operating systems with memory protection and virtual addressing
• Operating voltage of 3.3V with 5V compatible I/O, using a fully static design	• Low-power core reduces power consumption and supports industry standard peripherals
• Integrated power management circuitry	• Standby mode consumes less than ten percent nominal power consumption
• IEEE 1149.1 (JTAG) boundary scan test bus	• Ease of manufacturing tests

microSPARC-IIep Architecture



SPECIFICATIONS

SPARC™ VERSION 8 RISC architecture ; uniprocessor design

Operating frequency from 0-150 MHz (0.25µ) and 0-200 MHz (0.18µ)

Binary compatible with all SPARC application codes

Direct programmable DRAM interface

Direct interface to flash memory

Integrated PCI Rev 2.1 compliant expansion bus controller

Direct interface to PCI bus and support for up to 4 PCI slots

33 Mhz, 32-bit PCI bus

On-chip 16 Kbyte instruction cache and 8 Kbyte data cache

Fully static 3.3-volt core

5-volt compatible I/O pins

Typical power consumption of 4 watts

Power-down mode: < 10% nominal power consumption

Advanced 0.35 micron CMOS technology

2.2 million transistors

Estimated Performance

System Performance at 133 MHZ

Dhrystones 276K	
MIPS 156	

Maximum Bandwidth

DVMA (memory to PCI)	45 Mbytes/sec
DVMA (PCI to memory)	70 Mbytes/sec
Memory read (same page)	152 Mbytes/sec
Memory write (same page)	177 Mbytes/sec

TARGET APPLICATIONS

The microSPARC-IIep microprocessor is an ideal choice for control applications which are price/performance sensitive. Among the applications for which it can be used are: ASICs and semi-custom SOC applications such as digital set-top boxes, digital cameras, internet appliances, screen-phones, industrial controllers, automotive navigation devices, and graphic engines.

SUN COMMUNITY SOURCE LICENSE

Sun Microsystems now makes available via license its microSPARC-IIep processor technology, at no up-front cost to its world-wide developer community. Under the terms of this license the microSPARC-IIep processor technology can be downloaded via the Internet at Sun's Web site(www.sun.com). Information concerning this unique Sun program is found at: **http://www.sun.com/microelectronics/communitysource/**

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