TPS6501x Device Comparison

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ABSTRACT

This application report presents an overview on the differences between the TPS6501x family members. Devices included are the TPS65010, TPS65011, TPS65012, TPS65013, and TPS65014. It is intended to assist the design engineer in selecting the most suitable device for their application.

1 TPS6501x Family Members

The TPS6501x family members consist of several ICs that were derived from the TPS65010. Table 1 compares the parameters of the different family members. Table 1 shows the changes from TPS65010 in bold text.

Table 1. TPS6501x Family Members

	TPS65010	TPS65012	TPS65011	TPS65013	TPS65014
Wait mode (software programmable power down of VMAIN and VCORE)	No	Yes	Yes	**Yes**	Yes
Pushbutton-initiated Wait mode to power-on transition.	No	No	Yes	**Yes**	Yes
AC/USB Auto-start	No	No	Yes	**Yes**	Yes
Default VCORE voltages	DEFCORE = 1: VCORE = 1.6 V DEFCORE = 0 : VCORE = 1.5 V	DEFCORE = 1: VCORE = 1.6 V DEFCORE = 0 : VCORE = 1.5 V	*DEFCORE = 1: VCORE = **1.8 V*** DEFCORE = 0 : VCORE = 1.5 V	DEFCORE = 1: VCORE = 1.6 V **DEFCORE = 0 : VCORE = 1.3 V**	*DEFCORE = 1: VCORE = **1.8 V*** DEFCORE = 0 : VCORE = 1.5 V
Available VCORE voltages	0.85 V, 1 V, 1.1 V, 1.2 V, 1.3 V, 1.4 V, 1.5 V, 1.6 V	0.85 V, 1 V, 1.1 V, 1.2 V, 1.3 V, 1.4 V, 1.5 V, 1.6 V	0.85 V, 1 V, 1.1 V, 1.2 V, 1.3 V, 1.4 V, 1.5 V, **1.8 V**	0.85 V, **1.05 V**, 1.1 V, 1.2 V, 1.3 V, 1.4 V, 1.5 V, 1.6 V	0.85 V, 1 V, 1.1 V, 1.2 V, 1.3 V, 1.4 V, 1.5 V, **1.8 V**
Default VMAIN voltage	DEFMAIN = 1: VMAIN = 3.3 V DEFMAIN = 0: VMAIN = 3 V	DEFMAIN = 1: VMAIN = 3.3 V DEFMAIN = 0: VMAIN = 3 V	DEFMAIN = 1: VMAIN = 3.3 V DEFMAIN = 0: VMAIN = 3 V	DEFMAIN = 1: VMAIN = 3.3 V **DEFMAIN = 0: VMAIN = 1.8 V**	DEFMAIN = 1: VMAIN = 3.3 V DEFMAIN = 0: VMAIN = 3 V
Available VMAIN voltages	2.5 V, 2.75 V, 3 V, 3.3 V	2.5 V, 2.75 V, 3 V, 3.3 V	2.5 V, 2.75 V, 3 V, 3.3 V	**1.8 V**, 2.75 V, 3 V, 3.3 V	2.5 V, 2.75 V, 3 V, 3.3 V
Default VCORE voltage in low-power mode	1.1 V	1.1 V	1.1 V	**1.05 V**	1.1 V
Available VCORE voltage in low-power mode	0.85 V, 1 V, 1.1 V, 1.2 V	0.85 V, 1 V, 1.1 V, 1.2 V	0.85 V, 1 V, 1.1 V, 1.2 V	0.85 V, **1.05 V**, 1.1 V, 1.2 V	0.85 V, 1 V, 1.1 V, 1.2 V
LDO2 output voltage	1.8 V, 2.5 V, 2.75 V, 3 V 1.8 V = default at start-up	1.8 V, 2.5 V, 2.75 V, 3 V 1.8 V = default at start-up	1.8 V, 2.5 V, ***3 V, 3.3 V*** 1.8 V = default at start-up	1.8 V, 2.5 V, ***3.0 V, 3.3 V*** 1.8 V = default at start-up	1.8 V, 2.5 V, ***3 V, 3.3 V*** 1.8 V = default at start-up
UVLO default voltage	3.25 V	3.25 V	***2.75 V***	**2.75 V**	***2.75 V***
Available UVLO voltages	2.5 V, 2.75 V, 3 V, 3.25 V	2.5 V, 2.75 V, 3 V, 3.25 V	2.5 V, 2.75 V, 3 V, 3.25 V	2.5 V, 2.75 V, 3 V, 3.25 V	2.5 V, 2.75 V, 3 V, 3.25 V
UVLO hysteresis	175 mV	175 mV	***400 mV***	**400 mV**	***400 mV***
Default delay time for RESPWRON	1 s	1 s	**100 ms or 1 s set by pin 27 *(TPOR)***	**100 ms or 1 s set by pin 27 *(TPOR)***	**100 ms or 1 s set by pin 27 *(TPOR)***
RESPWRON source	LDO1	LDO1	***VMAIN***	**VMAIN**	**VMAIN**
Charger deglitch time	375 ms	375 ms	***23 ms***	**23 ms**	***23 ms***

Table 1. TPS6501x Family Members (continued)

	TPS65010	TPS65012	TPS65011	TPS65013	TPS65014
SCLK, SDAT, and LOW_PWR pin 1.8 V compliance	No	No	No	**Yes**	No
Interrupt if charger is removed	No	No	No	**Yes**	No
Recommended charge voltage	4.5 V to 5.5 V	4.5 V to 5.5 V	4.5 V to 5.5 V	4.5 V to 5.5 V	**4.5 V to 6.5 V**

TPS65010: This is the original device. It is compatible with the OMAP devices shown in Table A-1.

TPS65012: This device is similar to the TPS65010 with the additional Wait mode.

TPS65011: This device incorporates Wait mode at power up, which is mainly needed for smartphones and other systems in which the power supply does not automatically start when a battery is inserted.

TPS65013: This device is a variation of the TPS65011. The default VCORE voltages have been changed to 1.3 V and 1.6 V. The TPS65013 also generates an interrupt when both charger inputs are removed.

TPS65014: This device is a variation of the TPS65011. The only change is that the recommended charging voltage in the TPS65014 is increased from 5.5 V to 6.5 V.

2   TPS6501x Feature Description

2.1   Wait Mode

The TPS65011, TPS65012, TPS65013, and TPS65014 incorporate a condition called Wait mode. This mode allows a software initiated shutdown of the VMAIN and the VCORE converters. The LDOs may be independently enabled or disabled in Wait mode. The TPS65011, TPS65012, TPS65013, and TPS65014 can enter Wait mode at the command of the processor. The following sequence generates a processor shutdown to the Wait mode:

1. Set the ENABLE SUPPLY bit (register VDCDC1, bit B4) to *0*.
2. Set the ENABLE LP bit (register VDCDC1, bit B3) to *1*.
3. Pull the LOW _PWR pin (pin 36) high.

In the TPS65011,TPS65013, and TPS65014, if AC or USB are present, the AUA (AC/USB_ACTIVATION) bit (register CHGCONFIG, bit B7) must be set to *1* in order to stay in Wait mode.

Note that if the LDO1 OFF/nSLP and LDO2 OFF/nSLP bits (register VREGS1, bits B2 and B6) are set to *0*, the LDOs remain on in their reduced quiescent current mode. All registers retain their data in this mode. If these registers are set to *1* when Wait mode is entered, the LDOs turn off and all registers reset to their default values.

The TPS65011, TPS65013, and TPS65014 also enters Wait mode at initial power up when a voltage, typically the battery, is connected to the VCC pin.

2.2   Pushbutton-Initiated Wait Mode to Power-On Transition

The TPS65011, TPS65013, and TPS65014 incorporate a function that keeps the IC in Wait mode at turnon until either USB or AC power is applied, or either PB_ONOFF or HOT_RESET are asserted. Before exiting Wait mode, the BATT_COVER pin must be high and the voltage at VCC must be greater than the default UVLO voltage. When the IC leaves the Wait mode, it turns on the VMAIN and VCORE converts according to the sequencing defined by the PS_SEQ pin.

This function is useful when the designer does not want the system to automatically start when a battery is applied.

2.3 AC/USB Auto-Start

The TPS65011, TPS65013, and TPS65014 incorporate AC/USB Auto-Start. When in Wait mode, the IC is automatically enabled (goes into *ON* mode) when a voltage is applied to the AC or USB charger inputs.

Note that if the AUA bit (register CHGCONFIG, bit B7) is set to *1*, the IC stays in Wait mode even if a voltage is applied to the AC or USB inputs.

2.4 Default VCORE Voltage

Some TPS6501x family members support slightly different VCORE voltages at start-up in order to support different processors, and a large number of applications. See Table 1 for the specific default voltages at start-up. The two default VCORE voltages (programmed by DEFCORE, pin 1) can be reprogrammed after start-up.

2.5 Available VCORE Voltages

After start-up, the user can reprogram the VCORE output voltages to one of the levels shown in Table 1.

2.6 Default VMAIN Voltage

Some TPS6501x family members support slightly different VMAIN voltages at start-up in order to support different peripherals. See Table 1 for the specific default voltages at start-up. The two default VMAIN voltages (programmed by DEFMAIN, pin 12) can be reprogrammed after start-up.

2.7 Available VMAIN Voltages

After start-up, the user can reprogram the VMAIN output voltages to one of the levels shown in Table 1.

2.8 Default VCORE Voltage in Low-Power Mode

The default VCORE voltage in low-power mode is shown in Table 1.

2.9 Available VCORE Voltage in Low-Power Mode

After start-up, the user can reprogram the VCORE voltage in low-power mode to one of the levels shown in Table 1.

2.10 LDO2 Output Voltage

Some TPS6501x family members support slightly different LDO2 voltages in order to support different peripherals. See Table 1 for the specific voltages for each device.

2.11 UVLO Default Voltage

The TPS6501x family has undervoltage lockout (UVLO) that is separately programmable from the fixed charger UVLO. See Table 1 for the default UVLO voltage and available UVLO voltages. The lower default UVLO voltage, (2.75 V) for the TPS65011, TPS65013, and TPS65014, allows the ICs to be started with a nearly depleted battery.

2.12 Available UVLO Voltages

After start-up, the user can reprogram the UVLO voltage to one of the levels shown in Table 1.

2.13 UVLO Hysteresis

The UVLO circuit has hysteresis. This hysteresis ensures that all power supply outputs remain off until after the charger has charged the battery enough to exit the precharge mode. The VCC pin must rise above the UVLO voltage plus the hysteresis before the converters start. For example, the voltage on the TPS65011 VCC pin must rise to above 2.75 V + 0.4 V = 3.15 V before the converters are allowed to start.

2.14 Default Delay Time for $\overline{RESPWRON}$

The TPS65010 and TPS65012 default $\overline{RESPWRON}$ time is internally set to 1 s. After start-up, this can be reprogrammed to 69 ms by the POR bit (register CHGCONFIG, bit B7). The TPS65011 and TPS65013 default $\overline{RESPWRON}$ time is externally set by TPOR (pin 27). The $\overline{RESPWRON}$ time cannot be changed with the internal registers. Note that pin 27 is not connected on the TPS65010 and TPS65012.

2.15 RESPWRON Source

With the TPS65010 and TPS65012, $\overline{RESPWRON}$ is driven by the LDO1 PGOOD comparator. With the TPS65011, TPS65013, and TPS65014, $\overline{RESPWRON}$ is driven by the VMAIN PGOOD comparator. For the TPS65011, TPS65013, and TPS65014, when VMAIN is the highest system voltage, $\overline{RESPWRON}$ is asserted as long as the battery does not have enough charge to support all voltage rails. $\overline{RESPWRON}$ is activated for 80 µs to 120 µs after the appropriate PGOOD comparator detects an undervoltage condition.

2.16 Charger Deglitch Time

In the TPS65011, TPS65013, and TPS65014, all deglitch timers have been reduced from 375 ms to 23 ms. The AC to USB deglitch timer has been reduced to 5 ms.

This allows the TPS65011, TPS65013, and TPS65014 to start up and power the applications processor within 100 ms in order to respond to a USB connection applied.

2.17 SCLK, SDAT, GPIO, and LOW_PWR Pin 1.8-V Compliance

The TPS65010, TPS65011, TPS65012, and TPS65014 control signals are not compatible with 1.8-V logic. Logic *1* is defined as an input voltage greater than 2 V. Logic *0* is defined as an input voltage less than 0.8 V.

The TPS65013 control signals are 1.8-V compatible. Logic 1 is defined as an input voltage greater than 1.2 V. Logic 0 is defined as an input voltage less than 0.4 V.

2.18 Interrupt if Charger is Removed

The TPS65013 generates an interrupt signal when the last charging source is removed. This feature is disabled by default and can be masked by the internal register MASK2.

2.19 Recommended AC Charge Voltage

The TPS6501x family V(AC) charger input is capable of withstanding up to 20-V transients and features nonlatching overvoltage protection on the V(AC) input. The charger function is turned off if an overvoltage is detected. The charger resumes normal operation when the fault condition is removed. The TPS65010 through TPS65013 chargers are disabled if the V(AC) input exceeds a 5.5-V minimum threshold, 6.6 V typical. The TPS65014 charger is disabled if the V(AC) input exceeds a 6.5-V minimum threshold, 7 V typical.

2.20 References

1. TPS65010 data sheet (SLVS149)
2. TPS65011 data sheet (SLVS501)
3. TPS65012 data sheet (SLVS504)
4. TPS65013 data sheet (SLVS517)
5. TPS65014 data sheet (SLVS551)

Appendix A Compatible Devices

Table A-1 shows several OMAP devices that are compatible with the TPS6501x family.

Table A-1. TPS6501x-Compatible OMAP Devices

DEVICE	MIN CORE VOLTAGE (V)	TYP CORE VOLTAGE (V)	MAX CORE VOLTAGE (V)	MAX CORE CURRENT (mA)
OMAP730	1.425	1.5	1.575	300
OMAP750	1.425	1.5	1.575	300
OMAP850	1.425	1.5	1.575	300
OMAP1510	1.425	1.5	1.575	300
	1.525	1.6	1.675	320
	1.525	1.6	1.675	320
	1.375	1.6	1.675	320
OMAP330	1.425	1.5	1.575	200
	1.52	1.6	1.68	213
	1.52	1.6	1.68	213
OMAP1610	1.425	1.5	1.75	300
	1.5	1.6	1.65	320
OMAP1611/12	1.425	1.5	1.75	300
	1.525	1.6	1.75	320
OMAP1621	1.525	1.6	1.75	300
OMAP1623	1.425	1.5	1.75	300
	1.525	1.6	1.75	320
	1.525	1.6	1.75	320
OMAP331	1.52	1.6	1.68	250
OMAP1710	1.235	1.30	1.365	330

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