Small, Dynamic Voltage Management Solution Based on TPS62300 High-Frequency Buck Converter and DAC6571

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ABSTRACT

As cellular phones and other portable electronics become more complex, more power is consumed by both active and standby systems. Consequently, power management design for portable devices offers new challenges in core voltage, energy management, and battery lifetime.

Hardware designers already have started to use advanced and highly integrated power management devices featuring core voltage scaling and various voltage regulators to supply other rails (e.g., memory, I/Os, etc.). Nevertheless, these complex solutions do not necessarily offer enough flexibility to systems designers.

This application report describes an innovative way to tackle the dynamic voltage management problem based on the TPS62300, TI's first generation of high-frequency step-down converters.

Contents

Figures

Tables

1 System Overview

Most modern processors targeting portable applications have an integrated I^2C serial interface to control their external power management unit. Figure 1 shows an alternative solution to generate an adaptive core power supply. The power consumed by processor cores is proportional to the operating frequency and to V_{CORE}^2.

This two-chip solution based on the TPS62300 (3-MHz synchronous step-down converter) and the DAC6571 (10-bit digital-to-analog converter) combines high accuracy and ultra-small voltage stepping size.

Depending on the operating frequency of the processor, the core voltage can be dynamically and accurately adapted to its lower limit in order to minimize power consumption. This principle can be used not only to reduce power consumption in active mode, but also to extend standby time through a reduction of leakage current effects in deep-sleep mode.

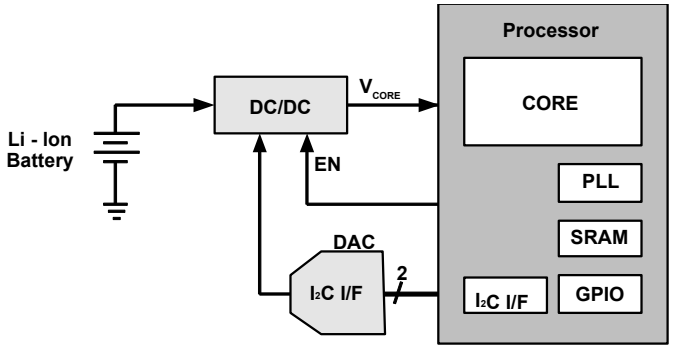

Figure 1. System Overview Adaptive Voltage Scaling

2 Step-Down Converter for Core Power Supply

The TPS62300 is the first product of a new generation of high-frequency step-down converters operating at 3-MHz switching frequency. The best-in-class transient response and output voltage accuracy meet the tightest voltage specifications required by modern cores.

The TPS62300 converter can operate with inductors down to 1 μH and output capacitors as low as 4.7 μF allowing the use of tiny and low-cost chip inductors. Along with its chip scale packaging (2 mm x 1 mm x 0,65 mm), the device fulfills mobile phone manufacturer needs when small and low-profile solution size becomes a key factor.

3 Dynamic Voltage Scaling

Figure 2 shows a simplified block diagram of TPS62300 converter that illustrates the gain architecture and control-loop design of the device. One noticeable departure from conventional regulators is the means by which the output voltage is set.

Conventionally, a reference voltage is applied to the positive terminal of an error amplifier, and the desired output voltage is programmed by sensing the output voltage and dividing it down to the reference voltage by means of external resistors.

The TPS62300 generates its output by amplifying the reference voltage (V_{REF} = 400 mV) up to 2/3 of the required output voltage by means of an internal low-power, low-offset operational amplifier and external resistor programming. This voltage becomes the reference for the power train that has a DC closed-loop gain (A_{PT}) of 1.5.

A fixed closed-loop gain in the power amplifier not only gives a constant small-signal transient response, irrespective of the programmed output voltage, but also leads to tight regulation tolerances and robustness in respect to L/C combinations.

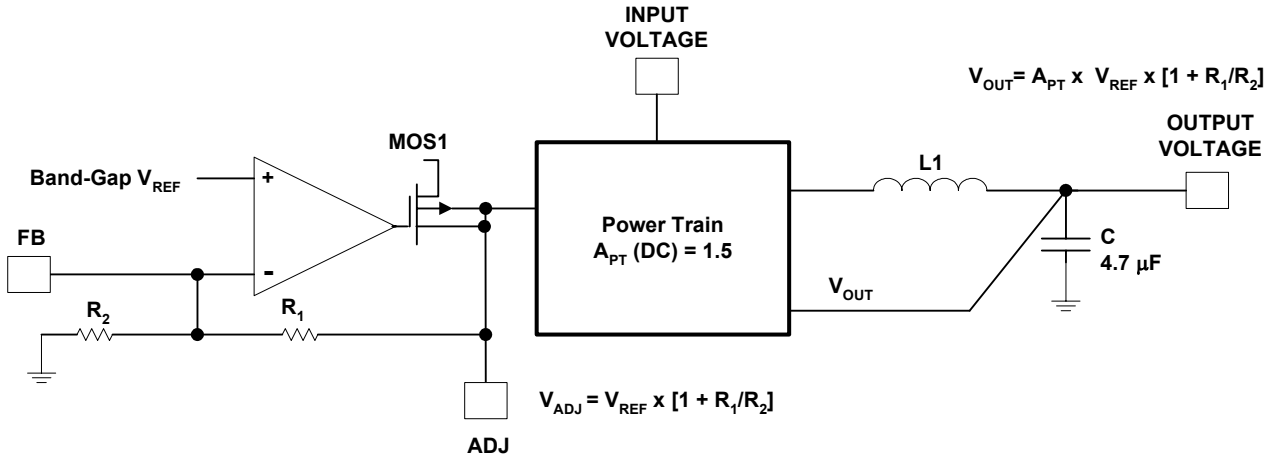

Figure 2. TPS62300 Simplified Block Diagram

Figure 3 details the implementation of the operational amplifier used to amplify the band-gap reference voltage. This low-offset operational amplifier can be seen as an ideal amplifier with a class-A output stage that has the characteristic to be able to source but not to sink current.

To act as a linear system with negative feedback, the band-gap buffer amplifier would need to be operated with a DAC voltage below V_{REF} (400 mV). Only in this case, current flows out of the ADJ pin towards GND via the R_1 and R_2 resistors.

Assuming that the DAC voltage is higher than V_{REF}, V_{REF} implies that a current is circulating the opposite way through R_1 and R_2 into the ADJ pin. Because the operational amplifier output stage (MOS1) can only source current, it cannot operate in linear mode any longer. In this case, the MOS1 transistor used in a voltage follower configuration has high impedance. Actually, to override the ADJ voltage, it is simply necessary to keep the FB potential above the internal reference voltage (V_{REF}).

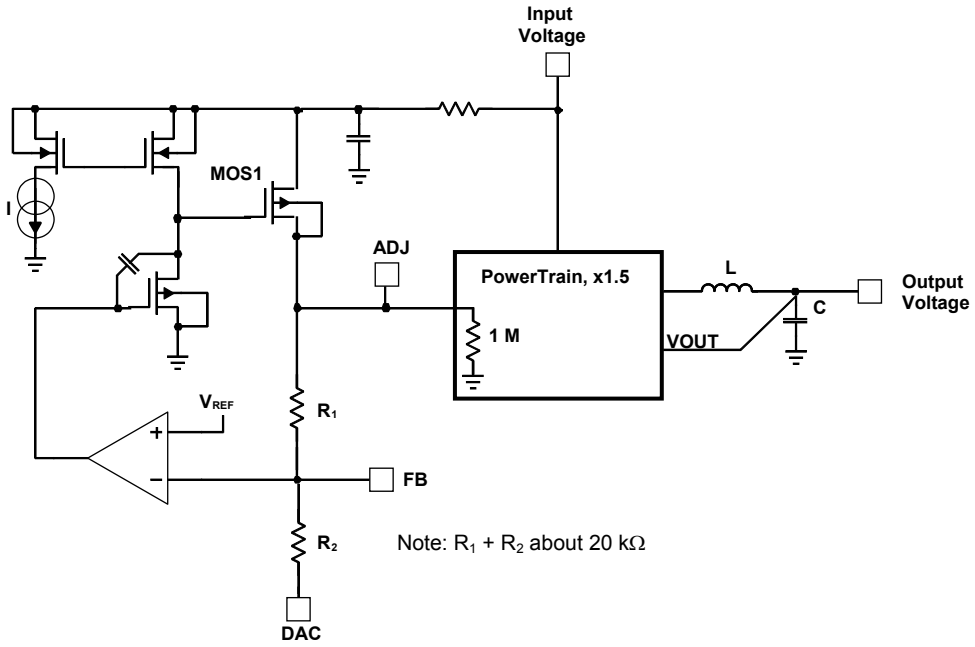

Figure 3. TPS62300 Reference Voltage Amplifier

When the ADJ voltage is overridden by the DAC, the external default voltage-setting resistors R_1 and R_2 need to be considered with respect to the resistance into the ADJ pin (1 MΩ ±30%).

In fact, R_1 and R_2 in series are forming a voltage divider with the resistance into the ADJ pin. To achieve 1% DC accuracy over temperature, line, and load variations, it is recommended to select R_1 + R_2 in the 20-kΩ range.

Table 1 summarizes the operation of the power converter.

Table 1. Power Converter Operation Summary

DAC Voltage (mV)	ADJ Voltage (mV)	DC/DC Output Voltage (mV)	Remarks
0	$V_{ADJ} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$	$V_{OUT} = A_{PT} \times V_{REF} \times \left(1 + \frac{R1}{R2}\right)$	Set default output voltage
< 400 mV	$V_{ADJ} = V_{REF} + \frac{R1}{R2}(V_{REF} - V_{DAC})$	$V_{OUT} = A_{PT} \times \left[V_{REF} + \frac{R1}{R2}(V_{REF} - V_{DAC})\right]$	
> 400 mV	$V_{ADJ} = V_{DAC} \times \left(\frac{1M\Omega}{1M\Omega + R1 + R2}\right)$	$V_{OUT} = A_{PT} \times V_{DAC} \times \left(\frac{1M\Omega}{1M\Omega + R1 + R2}\right)$	MOS1 high-impedance, override ADJ pin

Note 1. Internal reference voltage V_{REF} typical = 400 mV

Note 2. DC power train amplification A_{PT} typical = 1.5

Figure 4 shows TPS62300 output voltage response vs. DAC voltage. For best performance in dynamic voltage management applications, operating with a DAC voltage above 450 mV is recommended.

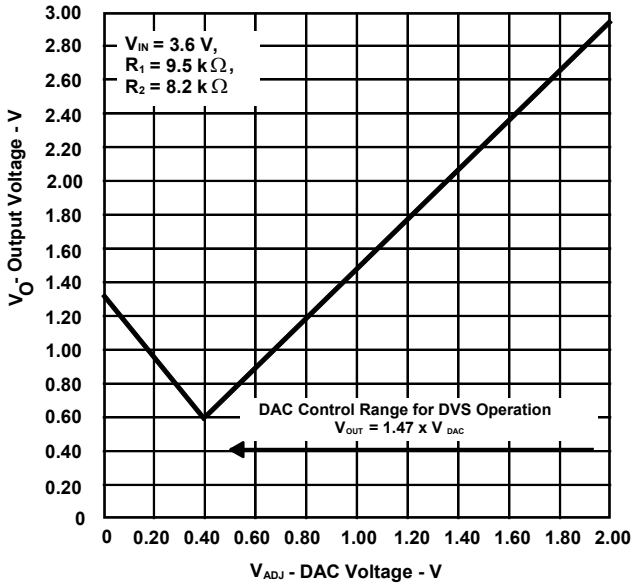

Figure 4. Output Voltage vs. DAC Control Voltage

4 I²C Controlled Adaptive Voltage Scaling: How it Works

Figure 5 shows circuit implementation based on TPS62300 and DAC6571. The TPS62300 can provide up to 500-mA output current and output voltage as low as 0.6 V.

The 10-bit D/A converter DAC6571 comes in a small 6-pin SOT23 package. This device is part of TI's single-channel D/A converter family DAC7571/6571/5571 providing a 12/10/8-bit resolution. These products integrate an I^2C interface supporting standard/fast mode (up to 400 kbps) and high-speed mode (up to 3.4 Mbps). At power up, the integrated power-on-reset circuitry sets the output voltage to 0 V.

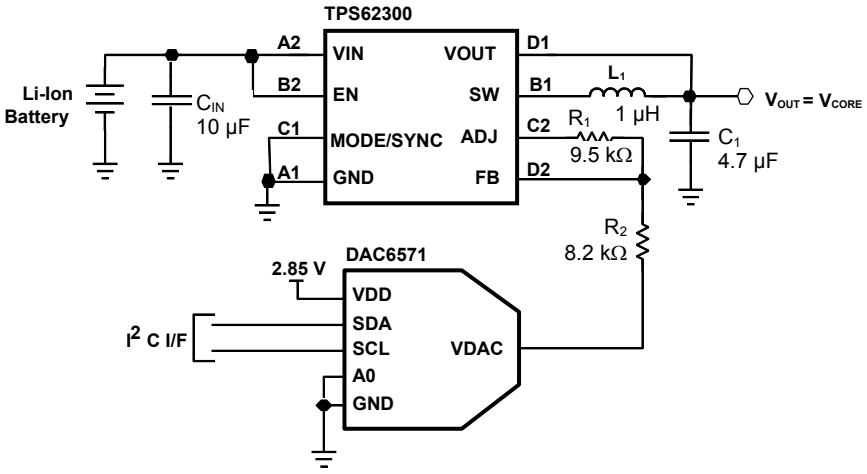

Figure 5. Application Circuit for Dynamic Management

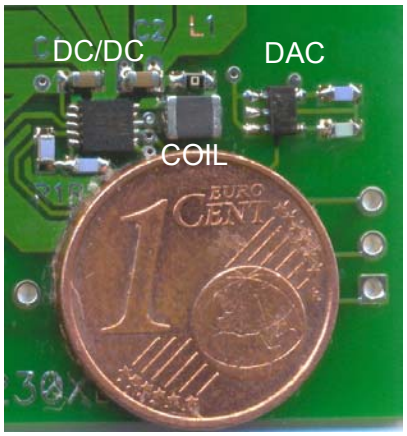

Figure 6. Application PCB

In this application, the TPS62300 is directly powered from a single-cell, Li-ion battery. The DAC6571 is supplied by a regulated voltage, in this case, 2.85 V. This supply voltage can be derived from another system rail. The architecture of the D/A converter is based on an R/2R resistor string, specified monotonic by design.

For the core supply voltage, two different operating modes need to be considered:

- Default output voltage:

  This voltage is valid after power-on-reset of the DAC at start-up. As long as the DAC has not been programmed via I^2C interface, its output voltage stays at 0 V. During this phase, the core voltage is defined by the resistors R_1 and R_2, according to the formula listed in Table 1 (see default output voltage).

- DAC-controlled output voltage:

In this mode, the D/A converter output voltage should be programmed higher than 0.45 V to take advantage of the “override” function. In this mode, the core supply voltage can be calculated according to the formula listed in Table 1 (MOS1 high impedance).

The output voltage of the DAC6571 can be determined by Equation 1:

$$V_{DAC} = V_{DD} \times \left(\frac{D}{1024} \right) \quad (1)$$

Where:

D = Decimal equivalent of the binary code loaded into the DAC register; it can range from 0 to 1023.

And:

V_{DD} = DAC supply voltage

The core voltage V_{OUT} in DAC-controlled mode can therefore be calculated by Equation 2.

$$V_{out} = V_{DD} \times \left(\frac{D}{1024} \right) \times A_{PT} \times \left(\frac{1M\Omega}{1M\Omega + R_1 + R_2} \right) \quad (2)$$

With DC power train amplification A_{PT} typical = 1.5

Figure 7 illustrates V_{DAC} (DAC output voltage) and V_{OUT} (core voltage) depending on the DAC programming value.

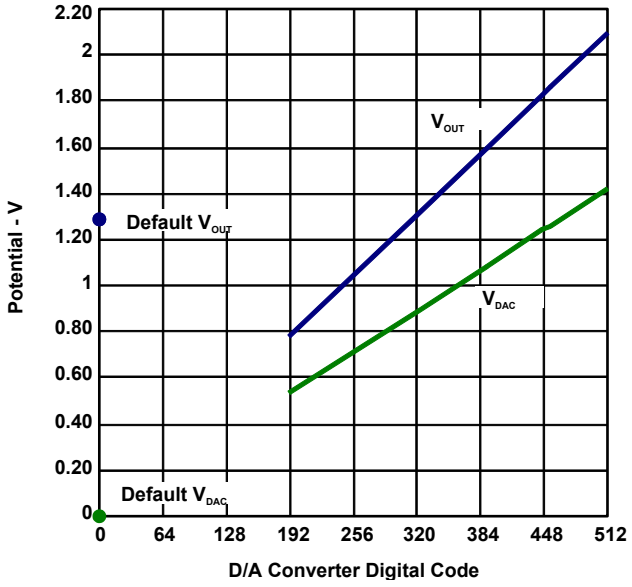

Figure 7. V_{DAC} and V_{OUT} vs. DAC Value

In this application, a default core voltage of 1.3 V has been selected. Therefore, the necessary resistor values for R1 and R2 need to be:

R1: 9.5 kΩ
R2: 8.2 kΩ

The default core voltage adjustment during power up is shown in Figure 8. The TPS62300 powers a resistive load of 3.9 Ω which results in a load current of 330 mA at 1.3-V default output voltage. In Figure 8, the enable pin (EN) of the DC/DC converter is driven high together with V_{IN}. The core voltage ramps up with a minimum delay. Modern processors, however, are able to generate control signals to start up external core supply circuits by themselves. In this case, the processor controls the enable pin of TPS62300.

After the core voltage has ramped up to its default value and the processor is operating, the core voltage can be dynamically adjusted. In order to reduce power consumption and to extend battery lifetime, the processor clock and core voltage can be adapted to the optimum.

Figure 9 and Figure 10 show scope snapshots of V_{OUT} during a step-up/down voltage scaling. This application executes the transition between a floor level of 1 V and a roof level of 1.5 V in less than 20 µs. Furthermore, the advanced regulation of the TPS62300 provides best-in-class line transient response, which results in minimized voltage over/undershoots during core voltage adaptation.

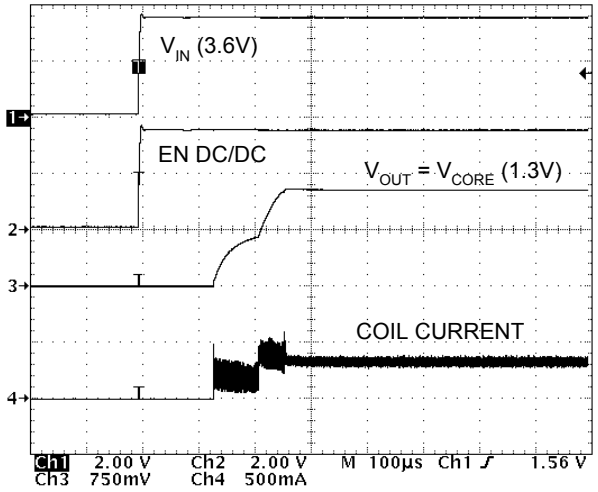

Figure 8. Default Core Voltage V_{OUT} Set to 1.3 V at Power Up

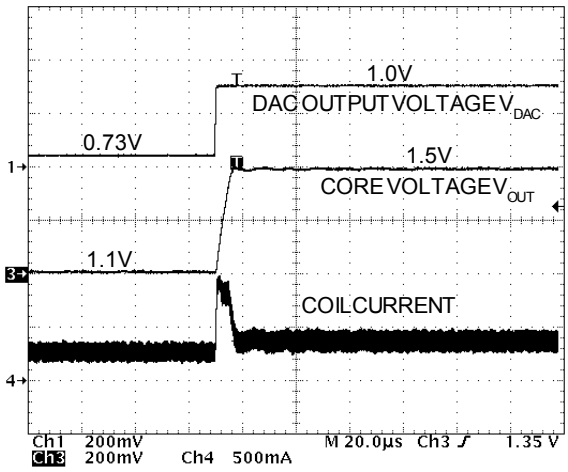

Figure 9. Core Voltage Step From 1.1 V to 1.5 V

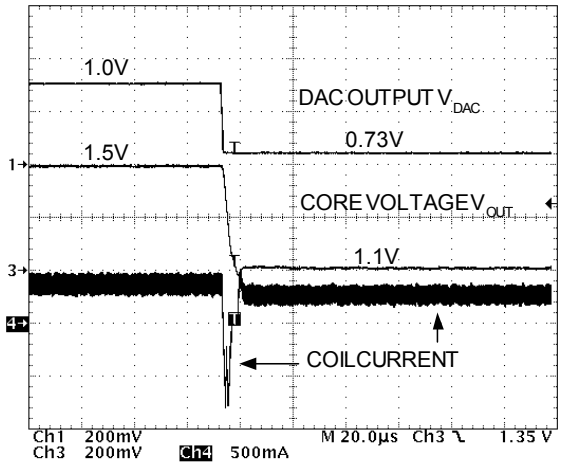

Figure 10. Core Voltage Step From 1.5 V to 1.1 V

5 Conclusion

This solution for dynamic voltage management supports fast and accurate voltage scaling as required by today's and next-generation processor cores. It is controlled via the I^2C serial interface, which is a common interface for this purpose. The small packages of the TPS62300 and DAC6571 and the few external components allow a small solution size. The best-in-class load and line transient performance of TPS62300 makes this device ideally suited for core supplies of modern and next-generation processors.

6 References

1. *TPS623xx, 500-mA, 3-MHz Synchronous Step-Down Converter in Chip Scale Packaging* data sheet (SLVS528)
2. *DAC6571, +2.7-V to +5.5-V, I^2C Interface, Voltage Output, 10-Bit Digital-to-Analog Converter* data sheet (SLAS406)

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