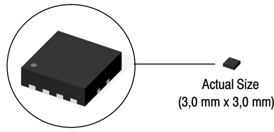


HIGH INPUT VOLTAGE, MICROPOWER SON PACKAGED 80-mA LDO LINEAR REGULATORS

FEATURES

- **24-V Maximum Input Voltage**
- **Low 3.2-μA Quiescent Current at 80 mA**
- **Stable With Any Capacitor (> 0.47 μF)**
- **80-mA Specified Current**
- **Available in Fixed and Adjustable (1.2V to 15V) Versions**
- **Specified Current Limit**
- **3mm x 3mm SON Package**
- **–40°C to +125°C Specified Junction Temperature Range**
- **For MSP430-Specific Output Voltages see TPS715xx**

APPLICATIONS

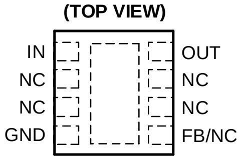
- **Ultralow Power Microcontrollers**
- **Industrial/Automotive Applications**
- **PDAs**
- **Portable, Battery-Powered Equipment**

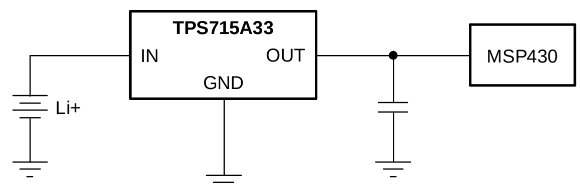
DESCRIPTION

The TPS715Axx low-dropout (LDO) voltage regulators offer the benefits of high input voltage, low-dropout voltage, low-power operation, and miniaturized packaging. The devices, which operate over an input range of 2.5 V to 24 V, are stable with any capacitor (≥ 0.47 μF). The high maximum input voltage combined with excellent power dissipation capability makes this part particularly well-suited to industrial and automotive applications.

A PMOS pass element behaves as a low-value resistor. The low dropout voltage, typically 670 mV at 80 mA of load current, is directly proportional to the load current. The low quiescent current (3.2 μA typically) is nearly constant over the entire range of output load current (0 mA to 80 mA).

DRB PACKAGE
3mm x 3mm SON
(TOP VIEW)





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS[1]

PRODUCT	V_{OUT}[2]
TPS715A**xxyyz**	**XX** is nominal output voltage (for example 33 = 3.3V, 01 = Adjustable) **YY** is Package Designator **Z** is Package Quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Custom output voltages from 1.25 V to 5.4 V in 50 mV increments are available on a quick-turn basis for prototyping. Production quantities are available; minimPackageum order quantities apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)[1]

	UNIT
V_{IN} range	–0.3 V to +24 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Junction temperature range, T_J	–40°C to +150°C
Storage temperature range	–65°C to +150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

POWER DISSIPATION RATING TABLE

BOARD	PACKAGE	$R_{\theta JA}$°C/W	DERATING FACTOR ABOVE T_A = +25°C	$T_A \leq$ 25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
High-K[1]	DRB	65	15.4 mW/°C	1.54 W	0.85 W	0.62 W

(1) The JEDEC High-K (2s2p) board design used to derive this data was a 3 inch × 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

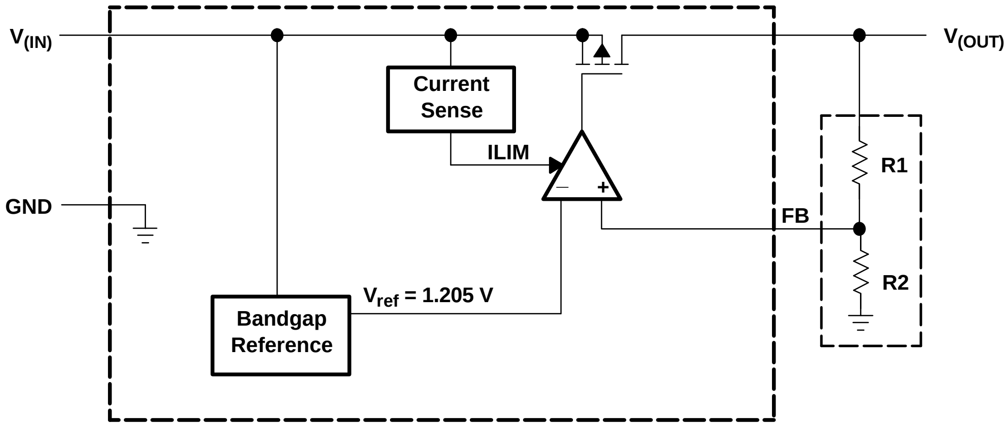
ELECTRICAL CHARACTERISTICS

Over operating junction temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(NOM)}$ + 1 V, I_{OUT} = 1 mA, C_{OUT} = 1 µF, unless otherwise noted. The TPS715A01 is tested with V_{OUT} = 2.8 V. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage(1)	V_{IN}	I_{OUT} = 10 mA	2.5		24	V
		I_{OUT} = 80 mA	3		24	
Voltage range (TPS715A01)	V_{OUT}		1.2		15	V
Output voltage accuracy(1)	TPS715A01	V_{OUT} + 1.0 V ≤ V_{IN} ≤ 24 V, 1.2 V ≤ V_{OUT} ≤ 15 V, 0 ≤ I_{OUT} ≤ 80 mA	0.96 × $V_{OUT(nom)}$	$V_{OUT(nom)}$	1.04 × $V_{OUT(nom)}$	V
	TPS715A33	4.3 V < V_{IN} < 24 V, 0 ≤ I_{OUT} ≤ 80 mA	3.135	3.3	3.465	
Output voltage line regulation(1)	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} + 1 V < V_{IN} ≤ 24 V		20	60	mV
Load regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 µA to 80 mA		35		mV
Dropout voltage $V_{IN} = V_{OUT(NOM)}$ – 0.1 V	V_{DO}	I_{OUT} = 80 mA		670	1120	mV
Output current limit	I_{CL}	V_{OUT} = 0 V	160		1100	mA
Ground pin current	I_{GND}	T_J = –40°C to +85°C, 0 mA ≤ I_{OUT} ≤ 80 mA		3.2	4.2	µA
		0 mA ≤ I_{OUT} ≤ 80 mA		3.2	4.8	
		V_{IN} = 24 V, 0 mA ≤ I_{OUT} ≤ 80 mA			5.8	
Power-supply ripple rejection	PSRR	f = 100 kHz, C_{OUT} = 10 µF		60		dB
Output noise voltage	V_{IN}	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$, or the value shown for *Input voltage*, whichever is greater.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION

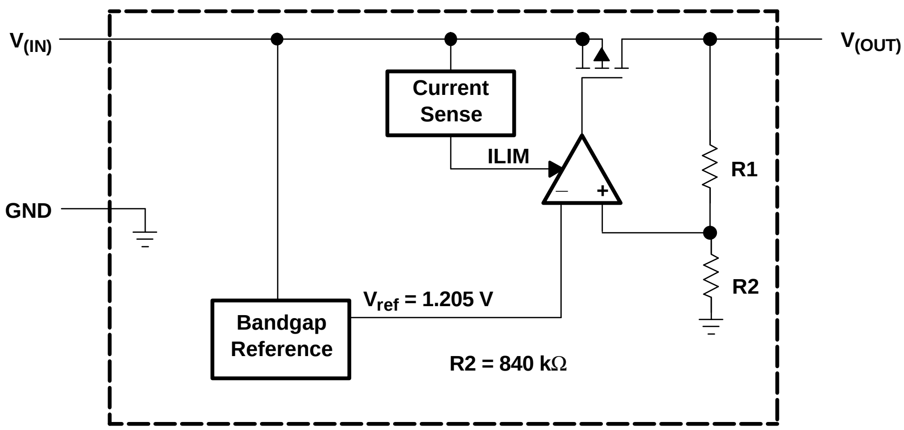


Table 1. Terminal Functions

TERMINAL			DESCRIPTION
NAME	NO.		
	FIXED	ADJ.	
FB		5	Adjustable version. This terminal is used to set the output voltage.
GND	4	4	Ground
NC	2, 3, 5-7	2, 3, 6, 7	No connection
IN	1	1	Unregulated input voltage.
OUT	8	8	Regulated output voltage, any output capacitor ≥ 0.47 μF can be used for stability.

TYPICAL CHARACTERISTICS

**TPS715A33
OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

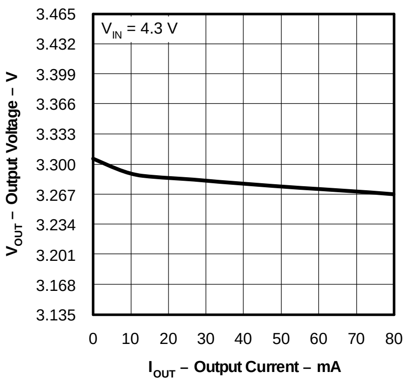


Figure 1.

**TPS715A33
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE**

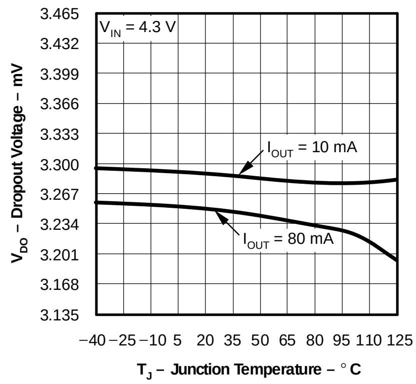


Figure 2.

**QUIESCENT CURRENT
vs
JUNCTION TEMPERATURE**

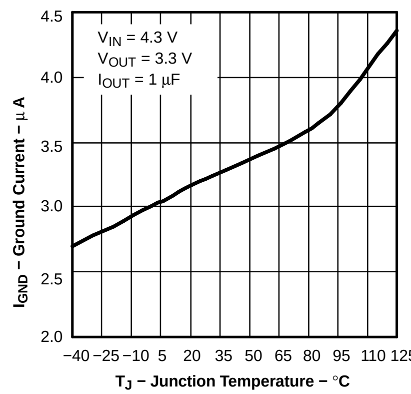


Figure 3.

**OUTPUT SPECTRAL
NOISE DENSITY
vs
FREQUENCY**

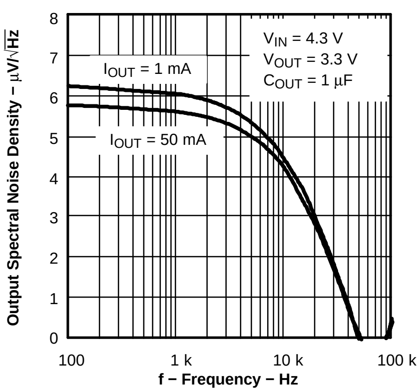


Figure 4.

**OUTPUT IMPEDANCE
vs
FREQUENCY**

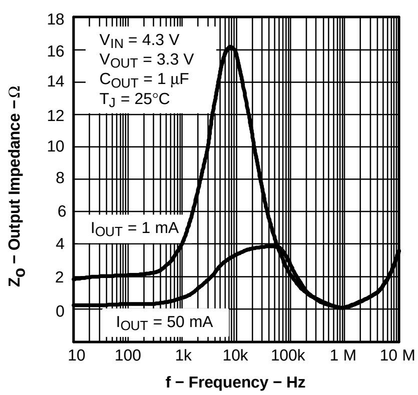


Figure 5.

**TPS715A33
DROPOUT VOLTAGE
vs
OUTPUT CURRENT**

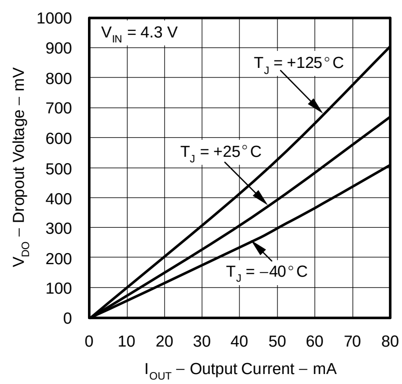


Figure 6.

**TPS71501
DROPOUT VOLTAGE
vs
INPUT VOLTAGE**

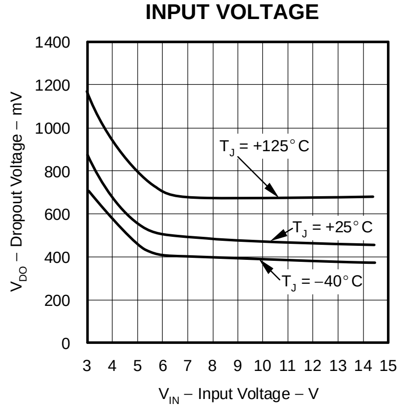


Figure 7.

**TPS715A33
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE**

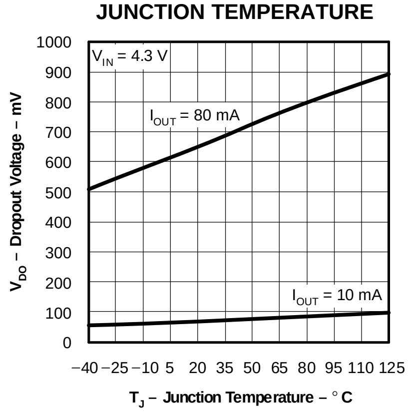


Figure 8.

**CURRENT LIMIT
vs
V_{OUT}**

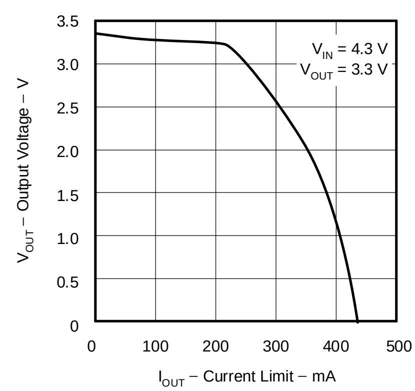


Figure 9.

TYPICAL CHARACTERISTICS (continued)

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY

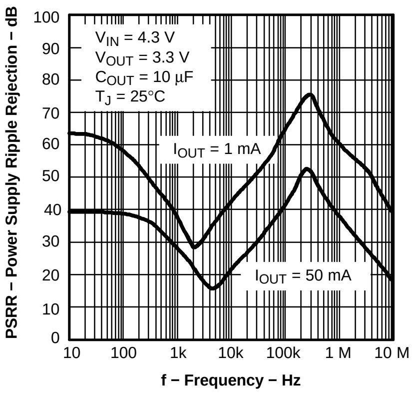


Figure 10.

POWER UP / POWER DOWN

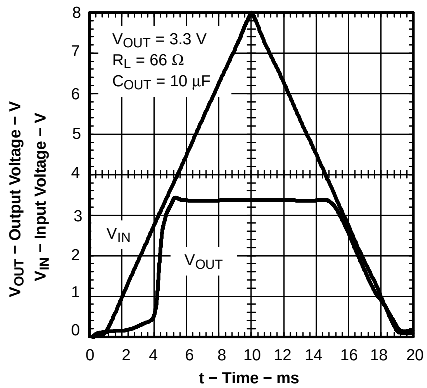


Figure 11.

LINE TRANSIENT RESPONSE

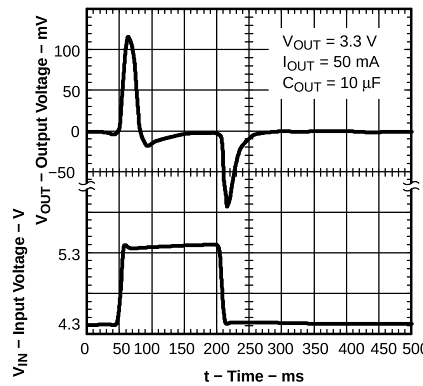


Figure 12.

LOAD TRANSIENT RESPONSE

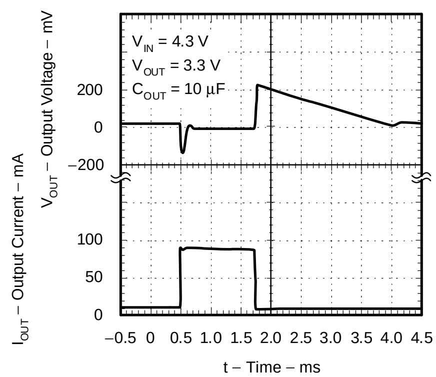


Figure 13.

APPLICATION INFORMATION

The TPS715Axx family of LDO regulators has been optimized for ultra low power applications such as the MSP430 microcontroller. Its ultralow supply current maximizes efficiency at light loads, and its high input voltage range makes it suitable for supplies such as unconditioned solar panels.

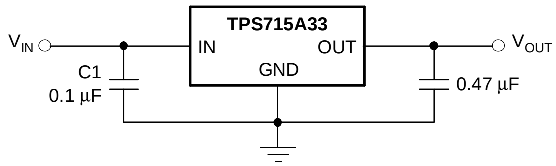


Figure 14. Typical Application Circuit (Fixed Voltage Version)

External Capacitor Requirements

Although not required, a 0.047-µF or larger input bypass capacitor, connected between IN and GND and located close to the device, is recommended to improve transient response and noise rejection of the power supply as a whole. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and if the device is located several inches from the power source.

The TPS715Axx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. Any capacitor (including ceramic and tantalum) that is ≥ 0.47 µF properly stabilizes this loop.

Power Dissipation and Junction Temperature

To ensure reliable operation, worst-case junction temperature should not exceed 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 1:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the Dissipation Rating table).
- T_A is the ambient temperature.

The regulator dissipation is calculated using Equation 2:

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \quad (2)$$

Power dissipation resulting from quiescent current is negligible.

Regulator Protection

The TPS715Axx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS715Axx features internal current limiting. During normal operation, the TPS715Axx limits output current to approximately 500 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. Take care not to exceed the power dissipation ratings of the package.

APPLICATION INFORMATION (continued)

Programming the TPS71501 Adjustable LDO Regulator

The output voltage of the TPS715A01 adjustable regulator is programmed using an external resistor divider as shown in Figure 15. The output voltage is calculated using Equation 3:

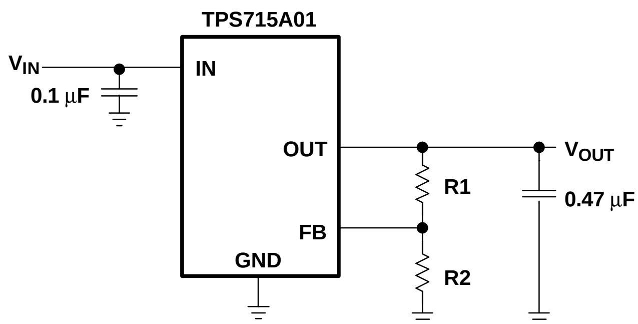
$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

where:

- V_{REF} = 1.205 V typ (the internal reference voltage)

Resistors R1 and R2 should be chosen for approximately 1.5-μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 1 MΩ to set the divider current at 1.5 μA, and then calculate R1 using Equation 4:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (4)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2
1.8 V	392 MΩ	806 kΩ
2.8 V	1.07 MΩ	806 kΩ
5.0 V	2.55 MΩ	806 kΩ

Figure 15. TPS715A01 Adjustable LDO Regulator Programming

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS715A01DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS715A01DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS715A01DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS715A01DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS715A33DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS715A33DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS715A33DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS715A33DRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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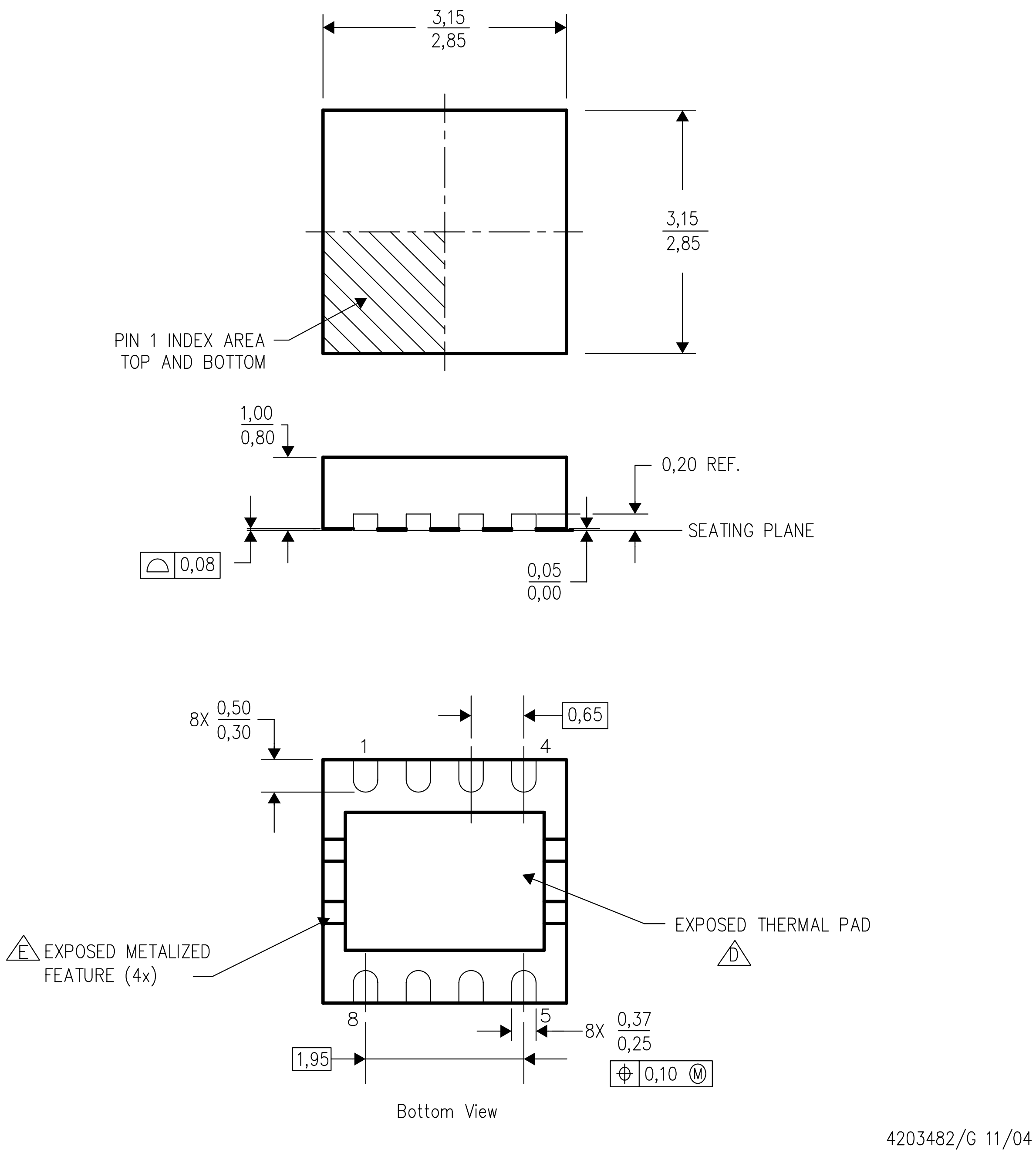
DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



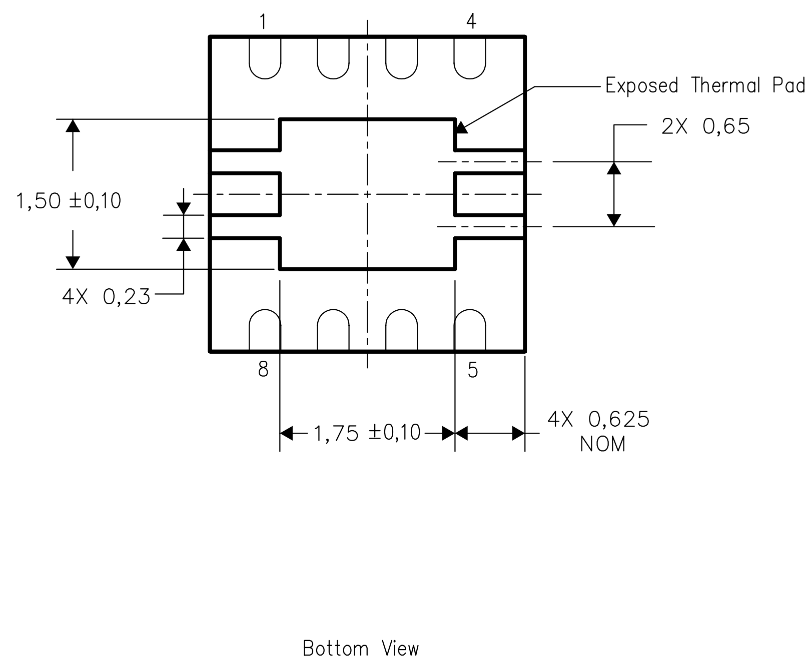
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

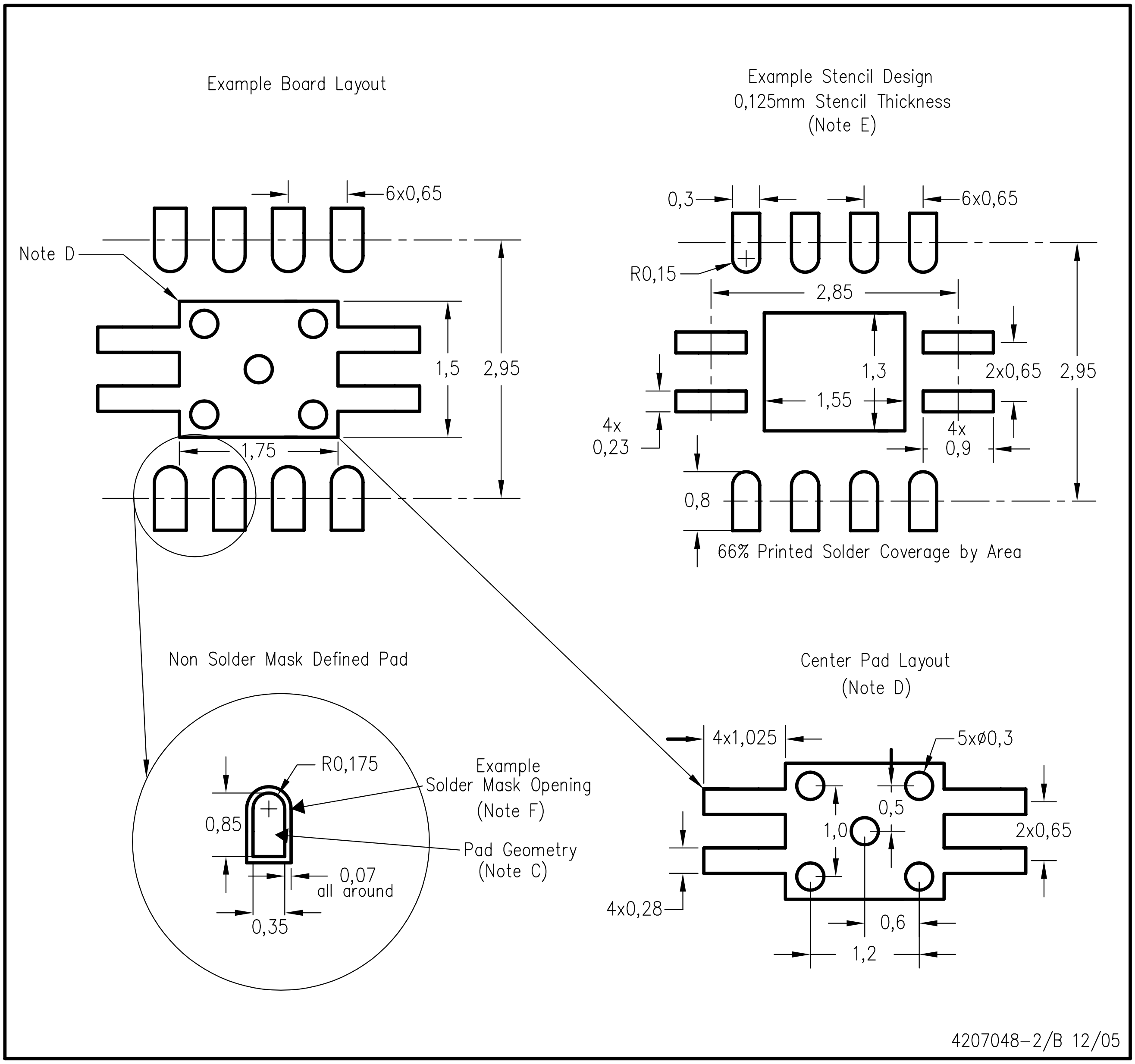
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DRB (S–PDSO–N8)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE