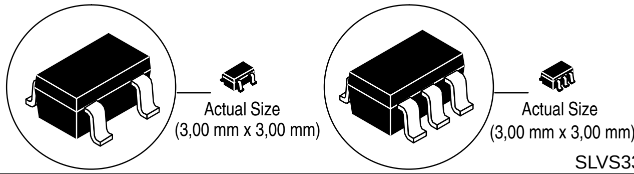


ULTRALOW-NOISE, HIGH PSRR, FAST RF 100-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **100-mA Low-Dropout Regulator With EN**
- **Available in 2.5-V, 2.8-V, 3-V, and Adj.**
- **High PSRR (75 dB at 10 kHz)**
- **Ultralow Noise (27 µV)**
- **Fast Start-Up Time (50 µs)**
- **Stable With Any 1-µF Ceramic Capacitor**
- **Excellent Load/Line Transient**
- **Very Low Dropout Voltage (55 mV at Full Load, TPS79230)**
- **5-Pin SOT23 (DBV) Package**
- **TPS791xx Provides $\overline{\text{EN}}$ Options**

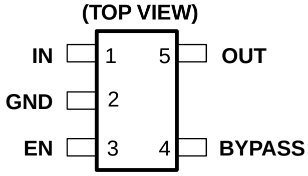
APPLICATIONS

- **Cellular and Cordless Telephones**
- **VCOs**
- **RF**
- **Bluetooth™, Wireless LAN**
- **Handheld Organizers, PDA**

DESCRIPTION

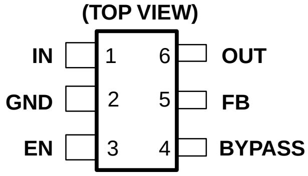
The TPS792xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline, SOT23, package. Each device in the family is stable, with a small 1-µF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 55 mV at 100 mA, TPS79230). Each device achieves fast start-up times (approximately 50 µs with a 0.001 µF bypass capacitor) while consuming very low quiescent current (170 µA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 µA. The TPS79228 exhibits approximately 27 μV_{RMS} of output voltage noise with a 0.1 µF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.

DBV PACKAGE (TOP VIEW)



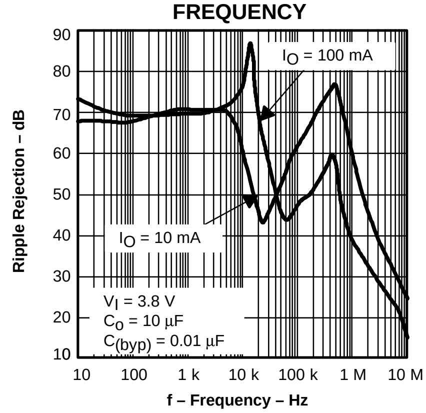
Fixed Option

DBV PACKAGE (TOP VIEW)

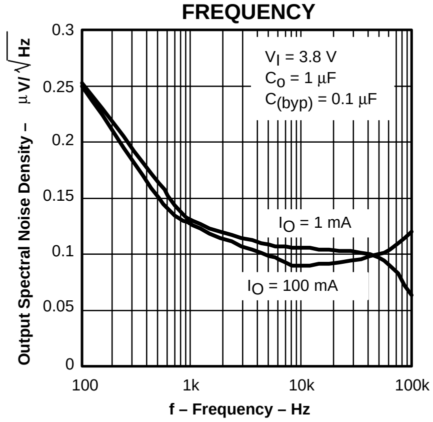


Adjustable Option

TPS79228 RIPPLE REJECTION vs FREQUENCY



TPS79228 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	VOLTAGE	PACKAGE	PART NUMBER		SYMBOL
–40°C to 125°C	1.2 to 5.5 V	SOT23 (DBV)	TPS79201DBVT(1)	TPS79201DBVR(2)	PEVI
	2.5 V		TPS79225DBVT(1)	TPS79225DBVR(2)	PEXI
	2.8 V		TPS79228DBVT(1)	TPS79228DBVR(2)	PEWI
	3 V		TPS79230DBVT(1)	TPS79230DBVR(2)	PEYI

(1) The DBVT indicates tape and reel of 250 parts.
(2) The DBVR indicates tape and reel of 3000 parts.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	TPS79201,TPS79225 TPS79228,TPS79230
Input voltage range (2)	–0.3 V to 6 V
Voltage range at EN	–0.3 V to V_I + 0.3 V
Voltage on OUT	–0.3 V to 6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	–40°C to 150°C
Operating ambient temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATING

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K(1)	DBV	63.75°C/W	256°C/W	3.906 mW/°C	391 mW	215 mW	156 mW
High K(2)	DBV	63.75°C/W	178.3°C/W	5.609 mW/°C	561 mW	308 mW	224 mW

(1) The JEDEC low K (1s) board design used to derive this data was a 3-inch x 3-inch, two layer board with 2 ounce copper traces on top of the board.
(2) The JEDEC high K (2s2p) board design used to derive this data was a 3-inch x 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I (1)	2.7		5.5	V
Continuous output current, I_O (2)	0		100	mA
Operating junction temperature, T_J	–40		125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:

$$V_I(min) = V_O(max) + V_{DO}\ (max\ load)$$

(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, (T_J = –40 to 125°C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, EN = V_I, C_o = 10 μF, $C_{(byp)}$ = 0.01 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	TPS79201	T_J = 25°C,	1.22 V ≤ V_O ≤ 5.2		V_O		V
		0 μA < I_O < 100 mA,	1.22 V ≤ V_O ≤ 5.2 V (1)	0.98 V_O		1.02 V_O	
	TPS79225	T_J = 25°C			2.5		
		0 μA < I_O < 100 mA,	3.5 V < V_I < 5.5 V	2.45		2.55	
	TPS79228	T_J = 25°C			2.8		
		0 μA < I_O < 100 mA,	3.8 V < V_I < 5.5 V	2.744		2.856	
	TPS79230	T_J = 25°C			3		
		0 μA < I_O < 100 mA,	4 V < V_I < 5.5 V	2.94		3.06	
Quiescent current (GND current)		0 μA < I_O < 100 mA,	T_J = 25°C		170		μA
		0 μA < I_O < 100 mA				250	
Load regulation		0 μA < I_O < 100 mA,	T_J = 25°C		5		mV
Output voltage line regulation ($\Delta V_O/V_O$)(2)		V_O + 1 V < V_I ≤ 5.5 V,	T_J = 25°C		0.05		%/V
		V_O + 1 V < V_I ≤ 5.5 V,				0.12	
Output noise voltage (TPS79228)		BW = 100 Hz to 100 kHz, I_O = 100 mA, T_J = 25°C	$C_{(byp)}$ = 0.001 μF		50		μV_{RMS}
			$C_{(byp)}$ = 0.0047 μF		33		
			$C_{(byp)}$ = 0.01 μF		31		
			$C_{(byp)}$ = 0.1 μF		27		
Time, start-up (TPS79228)		R_L = 28 Ω, C_o = 1 μF, T_J = 25°C	$C_{(byp)}$ = 0.001 μF		50		μs
			$C_{(byp)}$ = 0.0047 μF		70		
			$C_{(byp)}$ = 0.01 μF		90		
Output current limit		V_O = 0 V (1)		285		600	mA
UVLO threshold		V_{CC} rising		2.25		2.65	V
UVLO hysteresis		T_J = 25°C	V_{CC} rising		100		mV
Standby current		EN = 0 V,	2.7 V < V_I < 5.5 V		0.7	1	μA
High level enable input voltage		2.7 V < V_I < 5.5 V		2			V
Low level enable input voltage		2.7 V < V_I < 5.5 V				0.7	V
Input current (EN)		EN = 0 V		–1		1	μA
Power supply ripple rejection	TPS79228	f = 100 Hz, T_J = 25°C,	I_O = 10 mA		70		dB
		f = 100 Hz, T_J = 25°C,	I_O = 100 mA		72		
		f = 10 kHz, T_J = 25°C,	I_O = 100 mA		75		
		f = 100 kHz, T_J = 25°C,	I_O = 100 mA		47		
Dropout voltag(3)	TPS79228	I_O = 100 mA,	T_J = 25°C		60		mV
		I_O = 100 mA				110	
	TPS79230	I_O = 100 mA,	T_J = 25°C		55		
		I_O = 100 mA				100	

(1) The minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. The maximum output current is 100 mA.

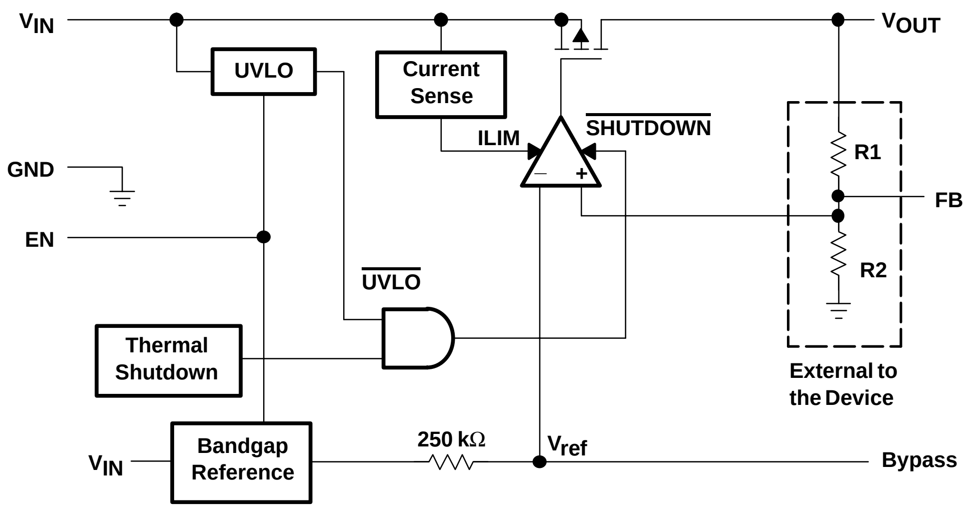
(2) If V_O ≤ 2.5 V then V_{Imin} = 2.7 V, V_{Imax} = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

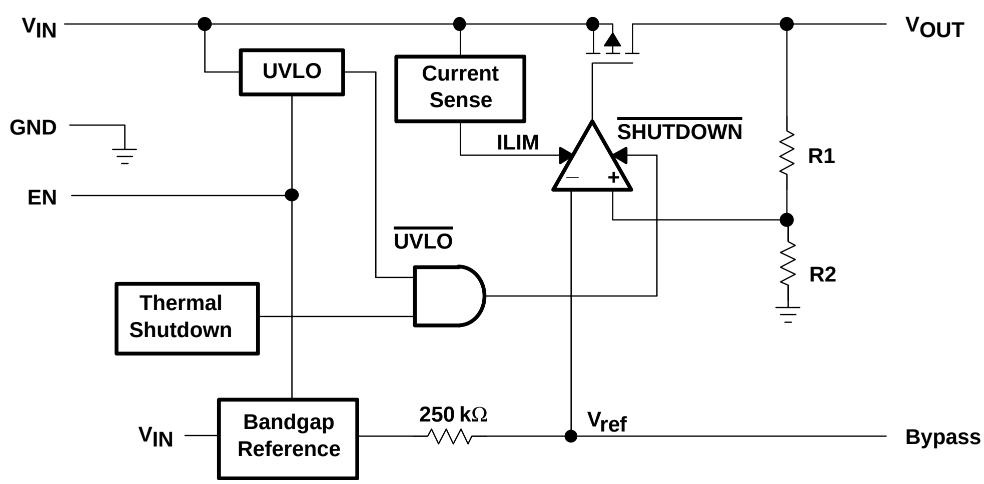
If V_O ≥ 2.5 V then V_{Imin} = V_O + 1 V, V_{Imax} = 5.5 V:

(3) IN voltage equals V_O(typ) – 100 mV; The TPS79225 dropout voltage is limited by the input voltage range limitations.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	ADJ	FIXED		
BYPASS	4	4		An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
EN	3	3	I	The EN terminal is an input which enables or shuts down the device. When EN goes to a logic high, the device will be enabled. When the device goes to a logic low, the device will be in shutdown mode.
FB	5	N/A	I	This terminal is the feedback input voltage for the adjustable device.
GND	2	2		Regulator ground
IN	1	1	I	The IN terminal is the input to the device.
OUT	6	5	O	The OUT terminal is the regulated output of the device.

TYPICAL CHARACTERISTICS

TPS79228
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

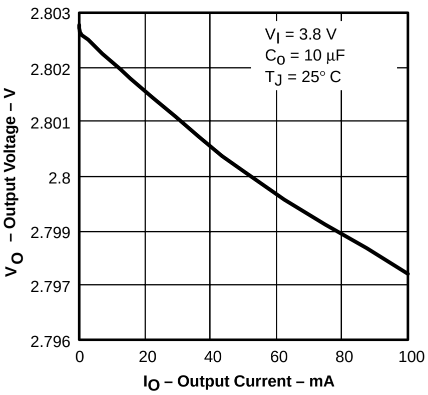


Figure 1

TPS79228
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

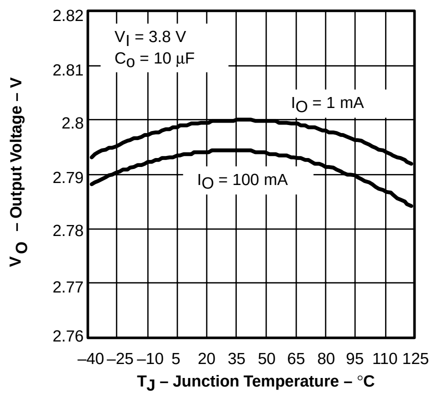


Figure 2

TPS79228
GROUND CURRENT
vs
JUNCTION TEMPERATURE

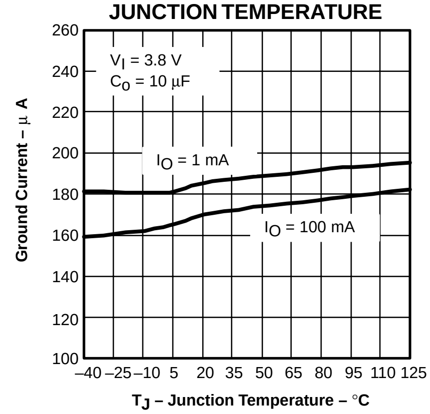


Figure 3

TPS79228
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

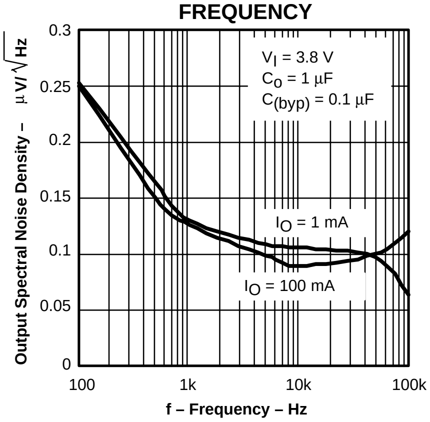


Figure 4

TPS79228
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

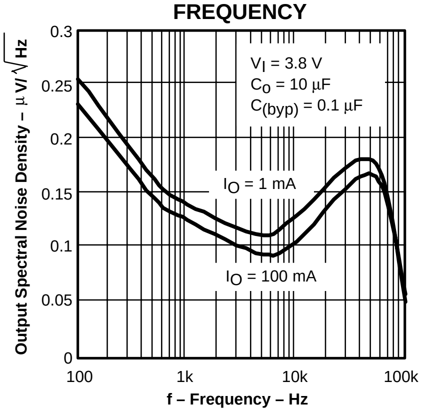


Figure 5

TPS79228
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY

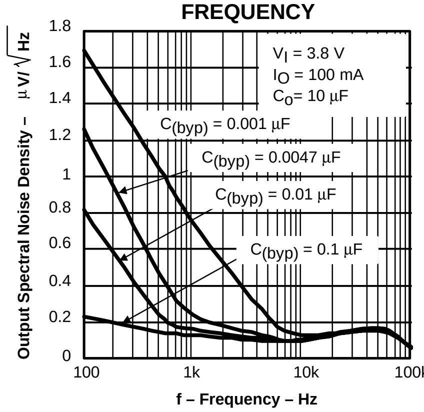


Figure 6

TPS79228
ROOT MEAN SQUARED OUTPUT NOISE
vs
BYPASS CAPACITANCE

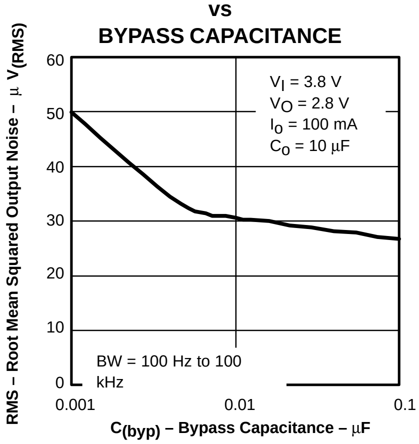


Figure 7

TPS79228
OUTPUT IMPEDANCE
vs
FREQUENCY

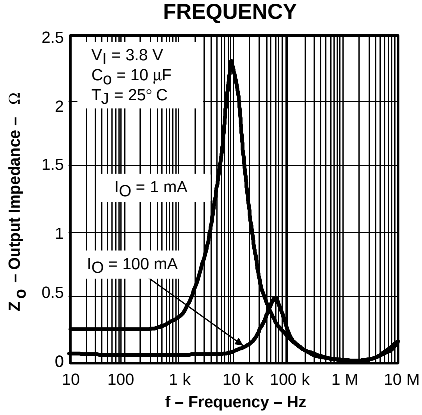


Figure 8

TPS79228
DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

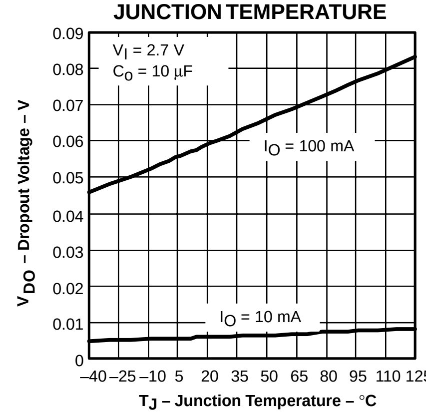


Figure 9

TYPICAL CHARACTERISTICS

TPS79228
DROPOUT VOLTAGE
vs
OUTPUT CURRENT

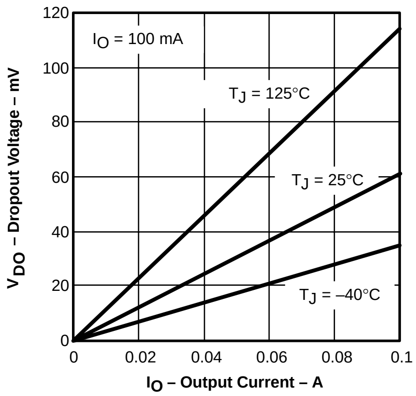


Figure 10

TPS79201
DROPOUT VOLTAGE
vs
INPUT VOLTAGE

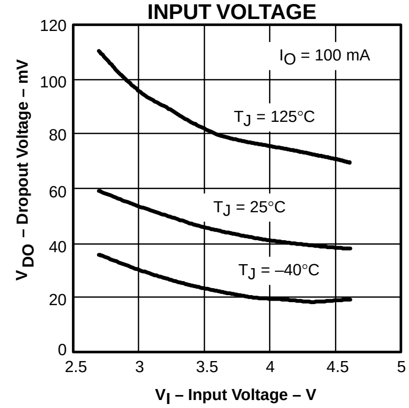


Figure 11

MINIMUM REQUIRED INPUT VOLTAGE
vs
OUTPUT VOLTAGE

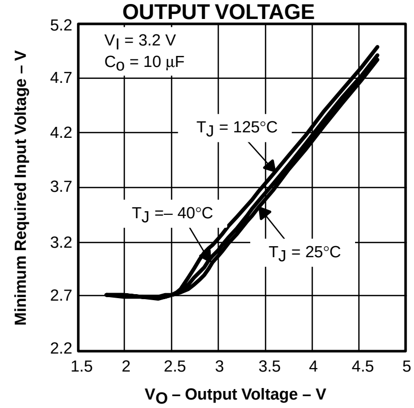


Figure 12

TPS79228
RIPPLE REJECTION
vs
FREQUENCY

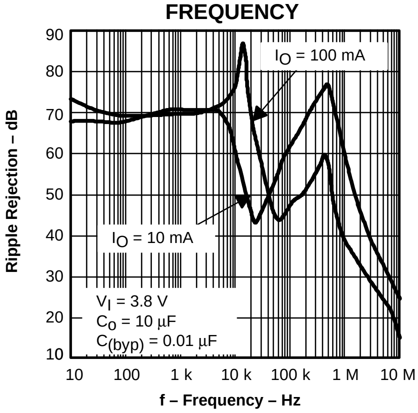


Figure 13

TPS79228
RIPPLE REJECTION
vs
FREQUENCY

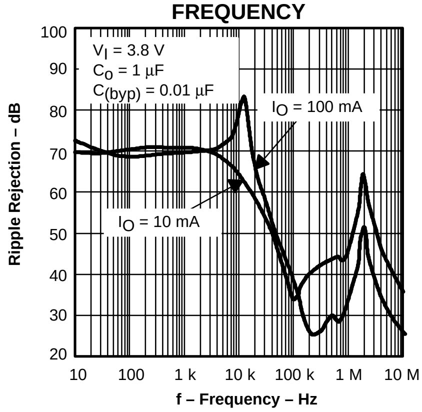


Figure 14

TPS79228
RIPPLE REJECTION
vs
FREQUENCY

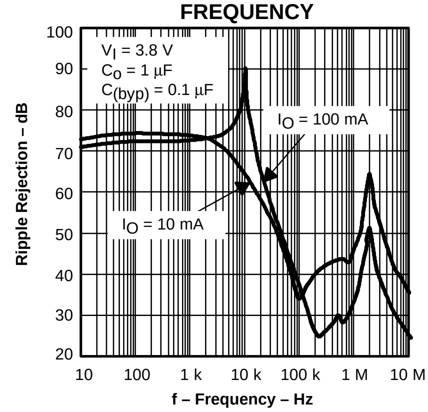


Figure 15

TPS79228
OUTPUT VOLTAGE, ENABLE VOLTAGE
vs
TIME (START-UP)

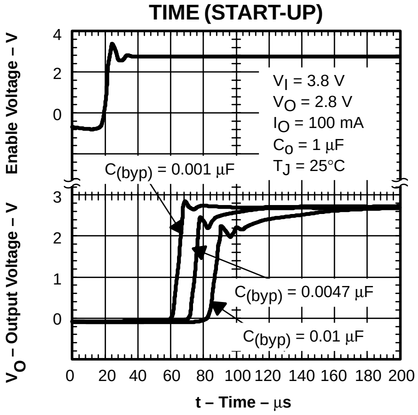


Figure 16

TPS79228
LINE TRANSIENT RESPONSE

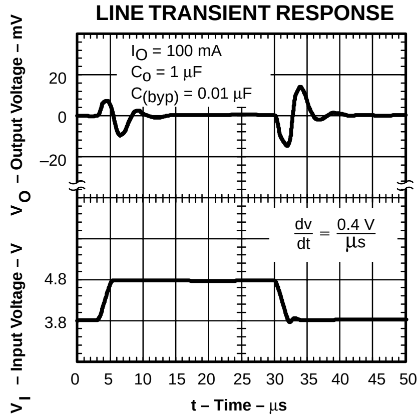


Figure 17

TPS79228
LOAD TRANSIENT RESPONSE

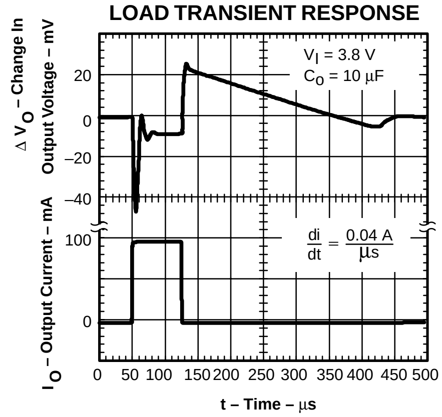


Figure 18

TYPICAL CHARACTERISTICS

TPS79228
TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

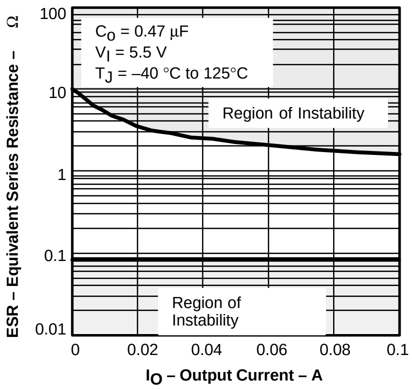


Figure 19

TPS79228
TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

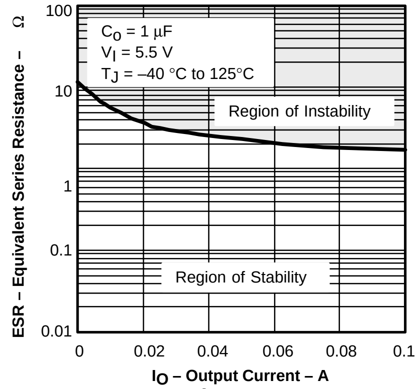


Figure 20

TPS79228
TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

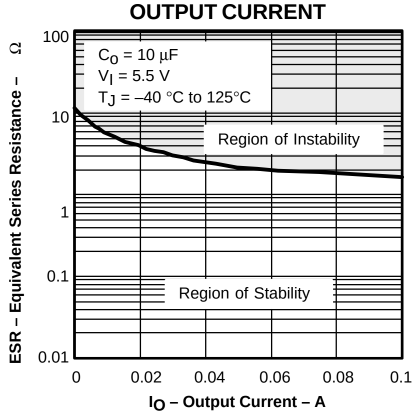


Figure 21

APPLICATION INFORMATION

The TPS792xx family of low-dropout (LDO) regulators have been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 µA typically), and enable-input to reduce supply currents to less than 1 µA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

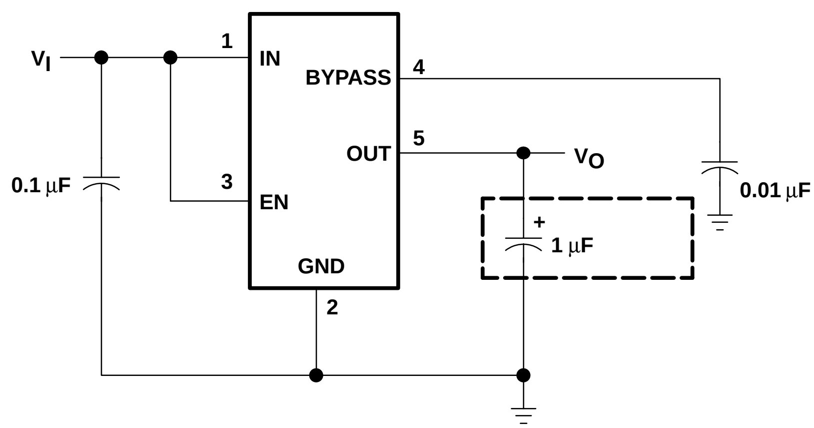


Figure 22. Typical Application Circuit

EXTERNAL CAPACITOR REQUIREMENTS

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS792xx, required for stability and to improve transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS792xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 µF. Any 1 µF or larger ceramic capacitor is suitable. The device is also stable with a 0.47 µF ceramic capacitor with at least 75 mΩ of ESR.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS792xx has a BYPASS pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79228 exhibits only 31 μV_{RMS} of output voltage noise using a 0.1-µF ceramic bypass capacitor and a 1-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250-kΩ resistor and external capacitor.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \qquad (1)$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \qquad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

PROGRAMMING THE TPS79201 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79201 adjustable regulator is programmed using an external resistor divider as shown in Figure 23. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \qquad (3)$$

Where:

V_{ref} = 1.2246 V typ (the internal reference voltage)

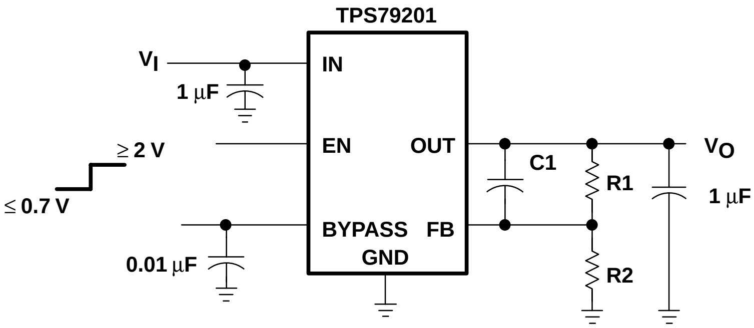
Resistors R1 and R2 should be chosen for approximately 50-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 µA, C1 = 15 pF for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \qquad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \text{ x } 10^{-7}) \text{ x } (R1 + R2)}{(R1 \text{ x } R2)} \qquad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 2.2 µF instead of 1 µF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	33.4 kΩ	30.1 kΩ	22 pF
3.3 V	53.6 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

Figure 23. TPS79201 Adjustable LDO Regulator Programming

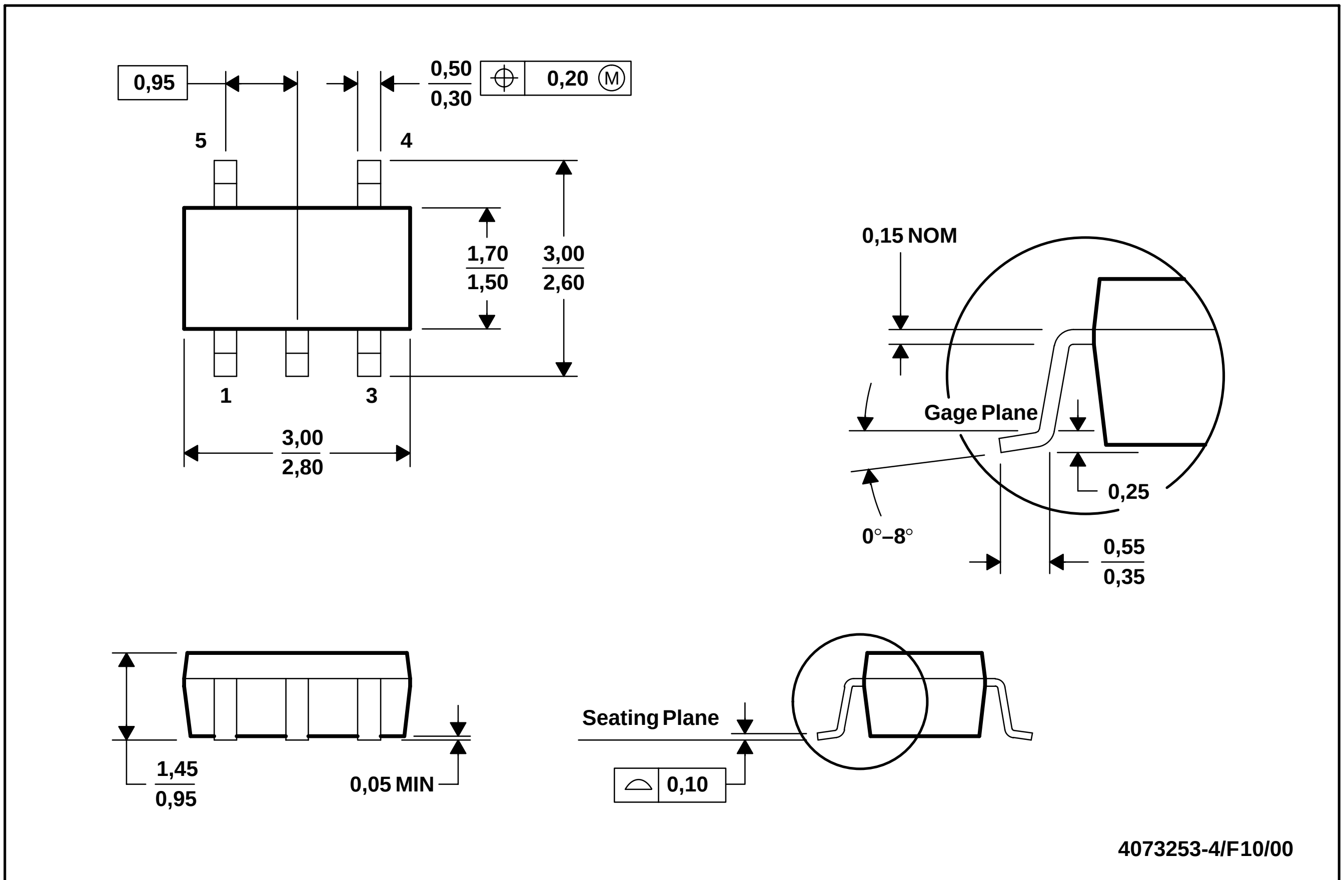
REGULATOR PROTECTION

The TPS792xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS792xx features internal current limiting and thermal protection. During normal operation, the TPS792xx limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

MECHANICAL DATA

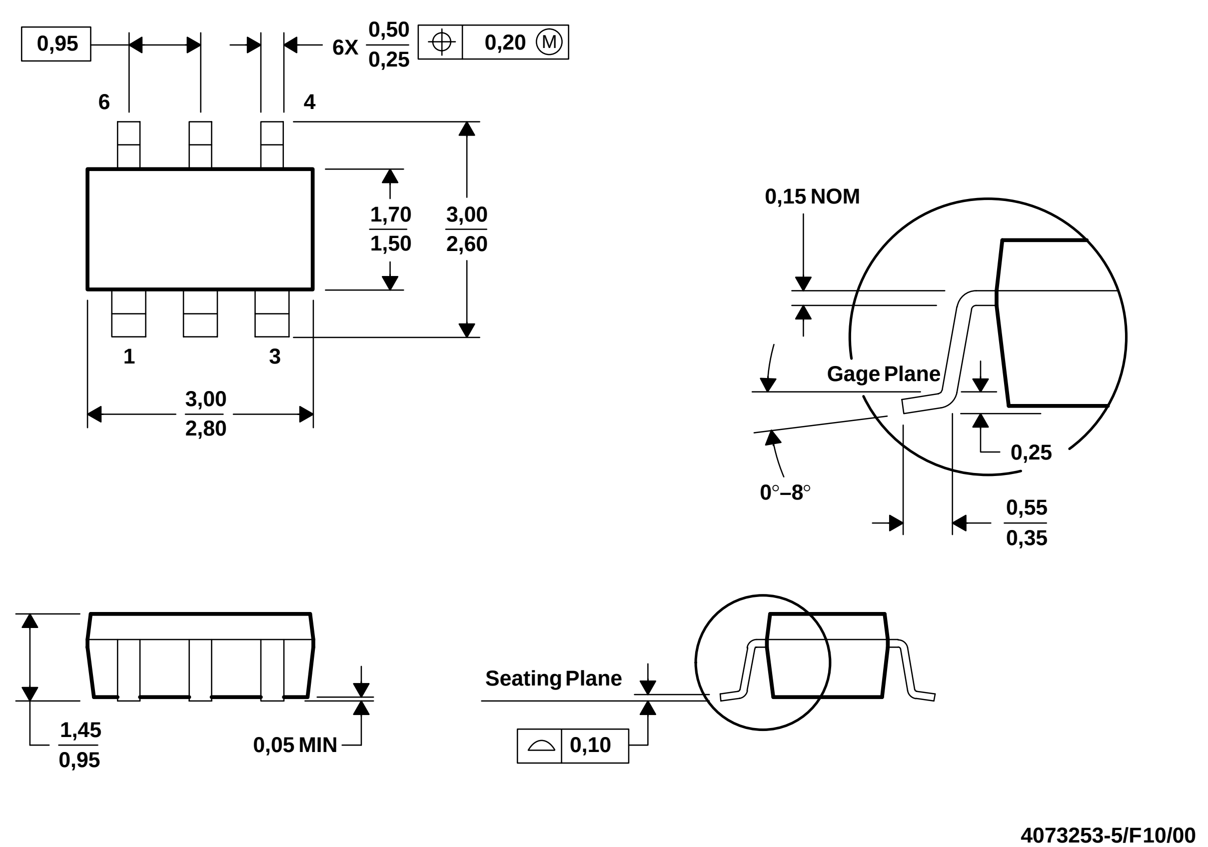
DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

MECHANICAL DATA

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 are wider than leads 4, 5, 6 for package orientation.
E. Pin 1 is located below the first letter of the top side symbolization.

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
TPS79201DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79201DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79201DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79225DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79225DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79225DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79225DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79228DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79228DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79228DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79228DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79230DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79230DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79230DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79230DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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