



## ULTRALOW-NOISE, HIGH-PSRR, FAST, RF, 250-mA LOW-DROPOUT LINEAR REGULATORS

### FEATURES

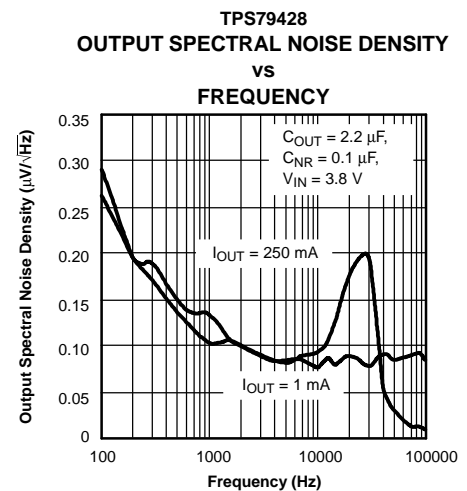
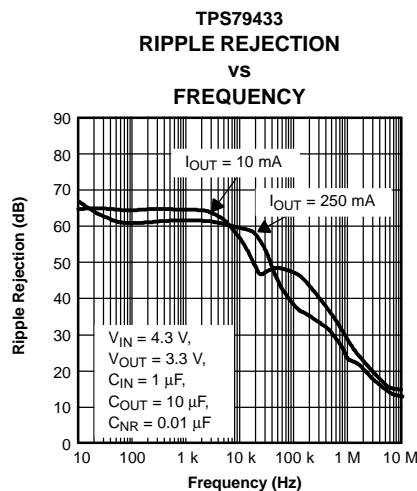
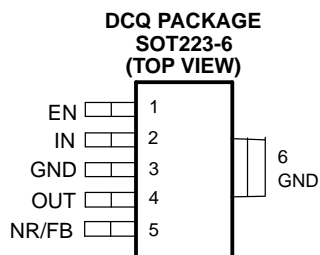
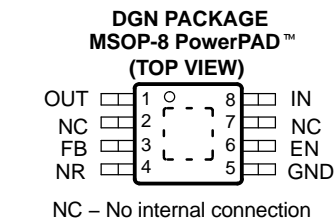
- 250-mA Low-Dropout Regulator With Enable
- Available in Fixed and Adjustable (1.2 V to 5.5 V) Versions
- High PSRR (60 dB at 10 kHz)
- Ultralow Noise (32  $\mu$ Vrms, TPS79428)
- Fast Start-Up Time (50  $\mu$ s)
- Stable With a 2.2- $\mu$ F Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (155 mV at Full Load)
- Available in MSOP-8 and SOT223-6 Packages

### APPLICATIONS

- RF: VCOs, Receivers, ADCs
- Audio
- Bluetooth™, Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

### DESCRIPTION

The TPS794xx family of low-dropout (LDO) linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in small outline, MSOP-8 PowerPAD™ and SOT223-6 packages. Each device in the family is stable with a small 2.2- $\mu$ F ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (for example, 155 mV at 250 mA). Each device achieves fast start-up times (approximately 50  $\mu$ s with a 0.001- $\mu$ F bypass capacitor) while consuming low quiescent current (170  $\mu$ A typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1  $\mu$ A. The TPS79428 exhibits approximately 32  $\mu$ V<sub>RMS</sub> of output voltage noise at 2.8 V output with a 0.1- $\mu$ F bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.




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 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub> <sup>(2)</sup>
TPS794xxyyz	XX is nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). YYY is package designator. Z is package quantity.

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Output voltages from 1.3 V to 5.0 V in 100 mV increments are available; minimum order quantities may apply. Contact factory for details and availability.

### ABSOLUTE MAXIMUM RATINGS

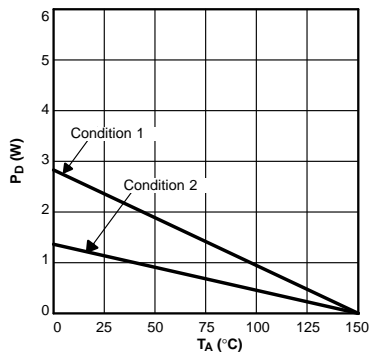
over operating temperature range unless otherwise noted<sup>(1)</sup>

	VALUE
V <sub>IN</sub> range	–0.3 V to 6 V
V <sub>EN</sub> range	–0.3 V to V <sub>IN</sub> + 0.3 V
V <sub>OUT</sub> range	–0.3 V to 6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Ratings Table
Junction temperature range, T <sub>J</sub>	–40°C to +150°C
Storage temperature range, T <sub>stg</sub>	–65°C to +150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### PACKAGE DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	R <sub>θJC</sub> (°C/W)	R <sub>θJA</sub> (°C/W)	T <sub>A</sub> ≤ 25°C POWER RATING	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
DGN	0	8.47	55.09	2.27 W	1.45 W	1.18 W
	150	8.21	49.97	2.50 W	1.60 W	1.30 W
	250	8.20	48.10	2.60 W	1.66 W	1.35 W



CONDITIONS	PACKAGE	PCB AREA	θ <sub>JA</sub>
1	SOT223	4in <sup>2</sup> Top Side Only	53°C/W
2	SOT223	0.5in <sup>2</sup> Top Side Only	110°C/W

Figure 1. SOT223 Power Dissipation

## ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range ( $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ),  $V_{EN} = V_{IN}$ ,  $V_{IN} = V_{OUT(nom)} + 1\text{ V}^{(1)}$ ,  $I_{OUT} = 1\text{ mA}$ ,  $C_{OUT} = 10\mu\text{F}$ ,  $C_{NR} = 0.01\mu\text{F}$ , unless otherwise noted. Typical values are at  $25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input voltage, $V_{IN}^{(1)}$			2.7		5.5	V	
Continuous output current, $I_{OUT}$			0		250	mA	
Output voltage	Output voltage range	TPS79401	1.225		$5.5 - V_{DO}$	V	
	Accuracy	TPS79401 <sup>(2)</sup>	$0\mu\text{A} \leq I_{OUT} \leq 250\text{ mA}$ , $V_{OUT} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}^{(1)}$	$0.97(V_{OUT})$	$V_{OUT}$	$1.03(V_{OUT})$	V
		Fixed $V_{OUT}$	$0\mu\text{A} \leq I_{OUT} \leq 250\text{ mA}$ , $V_{OUT} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}^{(1)}$	-3.0		+3.0	%
Output voltage line regulation ( $\Delta V_{OUT}\%/\Delta V_{IN}$ ) <sup>(1)</sup>		$V_{OUT} + 1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.05	0.12	%/V	
Load regulation ( $\Delta V_{OUT}\%/\Delta I_{OUT}$ )		$0\mu\text{A} \leq I_{OUT} \leq 250\text{ mA}$		10		mV	
Dropout voltage <sup>(3)</sup> $V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$	TPS79428	$I_{OUT} = 250\text{ mA}$		155	210	mV	
	TPS79430	$I_{OUT} = 250\text{ mA}$		155	210		
	TPS79433	$I_{OUT} = 250\text{ mA}$		145	200		
Output current limit		$V_{OUT} = 0\text{ V}$		925		mA	
Ground pin current		$0\mu\text{A} \leq I_{OUT} \leq 250\text{ mA}$		170	220	$\mu\text{A}$	
Shutdown current <sup>(4)</sup>		$V_{EN} = 0\text{ V}$ , $2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.07	1	$\mu\text{A}$	
FB pin current		$V_{FB} = 1.225\text{ V}$			1	$\mu\text{A}$	
Power-supply ripple rejection	TPS79428	$f = 100\text{ Hz}$ , $I_{OUT} = 250\text{ mA}$		65		dB	
		$f = 10\text{ kHz}$ , $I_{OUT} = 250\text{ mA}$		60			
		$f = 100\text{ kHz}$ , $I_{OUT} = 250\text{ mA}$		40			
Output noise voltage	TPS79428	$BW = 100\text{ Hz to }100\text{ kHz}$ , $I_{OUT} = 250\text{ mA}$	$C_{NR} = 0.001\mu\text{F}$		55	$\mu\text{V}_{RMS}$	
			$C_{NR} = 0.0047\mu\text{F}$		36		
			$C_{NR} = 0.01\mu\text{F}$		33		
			$C_{NR} = 0.1\mu\text{F}$		32		
Time, start-up	TPS79428	$R_L = 14\Omega$ , $C_{OUT} = 1\mu\text{F}$	$C_{NR} = 0.001\mu\text{F}$		50	$\mu\text{s}$	
			$C_{NR} = 0.0047\mu\text{F}$		70		
			$C_{NR} = 0.01\mu\text{F}$		100		
High-level enable input voltage		$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	1.7		$V_{IN}$	V	
Low-level enable input voltage		$2.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$	0		0.7	V	
EN pin current		$V_{EN} = 0$	1		1	$\mu\text{A}$	
UVLO threshold		$V_{CC}$ rising	2.25		2.65	V	
UVLO hysteresis				100		mV	

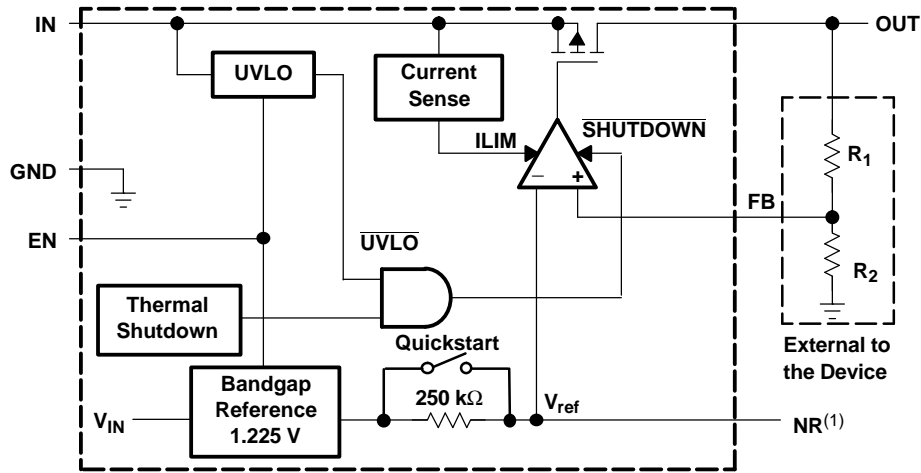
(1) Minimum  $V_{IN}$  is 2.7 V or  $V_{OUT} + V_{DO}$ , whichever is greater.

(2) Tolerance of external resistors not included in this specification.

(3) Dropout is not measured for the TPS79418 and TPS79425 since minimum  $V_{IN} = 2.7\text{ V}$ .

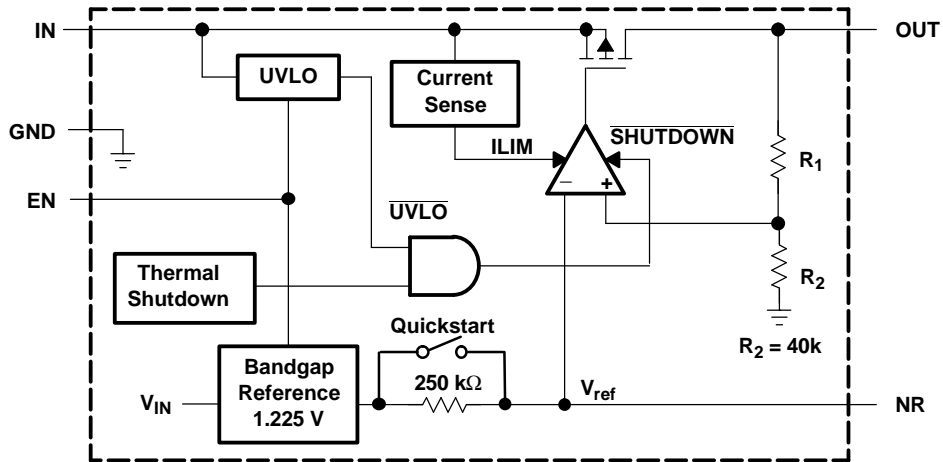
(4) For adjustable versions, this applies only after  $V_{IN}$  is applied; then  $V_{EN}$  transitions high to low.

**FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION**



(1) Not Available on DCQ (SOT223) options.

**FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION**



**Terminal Functions**

TERMINAL			DESCRIPTION
NAME	DGN (MSOP)	DCQ (SOT223)	
NR	4	5	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, which improves power-supply rejection and reduces output noise.
EN	6	1	The EN terminal is an input that enables or shuts down the device. When EN goes to a logic high, the device will be enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	3	5	Feedback input voltage for the adjustable device.
GND	5, PAD	3, 6	Regulator ground
IN	8	2	Unregulated input to the device.
NC	2, 7		No internal connection.
OUT	1	4	Regulator output

TYPICAL CHARACTERISTICS

TPS79433  
OUTPUT VOLTAGE  
vs OUTPUT CURRENT

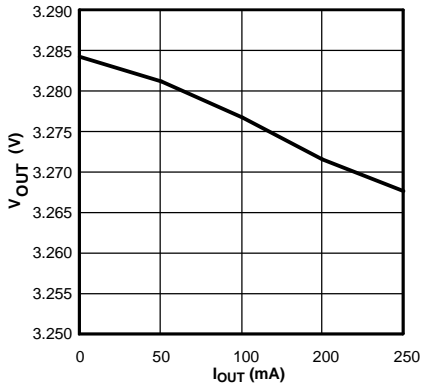


Figure 2.

TPS79428  
OUTPUT VOLTAGE  
vs JUNCTION TEMPERATURE

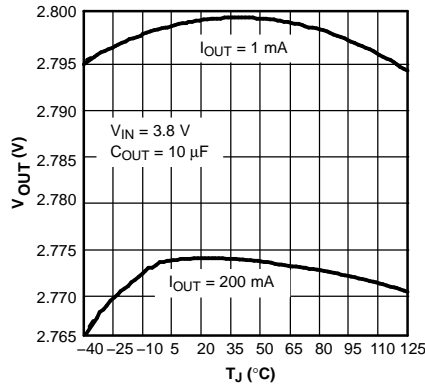


Figure 3.

TPS79428  
GROUND CURRENT  
vs JUNCTION TEMPERATURE

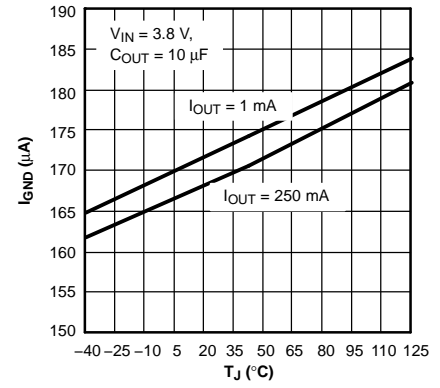


Figure 4.

TPS79428  
OUTPUT SPECTRAL  
NOISE DENSITY  
vs FREQUENCY

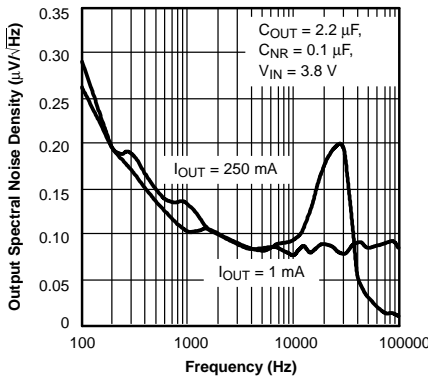


Figure 5.

TPS79428  
OUTPUT SPECTRAL  
NOISE DENSITY  
vs FREQUENCY

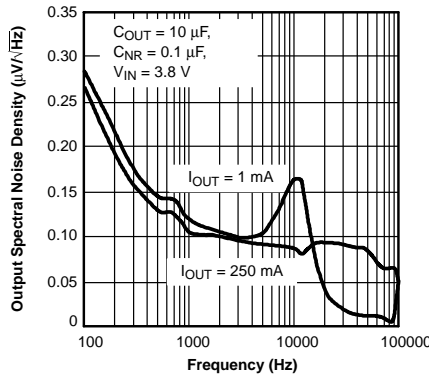


Figure 6.

TPS79428  
OUTPUT SPECTRAL  
NOISE DENSITY  
vs FREQUENCY

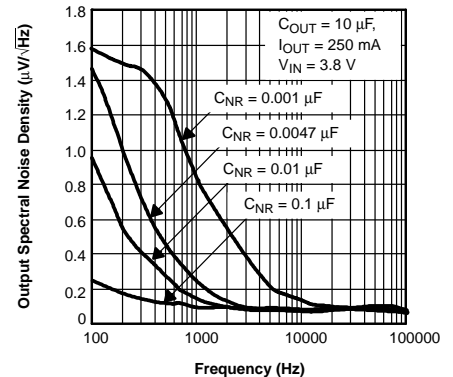


Figure 7.

TPS79428  
ROOT MEAN SQUARED  
OUTPUT NOISE vs C\_NR

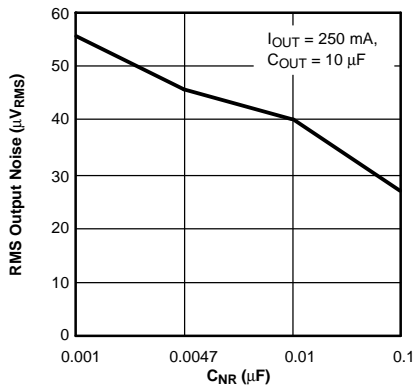


Figure 8.

TPS79433  
OUTPUT IMPEDANCE  
vs FREQUENCY

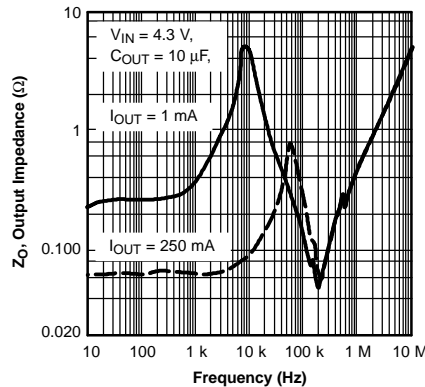


Figure 9.

TPS79428  
DROPOUT VOLTAGE  
vs JUNCTION TEMPERATURE

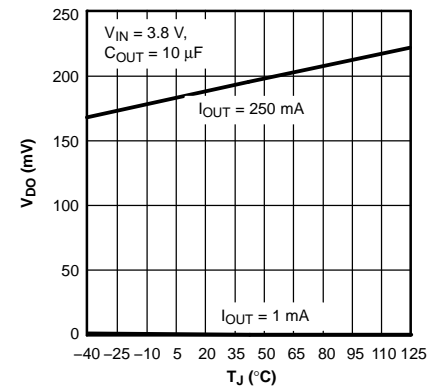


Figure 10.

TYPICAL CHARACTERISTICS (continued)

**TPS79433  
RIPPLE REJECTION  
vs FREQUENCY**

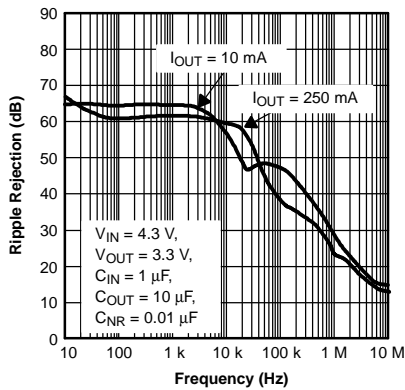


Figure 11.

**TPS79433  
RIPPLE REJECTION  
vs FREQUENCY**

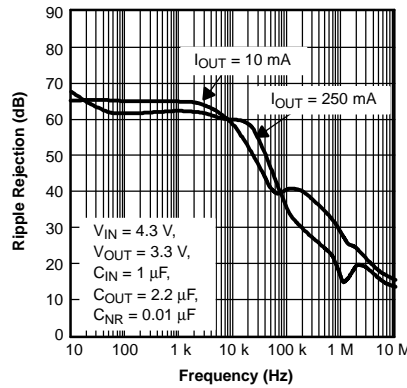


Figure 12.

**TPS79433  
RIPPLE REJECTION  
vs FREQUENCY**

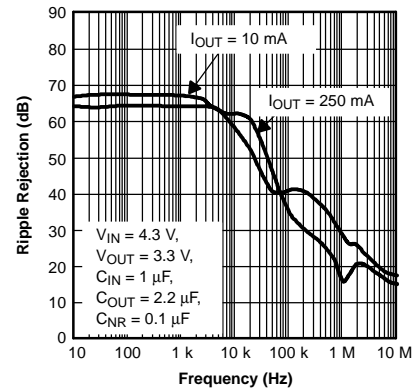


Figure 13.

**TPS79433  
OUTPUT VOLTAGE,  
ENABLE VOLTAGE  
vs TIME (START-UP)**

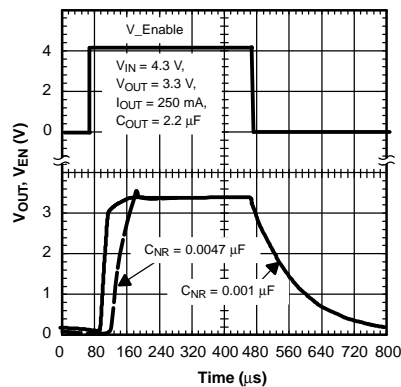


Figure 14.

**TPS79433  
LINE TRANSIENT  
RESPONSE**

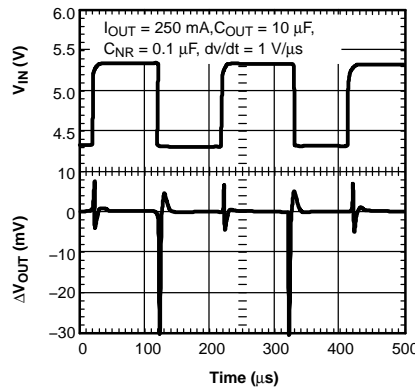


Figure 15.

**TPS79433  
LOAD TRANSIENT  
RESPONSE**

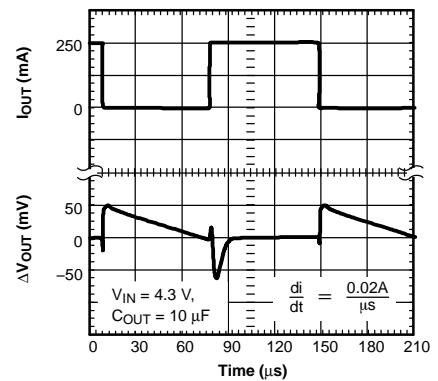


Figure 16.

**TPS79425  
POWER-UP/  
POWER-DOWN**

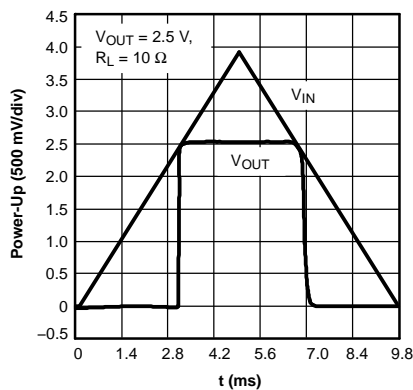


Figure 17.

**TPS79433  
DROPOUT VOLTAGE  
vs OUTPUT CURRENT**

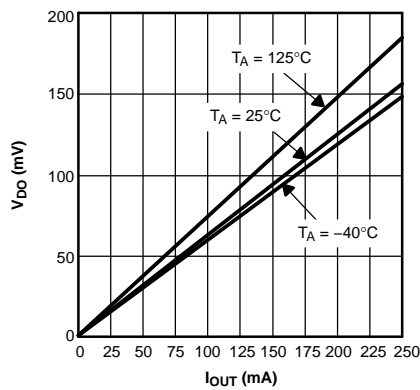


Figure 18.

**TPS79401  
DROPOUT VOLTAGE  
vs INPUT VOLTAGE**

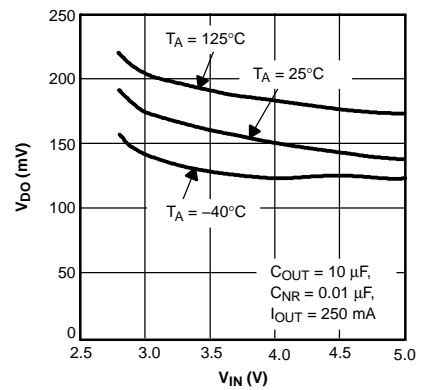


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TPS79428  
TYPICAL REGIONS OF STABILITY  
EQUIVALENT SERIES RESISTANCE  
(ESR)  
vs OUTPUT CURRENT

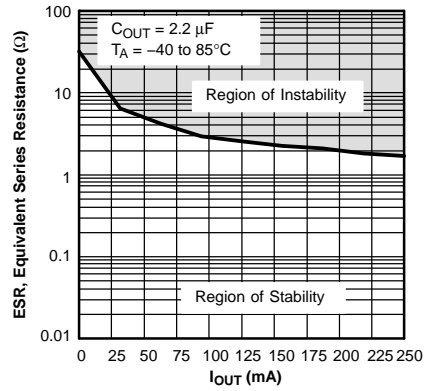


Figure 20.

TPS79428  
TYPICAL REGIONS OF STABILITY  
EQUIVALENT SERIES RESISTANCE  
(ESR)  
vs OUTPUT CURRENT

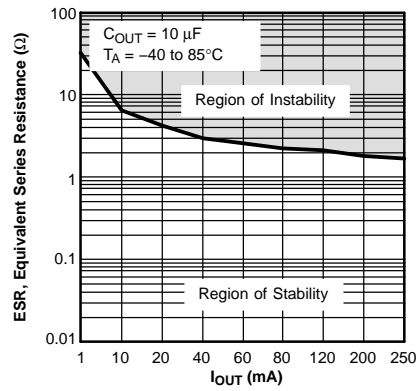
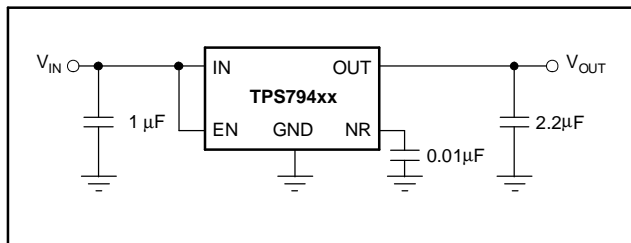


Figure 21.

## APPLICATION INFORMATION

The TPS794xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (265  $\mu\text{A}$  typically), and an enable input to reduce supply currents to less than 1  $\mu\text{A}$  when the regulator is turned off.

A typical application circuit is shown in [Figure 22](#).



**Figure 22. Typical Application Circuit**

### EXTERNAL CAPACITOR REQUIREMENTS

A 1- $\mu\text{F}$  or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS794xx, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like most low-dropout regulators, the TPS794xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1  $\mu\text{F}$ . Any 1  $\mu\text{F}$  or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS794xx has an NR pin which is connected to the voltage reference through a 250-k $\Omega$  internal resistor. The 250-k $\Omega$  internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise

and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor, thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1- $\mu\text{F}$  in order to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the [Functional Block Diagram](#).

For example, the TPS79430 exhibits only 33  $\mu\text{V}_{\text{RMS}}$  of output voltage noise using a 0.1- $\mu\text{F}$  ceramic bypass capacitor and a 10- $\mu\text{F}$  ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases because of the RC time constant at the bypass pin that is created by the internal 250-k $\Omega$  resistor and external capacitor.

### BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for  $V_{\text{IN}}$  and  $V_{\text{OUT}}$ , with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

### REGULATOR MOUNTING

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation.

Solder pad footprint recommendations for the devices are presented in Application Report [SBFA015](#), *Solder Pad Recommendations for Surface-Mount Devices*, available from the TI web site ([www.ti.com](http://www.ti.com)).



## PROGRAMMING THE TPS79401 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79401 adjustable regulator is programmed using an external resistor divider as shown in [Figure 23](#). The output voltage is calculated using [Equation 1](#):

$$V_{\text{OUT}} = V_{\text{REF}} \times \left( 1 + \frac{R_1}{R_2} \right) \quad (1)$$

where:

- $V_{\text{REF}} = 1.2246 \text{ V typ}$  (the internal reference voltage)

Resistors  $R_1$  and  $R_2$  should be chosen for approximately 40- $\mu\text{A}$  divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided, as leakage current at FB increases the output voltage error.

The recommended design procedure is to choose  $R_2 = 30.1 \text{ k}\Omega$  to set the divider current at 40  $\mu\text{A}$ ,  $C_1 = 15 \text{ pF}$  for stability, and then calculate  $R_1$  using [Equation 2](#):

$$R_1 = \left( \frac{V_{\text{OUT}}}{V_{\text{REF}}} - 1 \right) \times R_2 \quad (2)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB.

The approximate value of this capacitor can be calculated as [Equation 3](#):

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)} \quad (3)$$

The suggested value of this capacitor for several resistor ratios is shown in the table within [Figure 23](#). If this capacitor is not used (such as in a unity-gain configuration), then the minimum recommended output capacitor is 2.2  $\mu\text{F}$  instead of 1  $\mu\text{F}$ .

## REGULATOR PROTECTION

The TPS794xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS794xx features internal current limiting and thermal protection. During normal operation, the TPS794xx limits output current to approximately 2.8 A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

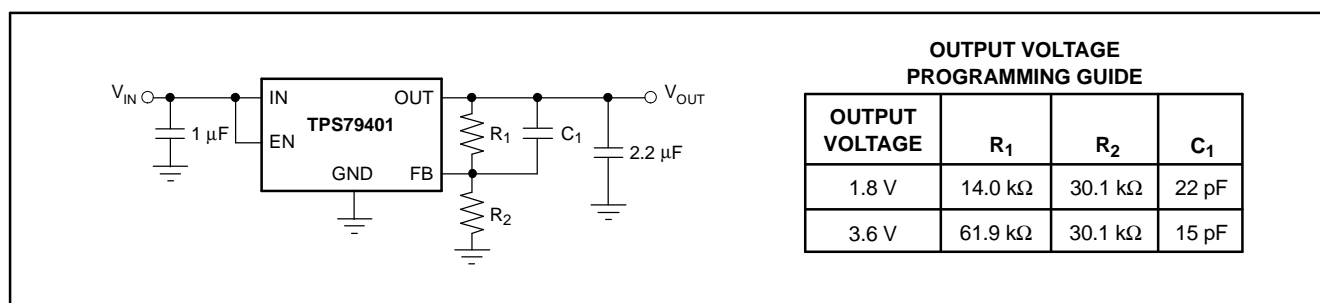


Figure 23. TPS79401 Adjustable LDO Regulator Programming

## THERMAL INFORMATION

The amount of heat that an LDO linear regulator generates is directly proportional to the amount of power it dissipates during operation. All integrated circuits have a maximum allowable junction temperature ( $T_{Jmax}$ ) above which normal operation is not assured. A system designer must design the operating environment so that the operating junction temperature ( $T_J$ ) does not exceed the maximum junction temperature ( $T_{Jmax}$ ). The two main environmental variables that a designer can use to improve thermal performance are air flow and external heatsinks. The purpose of this information is to aid the designer in determining the proper operating environment for a linear regulator that is operating at a specific power level.

In general, the maximum expected power ( $P_{Dmax}$ ) consumed by a linear regulator is computed as shown in [Equation 4](#):

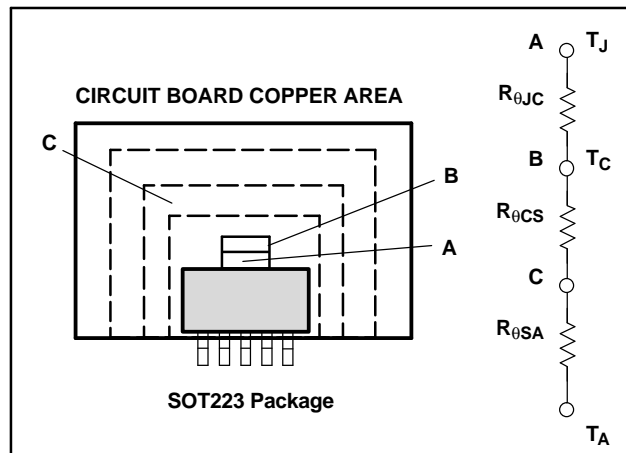
$$P_{Dmax} = (V_{IN(avg)} - V_{OUT(avg)}) \times I_{OUT(avg)} + V_{I(avg)} \times I_Q \quad (4)$$

where:

- $V_{IN(avg)}$  is the average input voltage
- $V_{OUT(avg)}$  is the average output voltage
- $I_{OUT(avg)}$  is the average output current
- $I_Q$  is the quiescent current

For most TI LDO regulators, the quiescent current is insignificant compared to the average output current; therefore, the term  $V_{IN(avg)} \times I_Q$  can be neglected. The operating junction temperature is computed by adding the ambient temperature ( $T_A$ ) and the increase in temperature due to the regulator's power dissipation. The temperature rise is computed by multiplying the maximum expected power dissipation by the sum of the thermal resistances between the junction and the case ( $R_{\theta JC}$ ), the case to heatsink ( $R_{\theta CS}$ ), and the heatsink to ambient ( $R_{\theta SA}$ ). Thermal resistances are measures of how effectively an object dissipates heat. Typically, the larger the device, the more surface area available for power dissipation and the lower the object's thermal resistance.

[Figure 24](#) illustrates these thermal resistances for a SOT223 package mounted in a JEDEC low-K board.



**Figure 24. Thermal Resistances**

[Equation 5](#) summarizes the computation:

$$T_J = T_A + P_{Dmax} \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \quad (5)$$

The  $R_{\theta JC}$  is specific to each regulator as determined by its package, lead frame, and die size provided in the regulator's data sheet. The  $R_{\theta SA}$  is a function of the type and size of heatsink. For example, *black body radiator* type heatsinks can have  $R_{\theta CS}$  values ranging from 5°C/W for very large heatsinks to 50°C/W for very small heatsinks. The  $R_{\theta CS}$  is a function of how the package is attached to the heatsink. For example, if a thermal compound is used to attach a heatsink to a SOT223 package,  $R_{\theta CS}$  of 1°C/W is reasonable.

Even if no external *black body radiator* type heatsink is attached to the package, the board on which the regulator is mounted provides some heatsinking through the pin solder connections. Some packages, like the DPAK and SOT223 packages, use a copper plane underneath the package or the circuit board ground plane for additional heatsinking to improve their thermal performance. Computer-aided thermal modeling can be used to compute very accurate approximations of an integrated circuit's thermal performance in different operating environments (for example, different types of circuit boards, different types and sizes of heatsinks, different air flows, etc.). Using these models, the three thermal resistances can be combined into one thermal resistance between junction and ambient ( $R_{\theta JA}$ ). This  $R_{\theta JA}$  is valid only for the specific operating environment used in the computer model.

Equation 5 simplifies into Equation 6:

$$T_J = T_A + P_{D,max} \times R_{\theta JA} \quad (6)$$

Rearranging Equation 6 gives Equation 7:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{D,max}} \quad (7)$$

Using Equation 6 and the computer model generated curves shown in Figure 25, a designer can quickly compute the required heatsink thermal resistance/board area for a given ambient temperature, power dissipation, and operating environment.

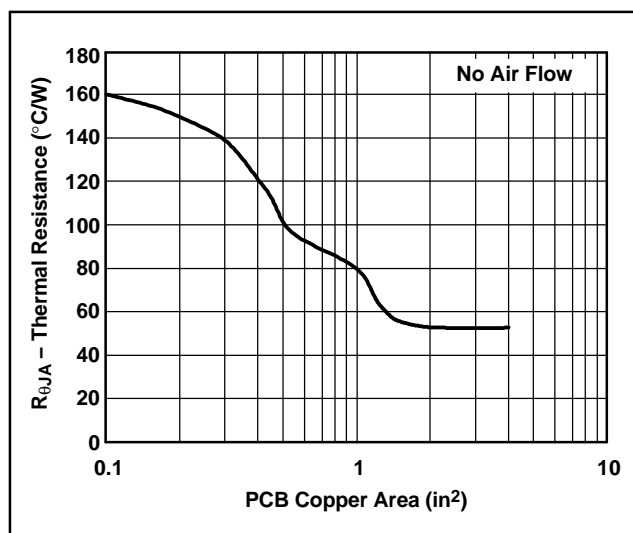


Figure 25. SOT223 Thermal Resistance vs PCB Copper Area

### SOT223 POWER DISSIPATION

The SOT223 package provides an effective means of managing power dissipation in surface-mount applications. The SOT223 package dimensions are provided in the *Mechanical Data* section at the end of the data sheet. The addition of a copper plane directly underneath the SOT223 package enhances the thermal performance of the package.

To illustrate, the TPS79425 in a SOT223 package was chosen. For this example, the average input voltage is 3.3 V, the output voltage is 2.5 V, the average output current is 1 A, the ambient temperature 55°C, no air flow is present, and the operating environment is the same as documented below. Neglecting the quiescent current, the maximum average power is Equation 8:

$$P_{D,max} = (3.3 - 2.5)V \times 1A = 800mW \quad (8)$$

Substituting  $T_{J,max}$  for  $T_J$  into Equation 4 gives Equation 9:

$$R_{\theta JA,max} = (125 - 55)^\circ C / 800mW = 87.5^\circ C/W \quad (9)$$

From Figure 25,  $R_{\theta JA}$  vs PCB Copper Area, the ground plane needs to be 0.55 in<sup>2</sup> for the part to dissipate 800 mW. The operating environment used to construct Figure 25 consisted of a board with 1 oz. copper planes. The package is soldered to a 1 oz. copper pad on the top of the board. The pad is tied through thermal vias to the 1 oz. ground plane.

From the data in Figure 25 and rearranging equation 6, the maximum power dissipation for a different ground plane area and a specific ambient temperature can be computed, as shown in Figure 26.

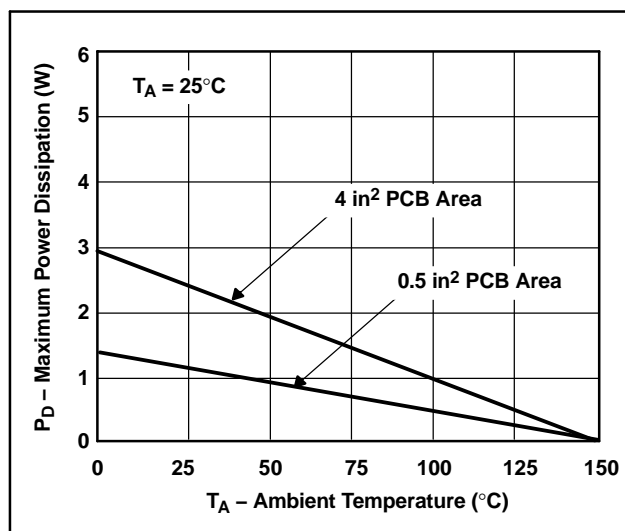


Figure 26. SOT223 Maximum Power Dissipation vs Ambient Temperature

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS79401DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79401DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79401DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79401DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79401DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79401DGNT	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79401DGNTG4	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79418DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79418DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79418DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79418DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79418DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79418DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79418DGNT	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79418DGNTG4	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79425DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79425DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79425DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79425DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79425DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79425DGNT	ACTIVE	MSOP-	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
		Power PAD				no Sb/Br)		
TPS79425DGNTG4	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79428DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79428DCQG4	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79428DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79428DCQRG4	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79428DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79428DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79428DGNT	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79428DGNTG4	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79430DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79430DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79430DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79430DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79430DGNT	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79430DGNTG4	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79433DCQ	ACTIVE	SOT-223	DCQ	6	78	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79433DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS79433DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79433DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS79433DGNT	ACTIVE	MSOP-Power	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
		PAD						
TPS79433DGNTG4	ACTIVE	MSOP-Power PAD	DGN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

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**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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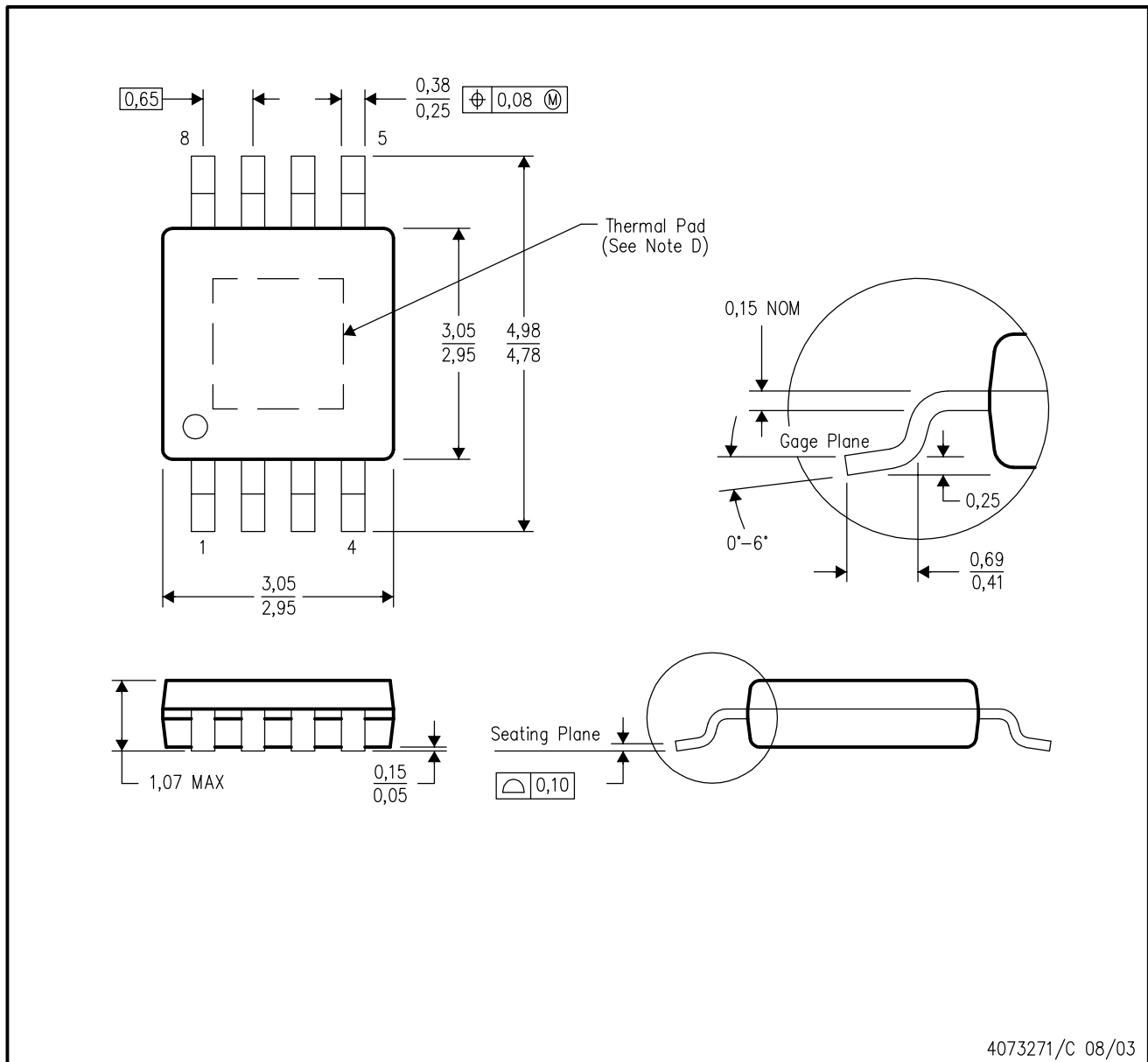
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



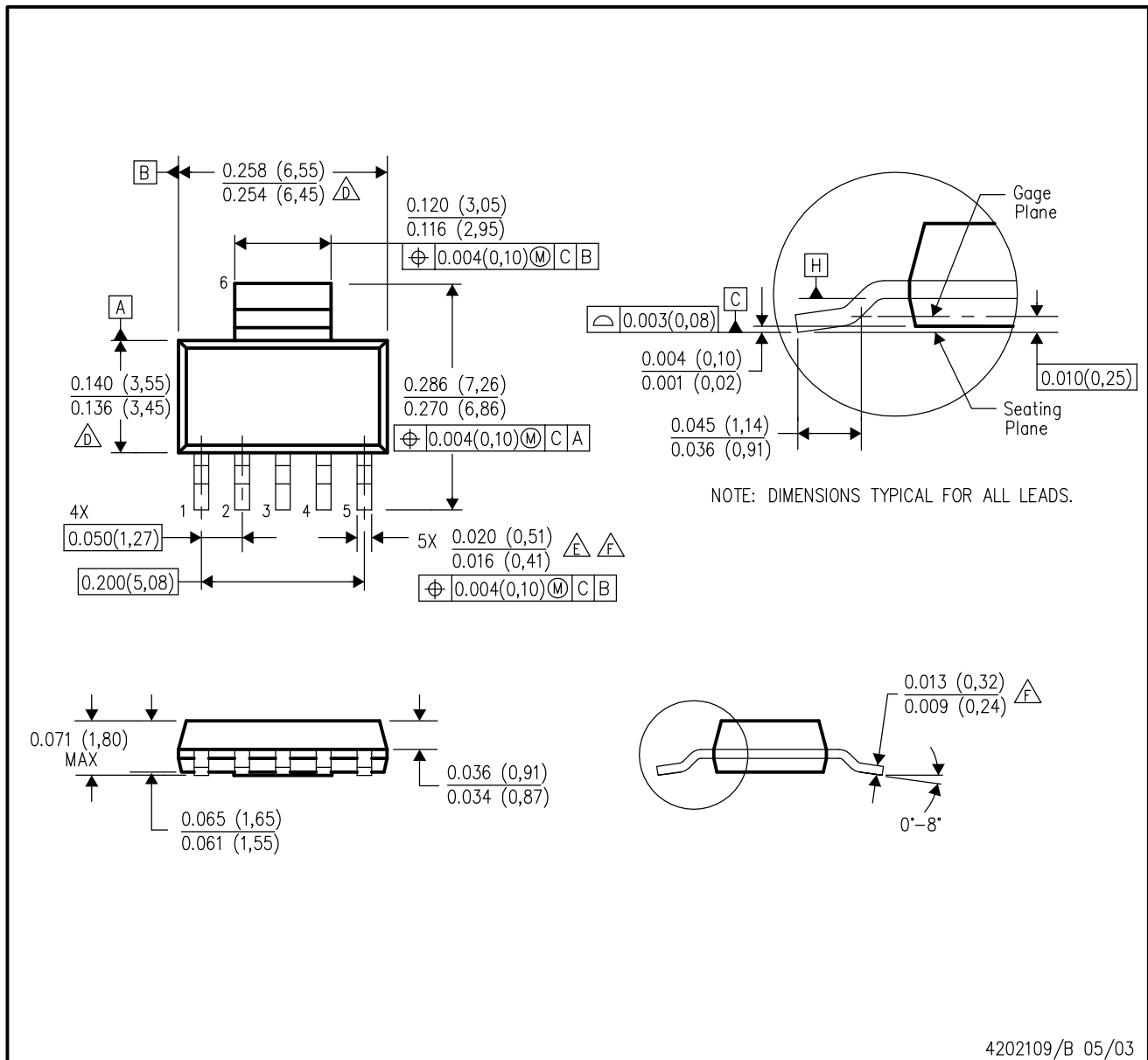
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- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Falls within JEDEC MO-187

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DCQ (R-PDSO-G6)

PLASTIC SMALL-OUTLINE



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  - B. This drawing is subject to change without notice.
  - C. Controlling dimension in inches.
  - $\triangle D$  Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
  - $\triangle E$  Lead width dimension does not include dambar protrusion.
  - $\triangle F$  Lead width and thickness dimensions apply to solder plated leads.
  - G. Interlead flash allow 0.008 inch max.
  - H. Gate burr/protrusion max. 0.006 inch.
  - I. Datums A and B are to be determined at Datum H.
  - J. Package dimensions per JEDEC outline drawing TO-261, issue B, dated Feb. 1999. This variation is not yet included.



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