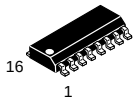
# MC145074

# Stereo Audio Sigma-Delta Digital-to-Analog Converter

## CMOS

The MC145074 is a high precision, Stereo Audio Digital–to–Analog Converter that utilizes second order sigma–delta modulators with 2–tap FIR feedback architecture. The part can be used as a stand alone stereo digital modulator, or as a companion part to the MC145076 smoothing filter to achieve high quality, low cost audio performance.

- Peak S/(N+D) > 100 dB
- Single 5 V Supply Operation
- Accepts 16, 18, or 20–Bit Data Words
- Dual/Single Pin Data Input Modes
- Programmable WCLK Divider
- Operating Temperature Range: – 40 to + 85°C
- Low Power Consumption: 40 mW Typical
- Companion to MC145076 Stereo Audio FIR Smoothing Filter

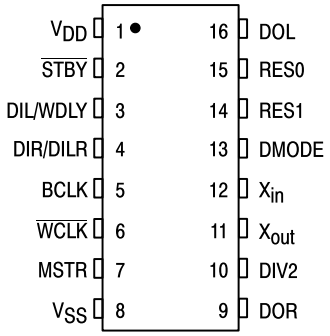


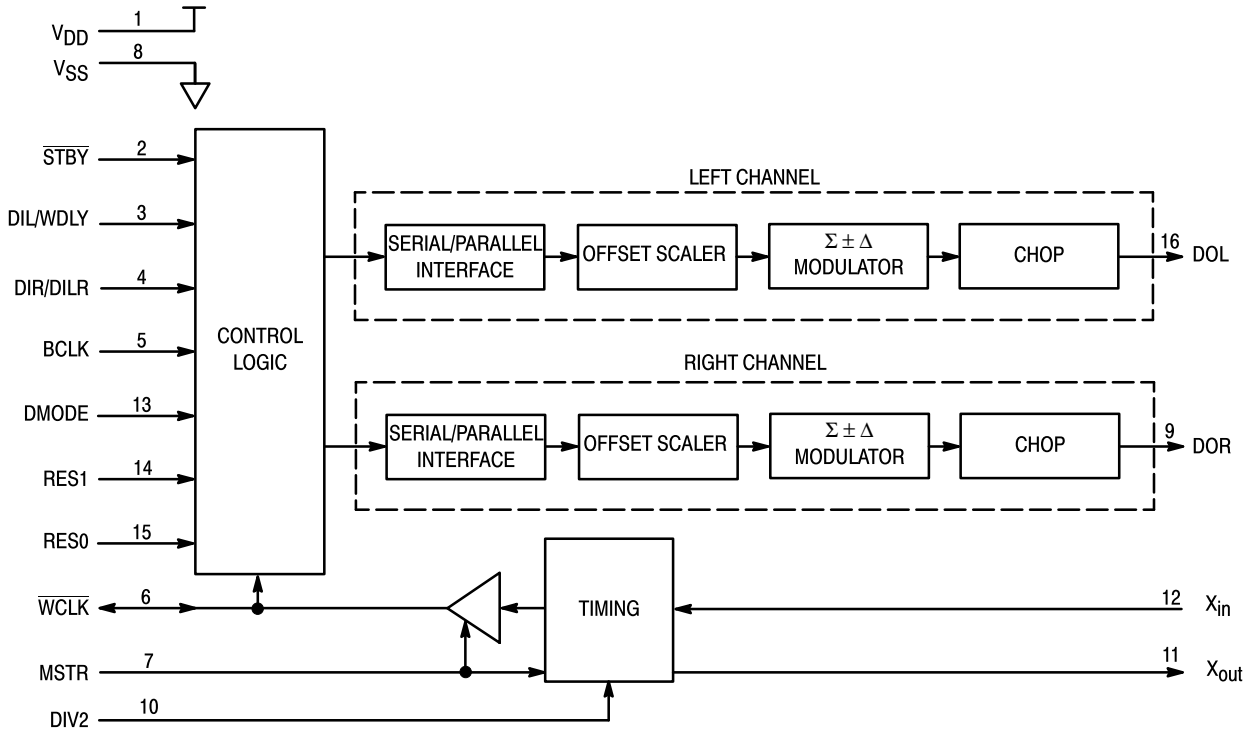

**D SUFFIX**
16 PIN SOIC
CASE 751B

**ORDERING INFORMATION**

| | |
|---|---|
| MC145074D | SOIC Package |

**PIN ASSIGNMENT**




**REV 2**
**3/97 TN97041197**

**MAXIMUM RATINGS*** (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | 6.0 | V |
| $V_{in}$ | DC Input Voltage, Any Digital Input | $V_{SS}$ – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±10 | mA |
| $T_{stg}$ | Storage Temperature | – 55 to 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Operation Ranges below.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

**OPERATION RANGES** (Applicable to Guaranteed Limits)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage, Referenced to $V_{SS}$ | 4.5 to 5.5 | V |
| $V_{in}$, $V_{out}$ | Digital Input/Output Voltage | $V_{SS}$ – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_D$ | Input Pin Current Drain | 1 | µA |
| $T_A$ | Operating Temperature | – 40 to + 85 | °C |

**DC ELECTRICAL CHARACTERISTICS**

(Voltages Referenced to $V_{SS}$, Full Temperature and Voltage Ranges per Operation Ranges table, unless otherwise indicated)

| Symbol | Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{dd}$ | Power Supply Current | | — | — | 10 | mA |
| $V_{IL}$<br>$V_{IH}$ | Input Voltage | Low Level Input<br>High Level Input | —<br>$V_{DD}$ x 0.7 | —<br>— | $V_{DD}$ x 0.3<br>— | V |
| $V_{OL}$<br>$V_{OH}$ | Output Voltage | Low Level Output (Load = 0.4 mA)<br>High Level Output (Load = 0.4 mA) | —<br>$V_{DD}$ – 0.3 | —<br>— | 0.3<br>— | V |
| $I_{lkg}$ | Input Leakage Current | | — | — | ± 10 | µA |

**AC ELECTRICAL CHARACTERISTICS**

(Full Temperature and Voltage Ranges per Operation Ranges Table at 50 pf Loads on Outputs)

(Output Current Loads = 400 μA)

| Symbol | Parameter | Figure | Guaranteed Limit | Unit |
|---|---|---|---|---|
| | Operating Frequency $X_{in}$ (DIV2 = 0)<br>(DIV2 = 1) | | 18.5<br>37.0 | MHz |
| | Bit Clock Frequency | | 18.5 | MHz |
| $t_r$, $t_f$ | Maximum Rise and Fall Times (BCLK, WCLK) | 2, 5 | 6 | ns |
| $t_{PLH}$<br>$t_{TLH}$ | $X_{out}$ L–H Propagation Delay<br>$X_{out}$ Rise Time | 2 | 10<br>20 | ns |
| $t_{PHL}$<br>$t_{THL}$ | $X_{out}$ H–L Propagation Delay<br>$X_{out}$ Fall Time | 2 | 10<br>20 | ns |
| $t_{PLH}$<br>$t_{TLH}$ | DOL, DOR L–H Propagation Delays<br>DOL, DOR Rise Time | 3 | 15<br>7.5 | ns |
| $t_{PHL}$<br>$t_{THL}$ | DOL, DOR H–L Propagation Delays<br>DOL, DOR Fall Time | 3 | 15<br>7.5 | ns |
| $t_{PLH}$<br>$t_{TLH}$ | $\overline{WCLK}$ Output L–H Propagation Delay<br>$\overline{WCLK}$ Output Rise Time | 4 | 15<br>7.5 | ns |
| $t_{PHL}$<br>$t_{THL}$ | $\overline{WCLK}$ Output H–L Propagation Delay<br>$\overline{WCLK}$ Output Fall Time | 4 | 15<br>7.5 | ns |
| $t_{su}$<br>$t_h$ | DIR Master Program Mode Minimum Setup Time<br>DIR Master Program Mode Minimum Hold Time | 5 | 5<br>5 | ns |
| $t_{su}$<br>$t_h$ | DIR, DIL Minimum Setup Time<br>DIR, DIL Minimum Hold Time | 5 | 5<br>5 | ns |
| $t_{su}$<br>$t_h$ | $\overline{WCLK}$ Minimum Setup Time to BCLK (not DMODE = WDLY = 1)<br>$\overline{WCLK}$ Minimum Hold Time to BCLK (not DMODE = WDLY = 1) | 6 | 5<br>5 | ns |
| $t_{su}$<br>$t_h$ | $\overline{WCLK}$ Minimum Setup Time to $X_{in}$ (not DMODE = WDLY = 1)<br>$\overline{WCLK}$ Minimum Hold Time to $X_{in}$ (not DMODE = WDLY = 1) | 6 | 5<br>5 | ns |
| $t_{su}$<br>$t_h$ | $\overline{WCLK}$ Minimum Setup Time to BCLK (DMODE = WDLY = 1)<br>$\overline{WCLK}$ Minimum Hold Time to BCLK (DMODE = WDLY = 1) | 7 | 5<br>5 | ns |
| $t_{LAG}$<br>$t_{LEAD}$ | BCLK to $X_{in}$ (1st Edge Only) Lag Time (DMODE = WDLY = 1)<br>BCLK to $X_{in}$ (1st Edge Only) Lead Time (DMODE = WDLY = 1) | 7 | 5<br>5 | ns |

## SWITCHING WAVEFORMS

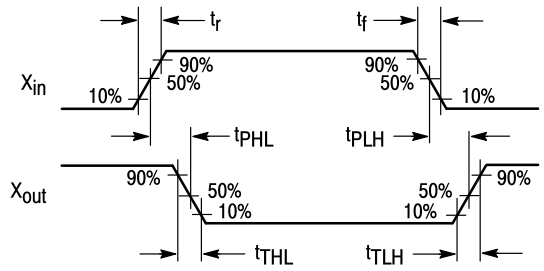



**Figure 1. $X_{out}$ Propagation Delay Timing**

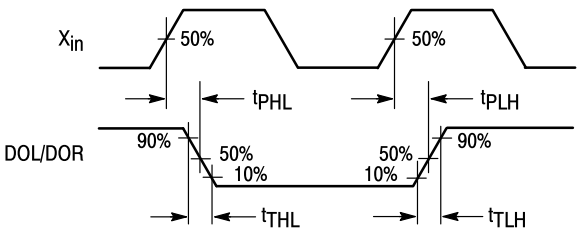



**Figure 2. DOL/DOR Propagation Delay Timing**

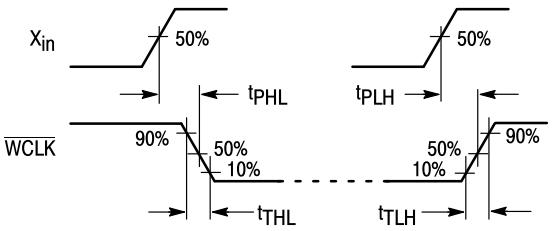



**Figure 3. $\overline{WCLK}$ Out Propagation Delay Timing (Master Mode)**

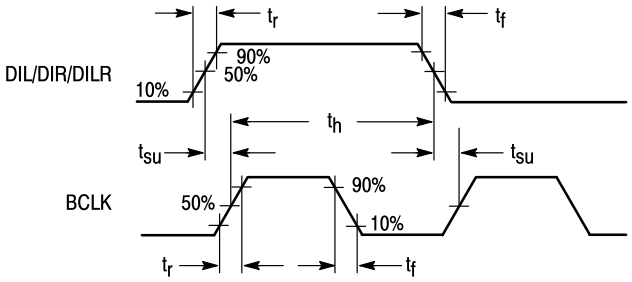



**Figure 4. DIL/DIR/DILR Setup and Hold Timing**

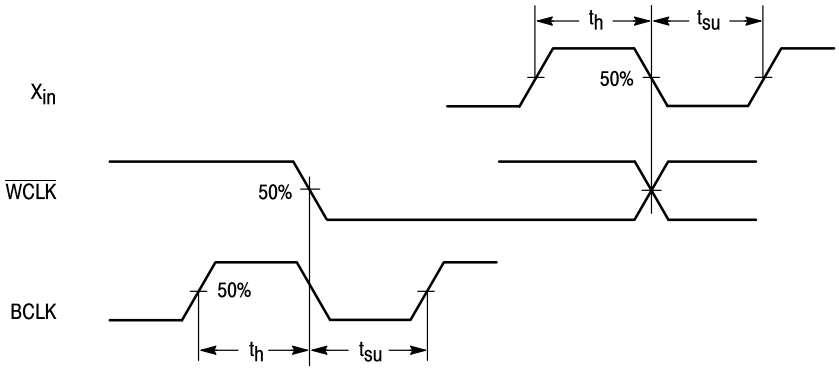



**Figure 5. $\overline{WCLK}$ Timing (All Modes Except DMODE = 1, WDLY = 1)**

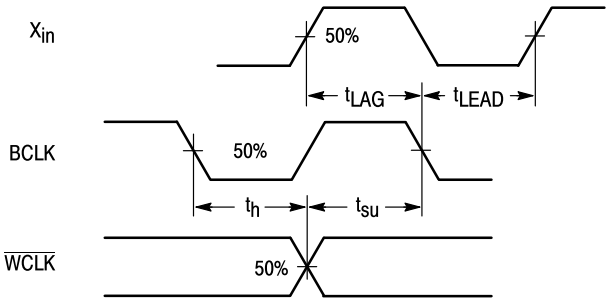



**Figure 6. $\overline{WCLK}$ Timing (DMODE = 1, WDLY = 1)**

| Bits / OSR | 16<br>S/(N+D) dB | 18<br>S/(N+D) dB | 20<br>S/(N+D) dB |
|---|---|---|---|
| 128x | 90 | 90 | 90 |
| 192x | 94 | 98 | 99 |
| 256x | 95 | 103 | 105 |
| 384x | 96 | 107 | 113 |

NOTE: Values are for 0 dB input signal, 0 – 20 kHz BW, and 44.1 kHz 1x fs Sampling Rate.

**Figure 7. Digital S/(N+D) Performance Levels**

## PIN DESCRIPTIONS

**$V_{DD}$**
**Positive Device Supply (Pin 1)**

$V_{DD}$ is the positive supply, nominally + 5 volts.

**$\overline{STBY}$**
**Active–Low Standby Input (Pin 2)**

A low level on the $\overline{STBY}$ pin will force the device into a standby state. If the device is being operated in the master mode (MSTR = 1), the $\overline{WCLK}$ internal divider can be programmed using the DIR/DILR, and BCLK pins while the $\overline{STBY}$ pin is active. When the device is in standby, the DOL and DOR pins will output a 50% duty cycle data stream that will generate a 1/2 scale analog output, when averaged through the output filter.

**DIL/WDLY**
**Left Channel Data/Word Clock Delay Input (Pin 3)**

When the DMODE pin is low, this pin is the left channel (MSB first) 2's complement serial data input. When the DMODE pin is high, this pin controls the $\overline{WCLK}$ delay. A high level on this pin will delay the $\overline{WCLK}$ an additional clock cycle internal to the device.

**DIR/DILR**
**Right Channel Data/Multiplexed Left – Right Data Input (Pin 4)**

When the DMODE pin is low, this pin is the right channel (MSB first) 2's complement serial data input. When the DMODE pin is high, this pin is the multiplexed left then right channel data input. If the part is being operated in the master mode (MSTR = 1), the $\overline{WCLK}$ internal divider can be programmed by clocking control word data onto this pin with the BCLK pin while the device is in the standby mode ($\overline{STBY}$ = 0).

**BCLK**
**Bit Clock Input (Pin 5)**

The BCLK pin provides the serial bit shift clock for the left and right channel data in all modes of operation. A rising edge on the BCLK pin shifts serial data into the device.

**$\overline{WCLK}$**
**Word Clock Output/Input (Pin 6)**

The $\overline{WCLK}$ pin is used to latch the shifted serial data word into the device. The MC145074 can accept an external word clock when in the slave mode, or can use an internally generated word clock when operating in the master mode. When DMODE is low, left and right channel data is latched into the device on the falling edge of $\overline{WCLK}$. When DMODE is high, left channel data is latched on the rising edge of $\overline{WCLK}$ and right channel data is latched on the falling edge of $\overline{WCLK}$ with both channel inputs being input to the modulator on the next rising edge of $\overline{WCLK}$. The internal divide ratio used to generate $\overline{WCLK}$, as well as the rising or falling edge latching of the input data can be programmed using the DIR/DILR and BCLK pins while the device is in the standby mode.

**MSTR**
**Active–High Master Mode Select Input (Pin 7)**

A high level on the MSTR pin will select the master mode of operation. In the master mode, the MC145074 will generate and output a word clock signal on the $\overline{WCLK}$ pin. A low level on the MSTR pin will place the MC145074 in the slave mode, and the $\overline{WCLK}$ signal must be provided by an external source. The default master mode divide rate is MODCLK/64.

**$V_{SS}$**
**Device Ground (Pin 8)**

$V_{SS}$ is normally connected to ground.

**DOR**
**Right Channel Data Output (Pin 9)**

DOR is the right channel modulator data output.

**DIV2**
**Master Clock Divide Control Input (Pin 10)**

DIV2 is the $X_{in}$ divide by two control pin. When cleared, the $X_{in}$ pin directly provides the modulator clock (MODCLK), and the data output bit streams are not chopped. When this pin is set, the $X_{in}$ clock is divided by two to provide the modulator clock and the output data bit stream is chopped at the $X_{in}$ frequency using an alternating 1,0 chop. The chop is used to reduce even order distortion for a stand–alone application without the MC145076. The reconstructed output signal will drop 6dB due to the chopping.

**$X_{out}$**
**Master Clock Output (Pin 11)**

$X_{out}$ is the inverted output signal of $X_{in}$ and may be used for a buffered clock output or for a crystal oscillator.

**$X_{in}$**
**Master Clock Input (Pin 12)**

$X_{in}$ is the input clock pin for the MC145074, and may be used with $X_{out}$ as the inverter for a crystal oscillator.

**DMODE**
**Data Mode Input (Pin 13)**

A low level on the DMODE pin will select the dual data pin mode of operation. In this mode, the serial input data is entered on the DIR and DIL pins. A high level on the DMODE pin selects the multiplexed mode of operation. In this mode, the left and right channel serial input data must be multiplexed on the DIR/DILR pin.

**RES0 and RES1**
**Input Data Resolution Pins (Pins 14, 15)**

The RES0 and RES1 pins select the length of the serial data word input to the MC145074. The serial input data can be 16, 18, or 20–bits in length with the most significant bits clocked in first. Figure 9 lists the serial interface formats.

**DOL**
**Left Channel Data Output (Pin 16)**

DOL is the left channel modulator data output.

| DMODE | RES1 | RES0 | Operating Mode |
|---|---|---|---|
| 0 | 0 | 0 | Dual Data Pin 16–Bit Input |
| 0 | 0 | 1 | Dual Data Pin 18–Bit Input |
| 0 | 1 | 0 | Dual Data Pin 20–Bit Input |
| 0 | 1 | 1 | Factory Test Mode |
| 1 | 0 | 0 | Single Data Pin 16–Bit Input |
| 1 | 0 | 1 | Single Data Pin 18–Bit Input |
| 1 | 1 | 0 | Single Data Pin 20–Bit Input |
| 1 | 1 | 1 | Factory Test Mode |

**Figure 8. Serial Interface Formats**

## FUNCTIONAL DESCRIPTION

The MC145074 is a high precision Stereo Audio Digital–to–Analog Converter, which utilizes a second–order sigma–delta modulator with a patented 2–tap architecture that significantly reduces problems normally associated with one–bit sigma–delta technology. Normally, a second order modulator can develop patterns in the digital output representation of small signals and with small DC input offsets. It is common to add dither to mask these effects, but a reduction of dynamic range can result. The implementation used in the MC145074 has considerable immunity to these troublesome inputs, and without performance compromise.

With RC filtering, the MC145074 can be used as a stand–alone stereo digital modulator for applications with modest requirements. High performance can be realized with the companion MC145076 Stereo Audio FIR Smoothing Filter, which reduces the in–band IM products formed by large amplitude spectral components of the out–of–band noise shaping, clock corruption, and power supply noise.

The MC145074 has been designed for maximum flexibility and is well suited for high fidelity audio and multimedia applications. If used in conjunction with a differential MC145076 smoothing filter, a peak S/(N+D) ratio of > 100 dB can be achieved by utilizing 18 or 20–bit input data and a 256x oversampling ratio. The MC145074 has a maximum operating frequency of 18.5 MHz, and can be used with any sampling rate including 32, 44.1, or 48 kHz.

The MC145074 can accept a 1x, or a 2x input clock with serial data output chop. The device can accept 16, 18, or 20–bit digital data in a dual data pin input format, or single pin multiplexed format. An offset scaler is included to allow 0 dB digital inputs while maintaining low distortion. The offset, scaled data is applied to the D/A modulator before being optionally chopped (2x mode), and sent to an external smoothing filter. When this device is used with the MC145076, dividing the clock down or using the chop mode is not necessary.

## TIMING CIRCUIT

The internal timing circuits of the MC145074 are driven by the $X_{in}$ clock. When the DIV2 pin is active high, the MC145074 divides the $X_{in}$ clock by two to generate the internal modulator clock (MODCLK), and uses the $X_{in}$ clock frequency to chop the output data using a 50% chop signal.

When the MC145074 is operated in the master mode, the $\overline{WCLK}$ pin is configured as an output. The $\overline{WCLK}$ output is generated by dividing down the modulator clock. The divide ratio of the internal frequency divider can be programmed utilizing a 5–bit control word while the MC145074 is in the standby mode. The 5–bit control word is defined as the last 5–bits (MSB first) that are clocked into the DIR/DILR pin using the BCLK signal. When cleared, the most significant bit of the control word indicates that the $\overline{WCLK}$ signal is negative edge triggered (just as in the slave mode). If the most significant bit is set, the $\overline{WCLK}$ is positive edge triggered. The next three most significant or middle three bits of the control word determine the value of the divide ratio of the internal frequency divider. The least significant bit of the 5–bit control word indicates a prescaler divide by two when cleared, and divide by three when set. The divider modes are summarized in Figure 10.

**NOTE**

The default mode of operation is control word $06 which provides a $\overline{WCLK}$ signal (negative edge triggered) at a frequency of 1/64 the modulator clock frequency. This is the preferred operating mode of 256x OSR and 4x FIR.

| Control Word Value (Hex) | Divide Ratio | $\overline{WCLK}$ Edge | Control Word Value (Hex) | Divide Ratio | $\overline{WCLK}$ Edge |
|---|---|---|---|---|---|
| 0 | 8 | | 10 | 8 | |
| 1 | 12 | | 11 | 12 | |
| 2 | 16 | | 12 | 16 | |
| 3 | 24 | | 13 | 24 | |
| 4 | 32 | | 14 | 32 | |
| 5 | 48 | | 15 | 48 | |
| 6 | 64 | | 16 | 64 | |
| 7 | 96 | ↓ | 17 | 96 | ↑ |
| 8 | 128 | | 18 | 128 | |
| 9 | 192 | | 19 | 192 | |
| A | 256 | | 1A | 256 | |
| B | 384 | | 1B | 384 | |
| C | 512 | | 1C | 512 | |
| D | 768 | | 1D | 768 | |
| E | 1024 | | 1E | 1024 | |
| F | 1536 | | 1F | 1536 | |

**Figure 9. $\overline{WCLK}$ Divider Modes**

## OFFSET SCALER

Second order sigma–delta modulators typically give up about 2 dB of dynamic range and an adjustment to the digital input words must be made if full scale digital input word recognition is desired. The offset scaler circuitry of the MC145074 digitally attenuates the input linearly to 3/4 or approximately – 2.5 dB. Figure 11 illustrates the function of the offset scaler block. An ideal DAC would perform as shown in curve one, but the sigma–delta modulator actually operates as shown in curve two. The digital input words to the MC145074 are attenuated to 3/4. This allows the MC145074 to operate on all 2's compliment digital inputs from $80000 to $7FFFF, with the resulting response shown in curve three. In addition to scaling the digital input word, the offset scaler adds a digital dc offset of 1/8th to re–center the digital input word so that the MC145074 output signal is centered around $V_{DD}/2$.

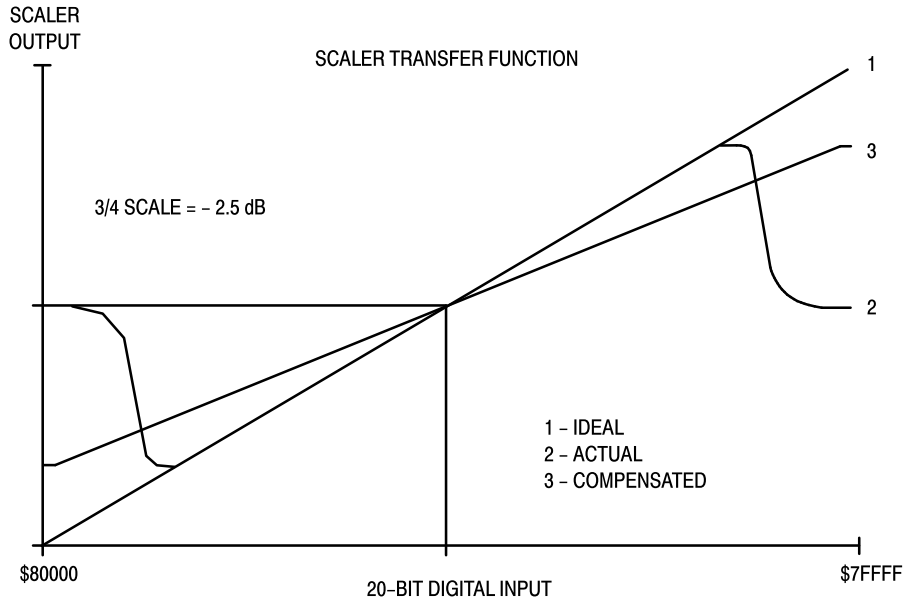



**Figure 10. Offset Scaler Operation**

## SERIAL INTERFACE AND CONTROL LOGIC

The serial interface and control logic of the MC145074 may be configured to accept 16, 18, or 20–bit data words by applying the appropriate logic levels to the RES1 and RES0 pins. The DMODE input pin configures the serial interface to accept 2's complement data (MSB first) in a dual data pin or single pin, multiplexed input format. It should be noted that in some cases when using the single data pin input mode and a large OSR, the BCLK rate may be too high for some DSPs, unless an interface circuit is added. Figure 9 shows the available serial interface formats of the MC145074.

When operating in a dual data pin mode, 2's complement data words are serially input from the DIR and DIL pins as shown in Figure 12. A rising edge on BCLK serially shifts in the data present on the DIR and DIL inputs. After all data bits of an input word are shifted in, a falling edge on $\overline{\text{WCLK}}$ latches the data word into the MC145074. The BCLK can be a continuous clock as long as the serial input data word is right justified in the word time, or as long as there exists one and only one BCLK cycle for every data bit input to the device.

When operating in a single pin multiplexed mode, the DIR input pin is reconfigured as the DILR pin. Left and right channel serial input data is multiplexed into the MC145074 on the DILR pin, and is serially shifted into the part using BCLK as shown in Figure 13. When WDLY is low, left channel data is latched into the part on the rising edge of $\overline{\text{WCLK}}$, and right channel data is latched on the falling edge of $\overline{\text{WCLK}}$. As in the dual data pin mode, the BCLK can be either an asynchronous or continuous clock as long as the serial input data word is right justified in the word time. Forcing WDLY high allows the $\overline{\text{WCLK}}$ cycle to appear one clock cycle early as shown in Figure 14.

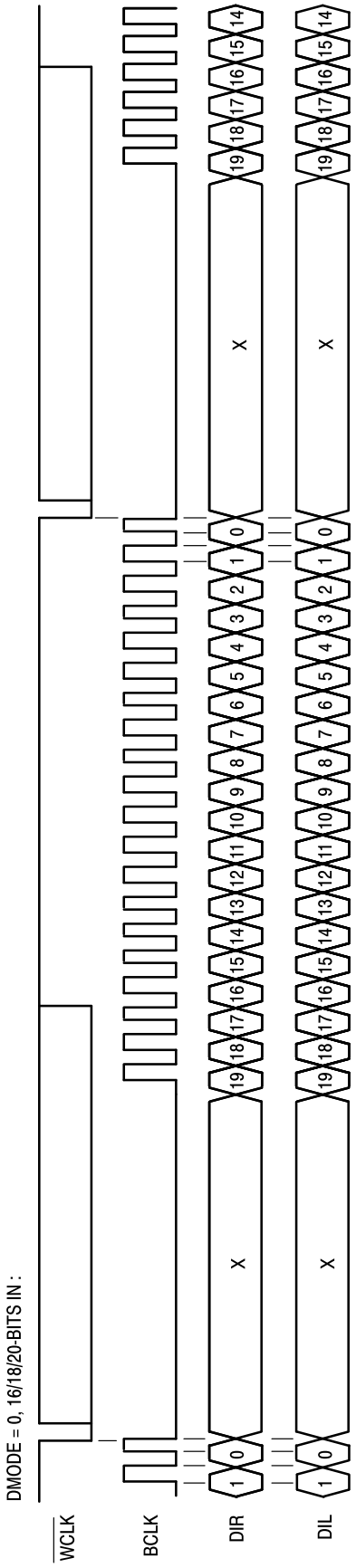



**Figure 11. DMODE = 0 Serial Interface Timing Diagram**

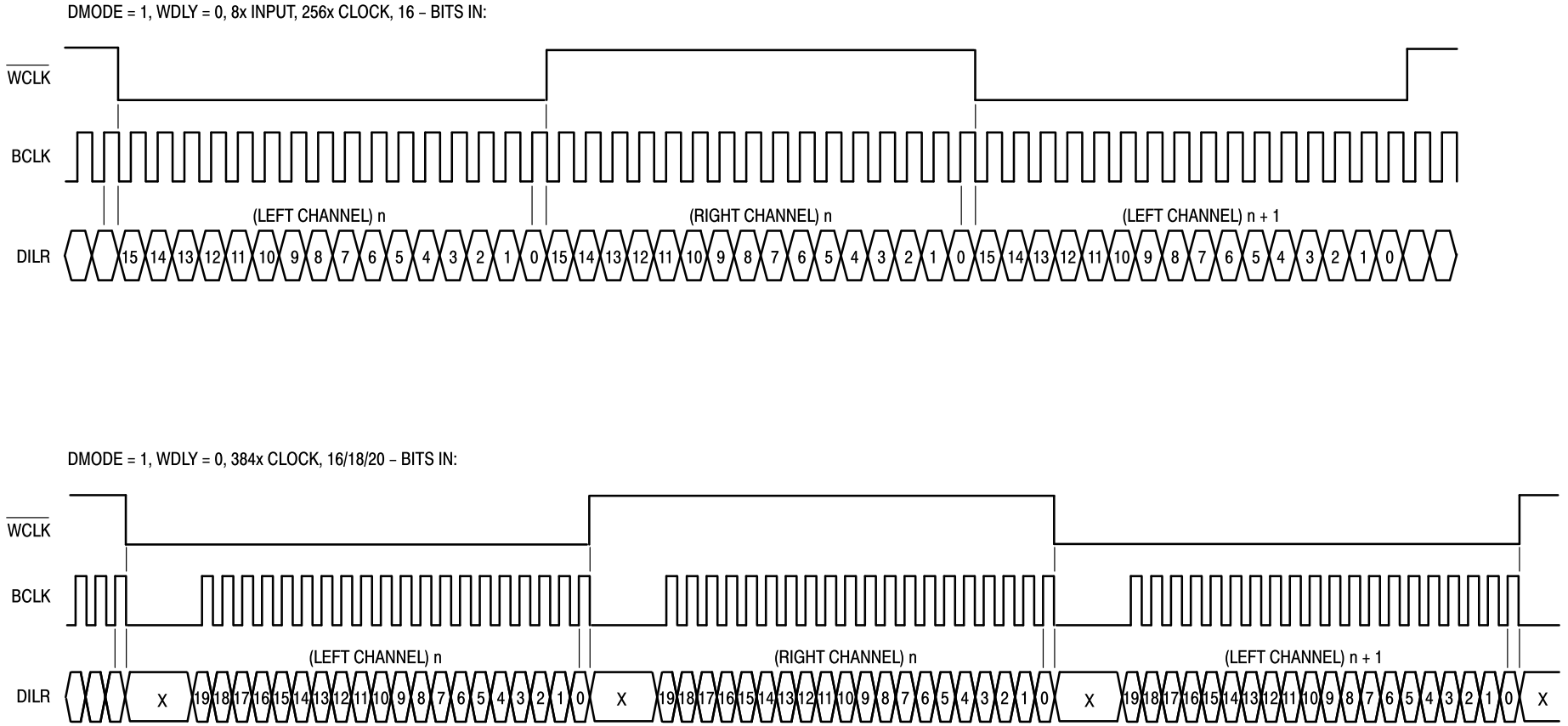



**Figure 12. DMODE = 1, WDLY = 0, Serial Interface Timing Diagram**

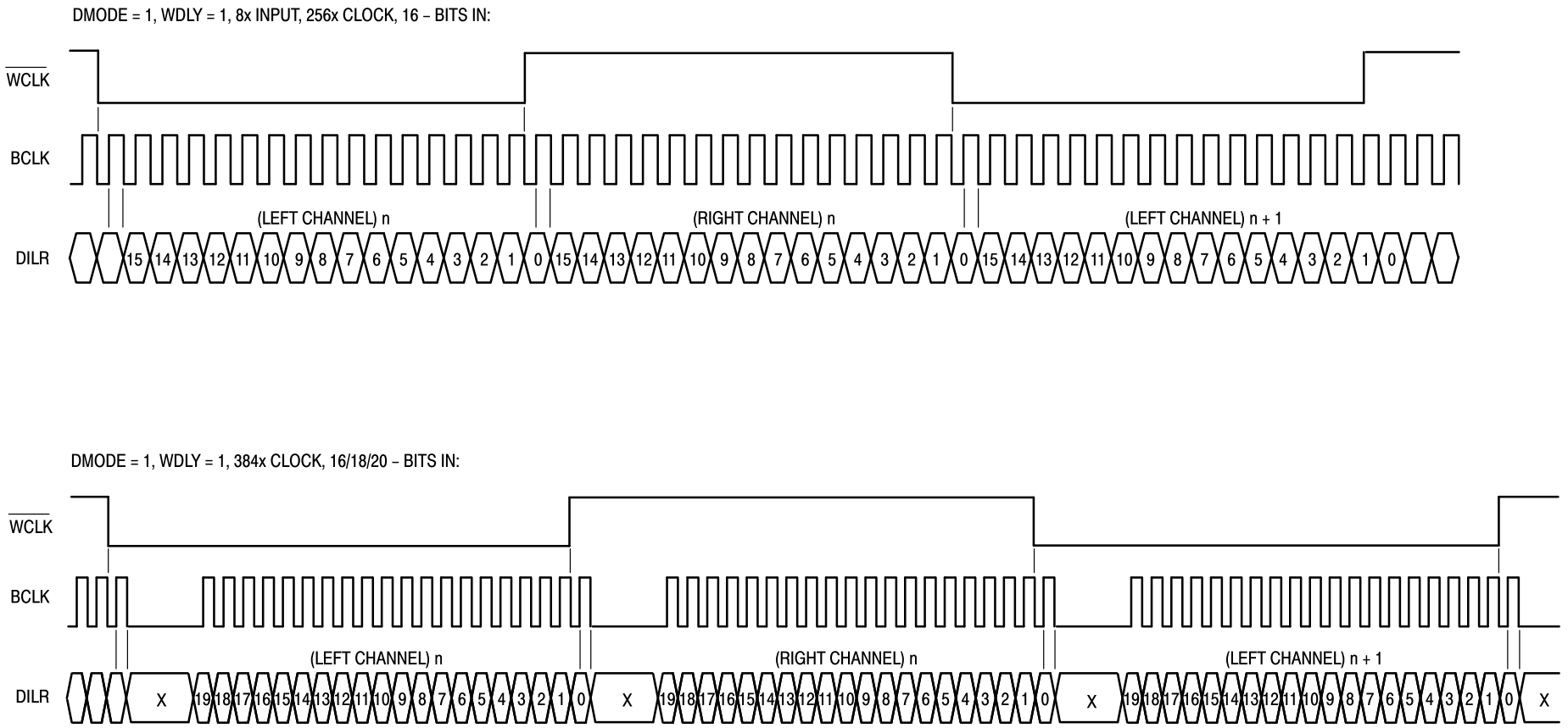



**Figure 13. DMODE = 1, WDLY = 1, Serial Interface Timing Diagram**

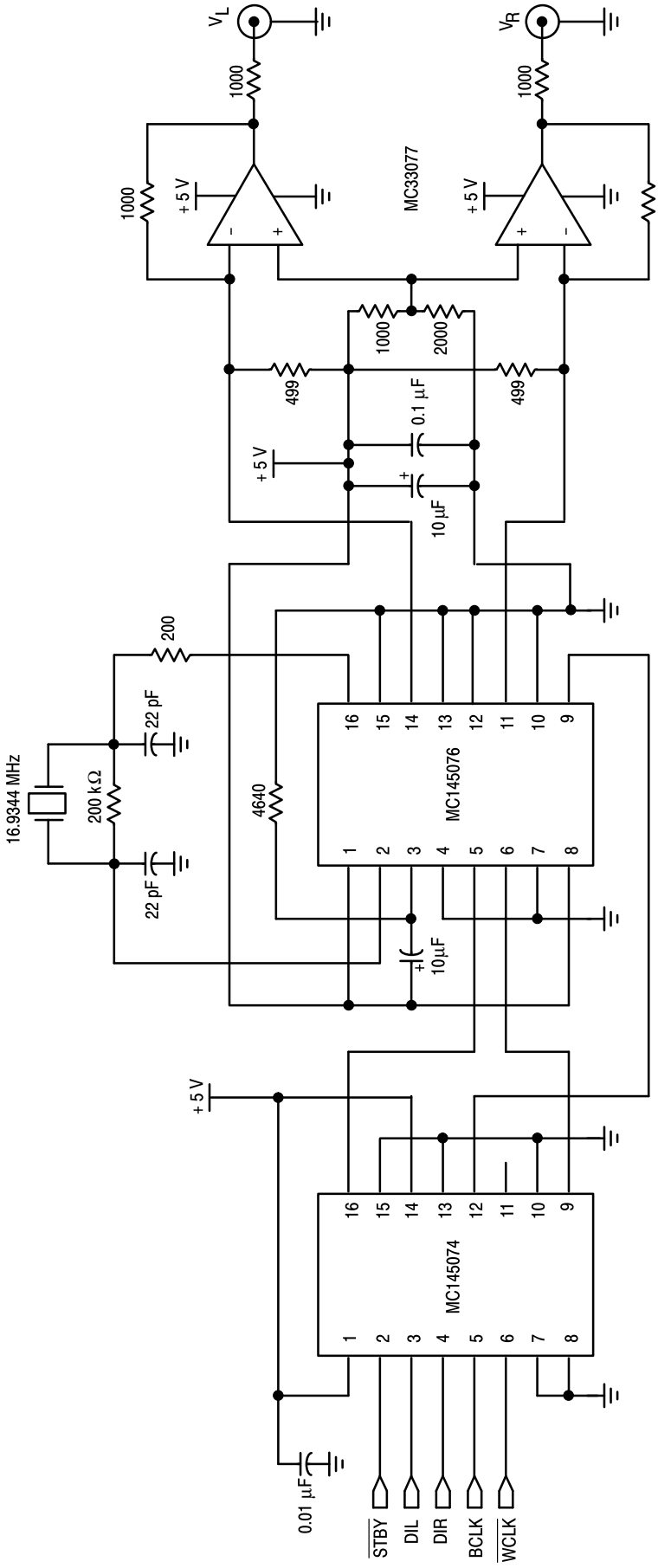



**Figure 14. Low Cost + 5 V Stereo Audio System, Typically 88 dB S/(N+D)**

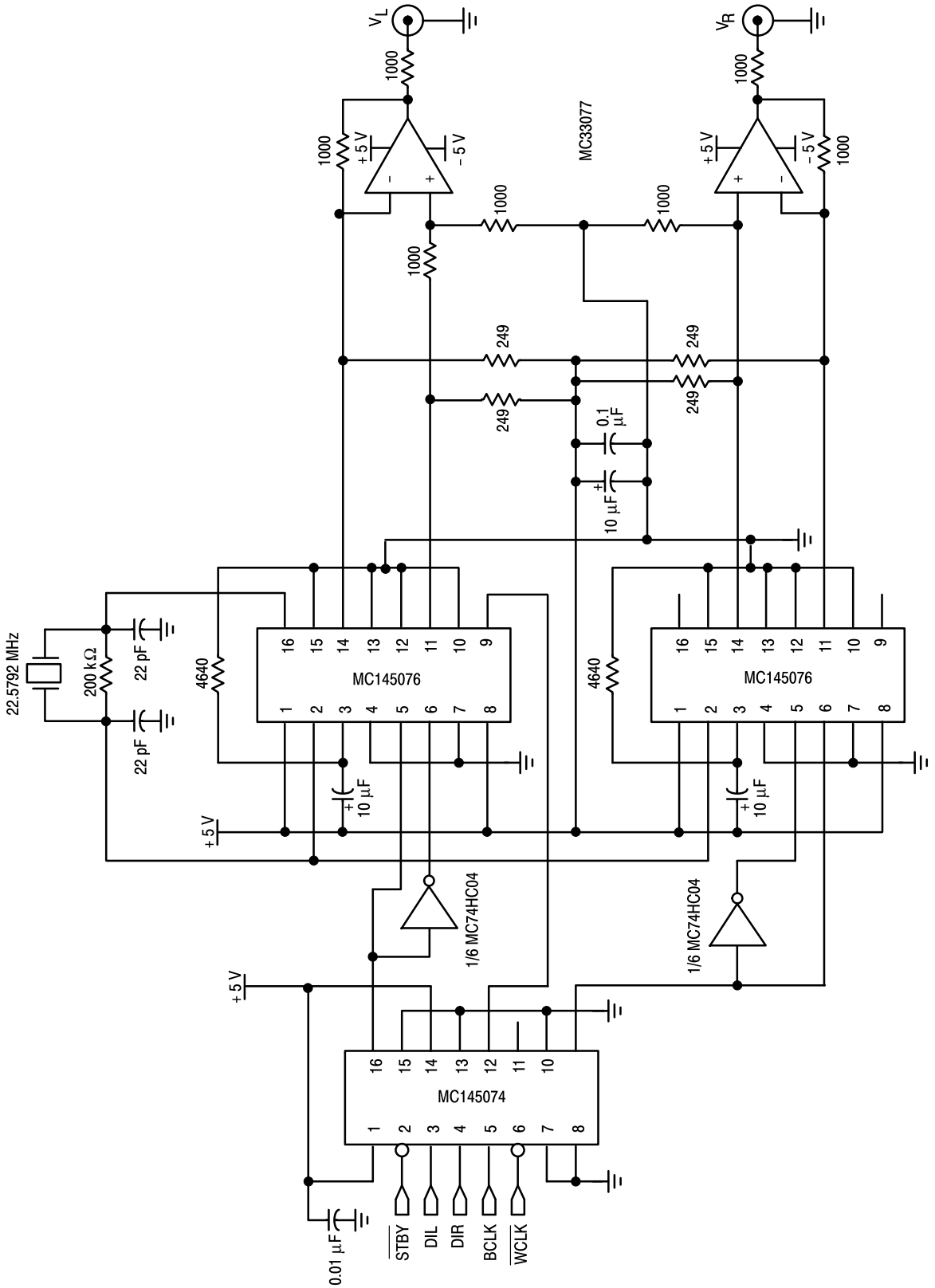



**Figure 15. Mid Performance Stereo Audio System, Typically 98 dB S/(N+D)**

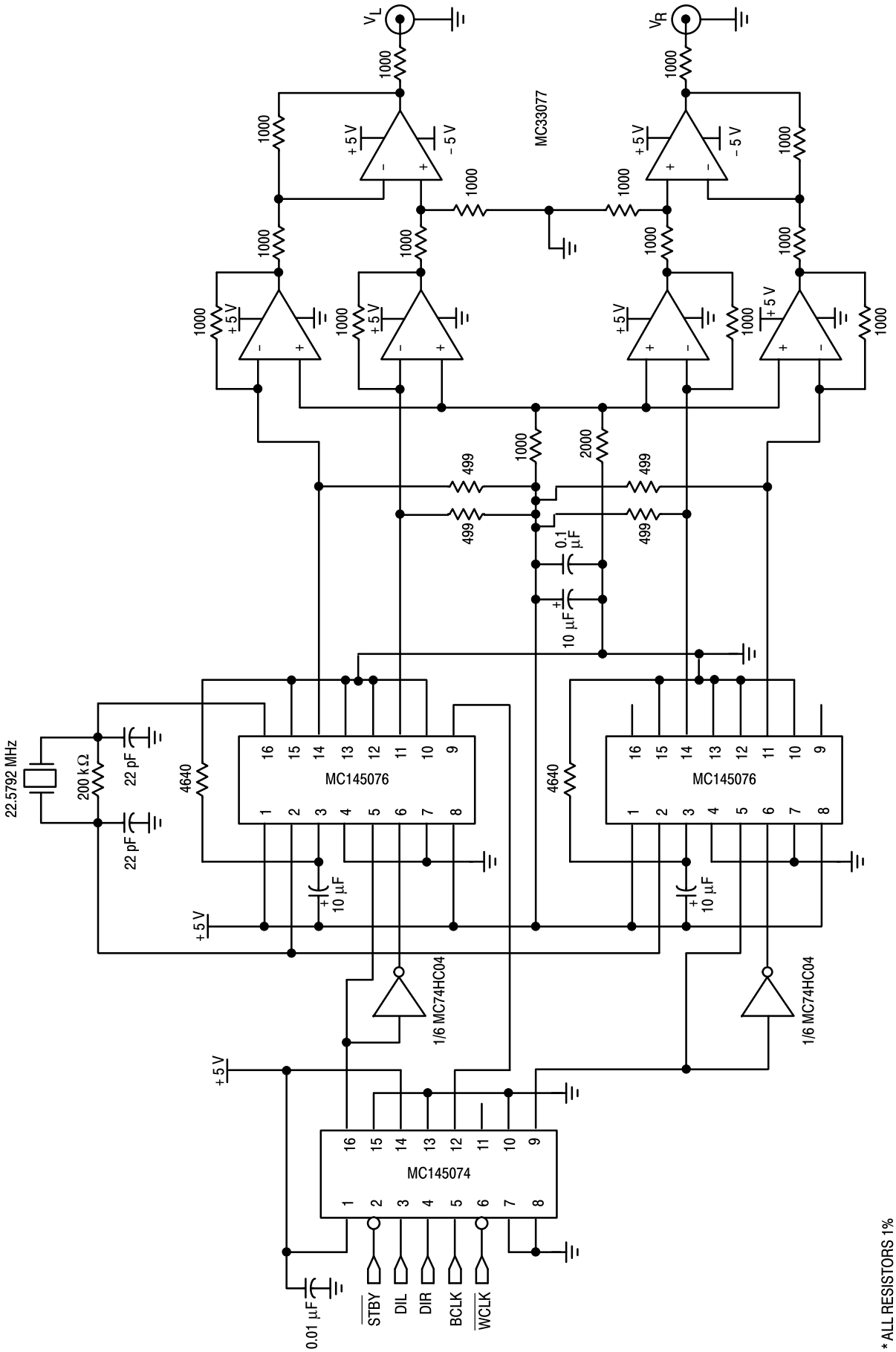
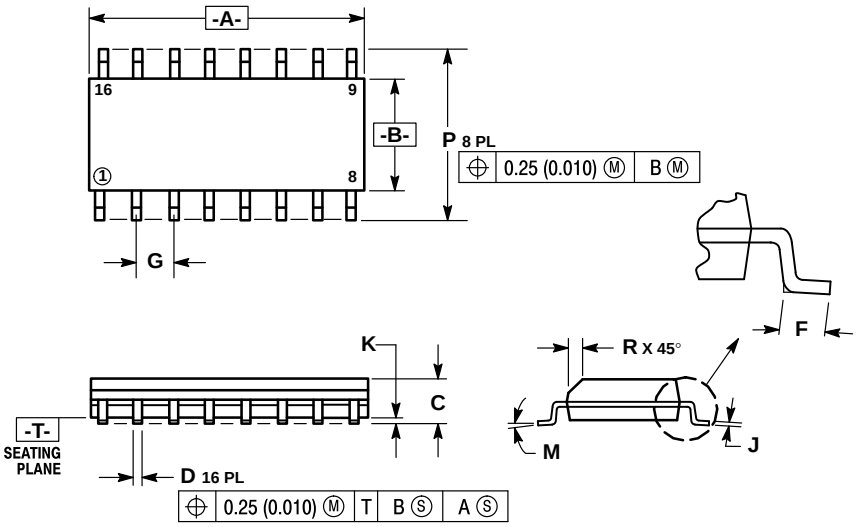



**Figure 16. High Performance Stereo Audio System, Typically 105 dB S/(N+D)**

## PACKAGE DIMENSIONS

**SOIC PACKAGE**
**CASE 751B–05**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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