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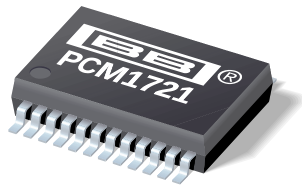


PCM1721

SoundPlus™ Stereo Audio DIGITAL-TO-ANALOG CONVERTER WITH PROGRAMMABLE PLL

FEATURES

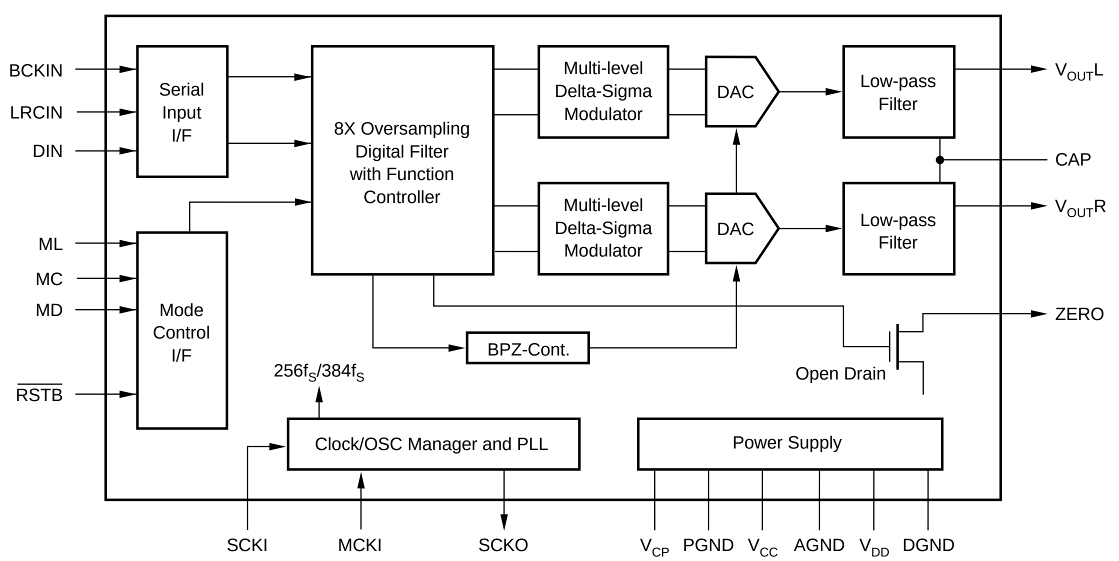
- ACCEPTS 16-, 20-, OR 24-BIT INPUT DATA
- COMPLETE STEREO DAC: Includes Digital Filter and Output Amp
- DYNAMIC RANGE: 94dB
- MULTIPLE SAMPLING FREQUENCIES:
  16kHz, 22.05kHz, 24kHz
  32kHz, 44.1kHz, 48kHz
  64kHz, 88.2kHz, 96kHz
- PROGRAMMABLE PLL CIRCUIT:
  $256f_S/384f_S$ from 27MHz Master Clock
- NORMAL OR I²S DATA INPUT FORMATS
- SELECTABLE FUNCTIONS:
  Soft Mute
  Digital Attenuator (256 Steps)
  Digital De-emphasis
- OUTPUT MODE: Left, Right, Mono, Mute

DESCRIPTION

The PCM1721 is a complete low cost stereo audio digital-to-analog converter (DAC) with a phase-locked loop (PLL) circuit included. The PLL derives either $256f_S$ or $384f_S$ system clock from an external 27MHz reference frequency. The DAC contains a 3rd-order $\Delta\Sigma$ modulator, a digital interpolation filter, and an analog output amplifier. The PCM1721 can accept 16-, 20-, or 24-bit input data in either normal or I²S formats.

The digital filter performs an 8X interpolation function and includes selectable features such as soft mute, digital attenuation and digital de-emphasis. The PLL can be programmed for sampling at standard digital audio frequencies as well as one-half and double sampling frequencies.

The PCM1721 is ideal for applications which combine compressed audio and video data such as DVD, DVD-ROM, set-top boxes and MPEG sound cards.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1319A

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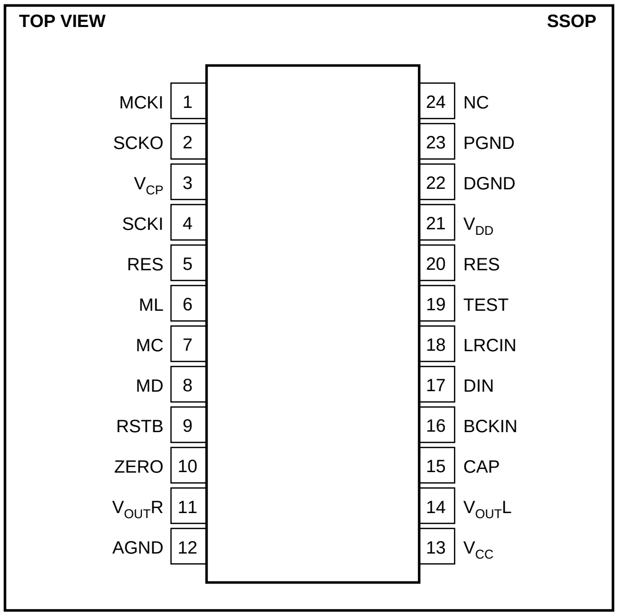
SPECIFICATIONS

All specifications at +25°C, $+V_{CC} = +V_{DD} = +5V$, $f_S = 44.1kHz$, and 16-bit input data, SYSCLK = $384f_S$, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1721			UNITS
		MIN	TYP	MAX	
RESOLUTION		16		24	Bits
DATA FORMAT					
Audio Data Format			Standard/I^2S		
Data Bit Length			16/20/24 Selectable		
Sampling Frequency (f_S)	Standard f_S	32	44.1	48	kHz
	One-half f_S	16	22.05	24	kHz
	Double f_S	64	88.2	96	kHz
PLL PERFORMANCE					
Master Clock Input Frequency			27		MHz
Generated Sysclk Frequency			$256f_S/384f_S$		
Generated Sysclk Jitter	f_M = 27MHz			±250	ps
Generated Sysclk Transient(1)	f_M = 27MHz			20	ms
Generated Sysclk Duty Cycle	f_M = 27MHz, C_L = 15pF	40	50	60	%
DIGITAL INPUT/OUTPUT LOGIC LEVEL			TTL		
DYNAMIC PERFORMANCE(2)					
THD+N at f_S (0dB)	fs = 44.1kHz		–89	–80	dB
	fs = 96kHz		–87		dB
THD+N at –60dB	fs = 44.1kHz		–31		dB
	fs = 96kHz		–29		dB
Dynamic Range (EIAJ Method)	fs = 44.1kHz	90	94		dB
	fs = 96kHz		91		dB
Signal-to-Noise Ratio(3)	fs = 44.1kHz	90	94		dB
	fs = 96kHz		92		dB
Channel Separation	fs = 44.1kHz	88	92		dB
DC ACCURACY					
Gain Error			±1.0	±5.0	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±5.0	% of FSR
Bipolar Zero Error	$V_{OUT} = V_{CC}/2$ at BPZ		±30		mV
ANALOG OUTPUT					
Output Voltage	Full Scale (–0dB)		0.62 x V_{CC}		Vp-p
Center Voltage			$V_{CC}/2$		V_{DC}
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Passband				0.445	f_S
Stopband		0.555			f_S
Passband Ripple				±0.17	dB
Stopband Attenuation		–35			dB
Delay Time			$11.125/f_S$		sec
De-emphasis Error		–0.2		+0.55	dB
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	$V_{CC} = V_{DD} = V_{CP}$	4.5	5	5.5	VDC
Supply Current: $I_{CC} + I_{DD} + I_{CP}$	f_S = 44.1kHz		36	43	mA
$I_{CC} + I_{DD} + I_{CP}$	f_S = 96kHz		49	58	mA
TEMPERATURE RANGE					
Operation		0		+70	°C
Storage		–55		+100	°C

NOTES: (1) Sysclk transient is the maximum frequency lock time when the PLL frequency is changed. (2) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average-Mode. (3) SNR is tested at Infinite Zero Detection off.

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	TYPE	FUNCTION
1	MCKI	IN	Master Clock Input.
2	SCKO	OUT	System Clock Out. This output is $256f_S$ or $384f_S$ system clock generated by the internal PLL.
3	V_{CP}	PWR	PLL Power Supply (+5V)
4	SCKI	IN	System Clock ($256f_S$ or $384f_S$) Input.
5	RES	N/A	Reserved for factory use, do not connect.
6*	ML	IN	Latch for serial control data
7*	MC	IN	Clock for serial control data
8*	MD	IN	Data for serial control
9*	RSTB	IN	Reset Input. When this pin is low, the digital filters and modulators are held in reset.
10	ZERO	OUT	Zero Data Flag. This pin is low when the input data is continuously zero for more than 65, 535 cycles of BCKIN.
11	$V_{OUT}R$	OUT	Right Channel Analog Output
12	AGND	GND	Analog Ground
13	V_{CC}	PWR	Analog Power Supply (+5V)
14	$V_{OUT}L$	OUT	Left Channel Analog Output
15	CAP		Common pin for analog output amplifiers.
16*	BCKIN	IN	Bit clock for clocking in the audio data.
17*	DIN	IN	Serial audio data input
18*	LRCIN	IN	Left/Right Word Clock. Frequency is equal to f_S.
19	TEST	N/A	Test pin, must be tied “LOW”.
20	RES	N/A	Reserved for factory use, do not connect.
21	V_{DD}	PWR	Analog Power Supply (+5V)
22	DGND	GND	Digital Ground
23	PGND	GND	PLL Ground
24	NC	—	No Connection

* These pins include internal pull-up resistors.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1721	24-Pin SSOP	338

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

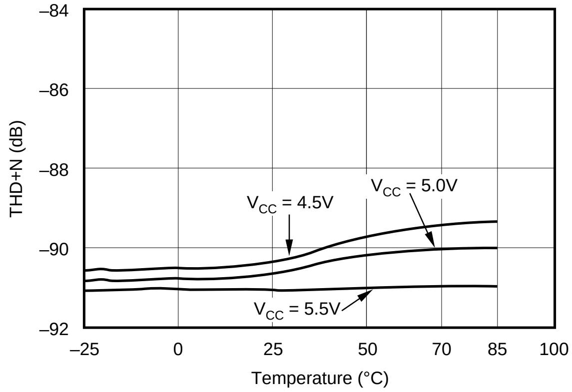
Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Power Dissipation	530mW
Operating Temperature Range	0°C to +70°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C
Thermal Resistance, θ_{JA}	+70°C/W

TYPICAL PERFORMANCE CURVES

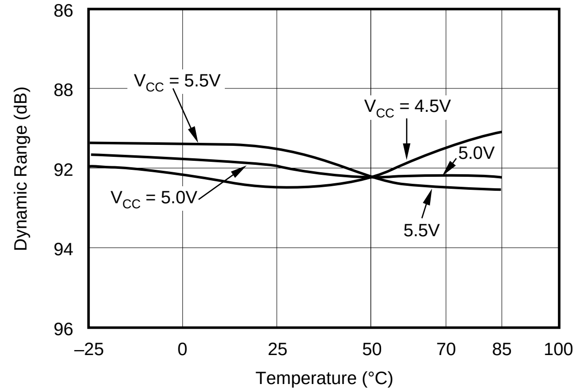
At T_A = +25°C, V_{CC} = V_{DD} = V_{CP} =+5V, f_S = 44.1kHz, 16-bit input data, 384f_S, unless otherwise noted. Measurement bandwidth is 20kHz.

DYNAMIC PERFORMANCE

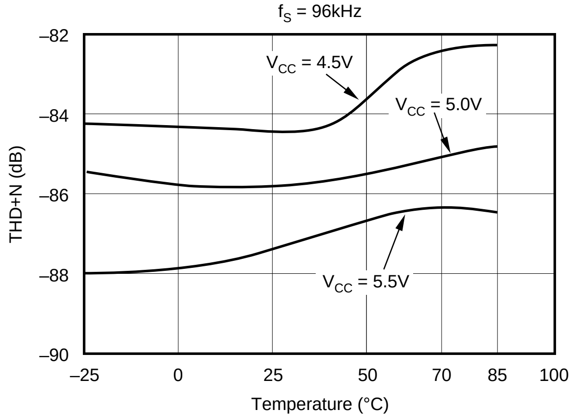
THD+N vs TEMPERATURE and V_{CC}
f_S = 44.1kHz



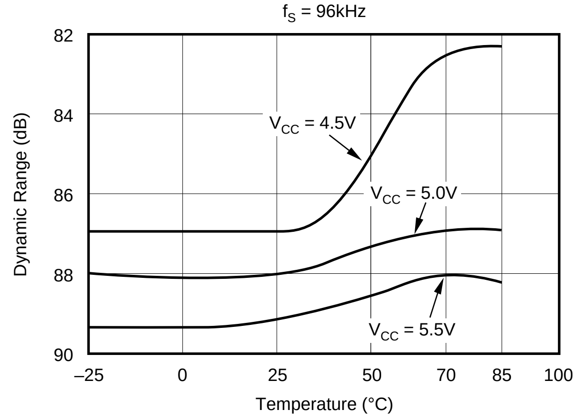
DYNAMIC RANGE vs TEMPERATURE and V_{CC}
f_S = 44.1kHz



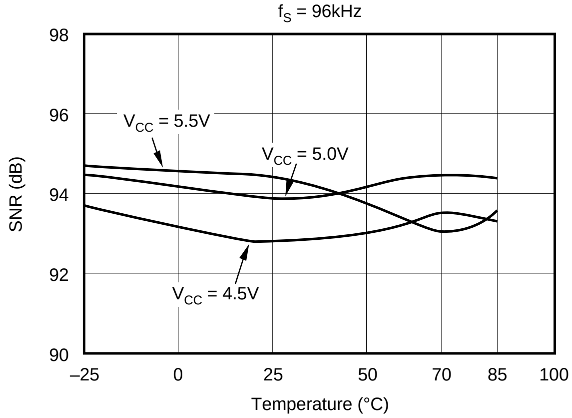
THD+N vs TEMPERATURE and V_{CC}
f_S = 96kHz



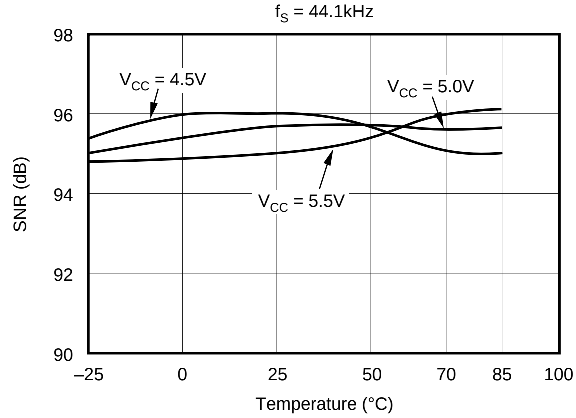
DYNAMIC RANGE vs TEMPERATURE and V_{CC}
f_S = 96kHz



SNR vs TEMPERATURE and V_{CC}
f_S = 96kHz



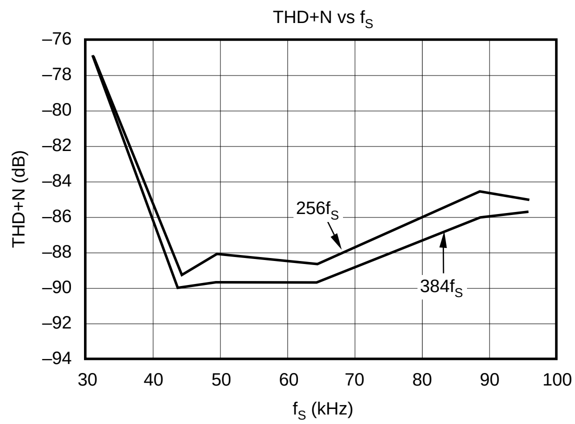
SNR vs TEMPERATURE and V_{CC}
f_S = 44.1kHz

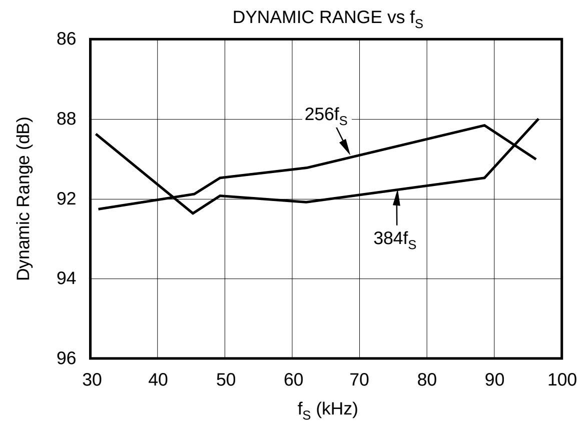


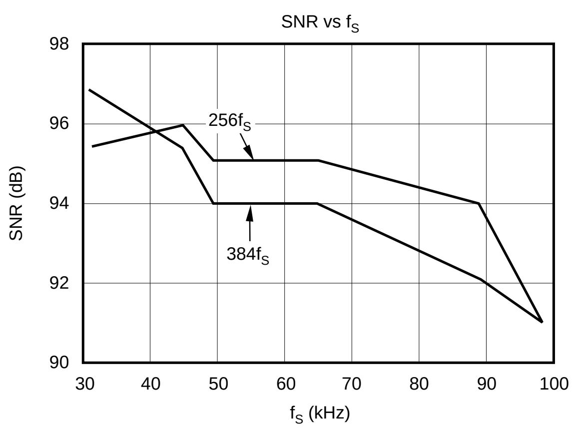
TYPICAL PERFORMANCE CURVES (CONT)

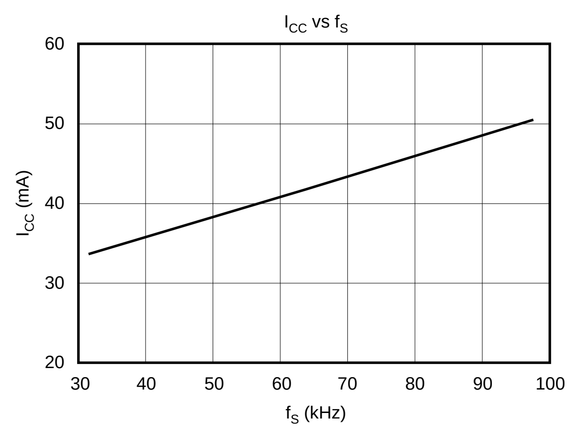
At T_A = +25°C, V_{CC} = V_{DD} = V_{CP} =+5V, f_S = 44.1kHz, 16-bit input data, $384f_S$, unless otherwise noted. Measurement bandwidth is 20kHz.

DYNAMIC PERFORMANCE





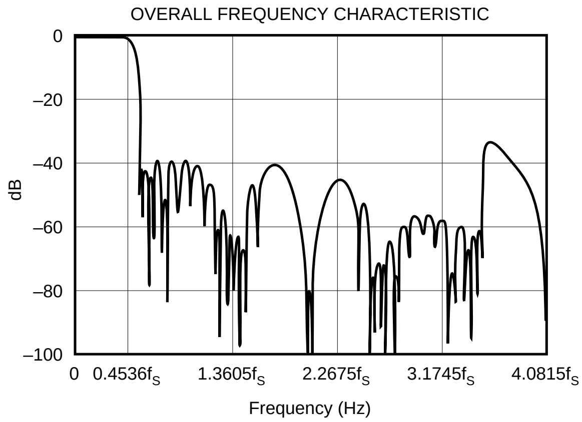


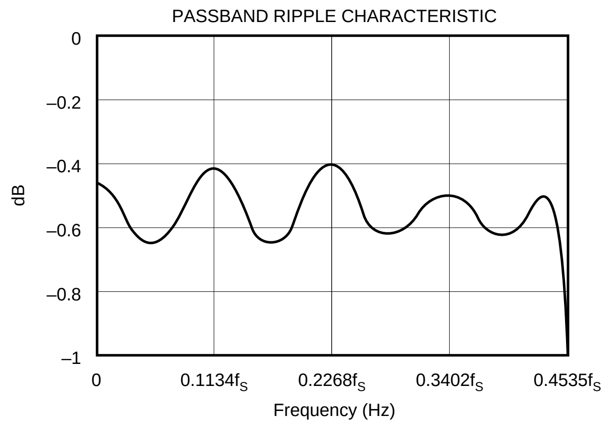


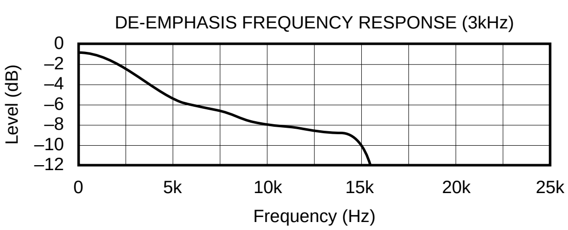
TYPICAL PERFORMANCE CURVES

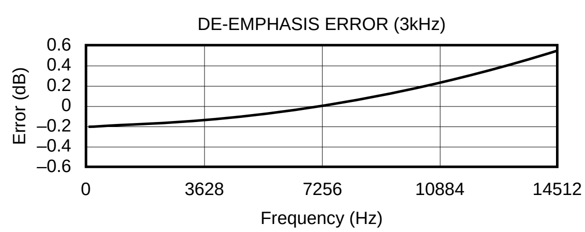
At T_A = +25°C, V_S = +5V, R_L = 44.1kHz, and f_{SYS} = 384f_S, unless otherwise noted.

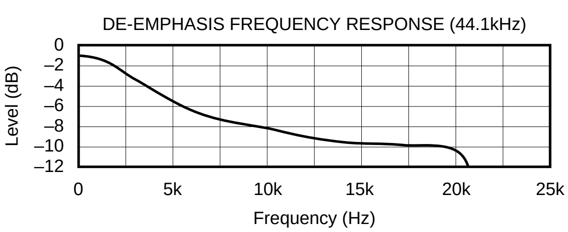
DIGITAL FILTER

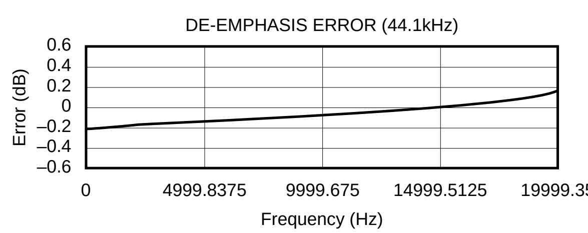


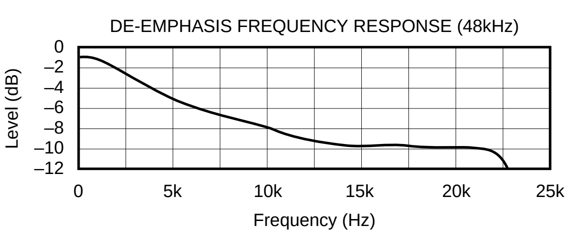


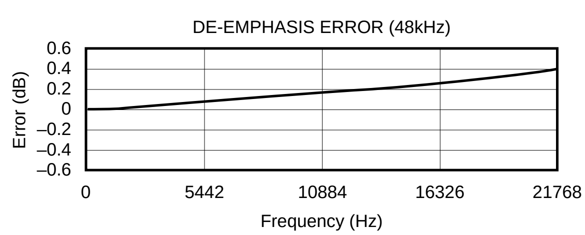












TYPICAL CONNECTION DIAGRAM

Figure 1 illustrates the typical connection diagram for PCM1721 in a MPEG2 application. The 27MHz master video clock (f_M) drives MCKI (pin 1) of PCM1721. A programmable system clock is generated by the PCM1721 PLL, with SCKO used to drive the MPEG2 decoder's system clock input. The standard audio signals (data, bit clock, and word clock) are generated in the decoder from PCM1721's system clock, providing synchonization of audio and video signals.

PLL CIRCUIT

PCM1721 has a programmable internal PLL circuit, as shown in Figure 2. The PLL is designed to accept a 27MHz master clock and generate all internal system clocks required to operate the digital filter and ΔΣ modulator, either at $256f_S$ or $384f_S$. The PLL will directly track any variations in the master clock's frequency, and jitter on the system clock is specified at 250ps maximum. Figure 3 illustrates the timing requirements for the 27MHz master clock.

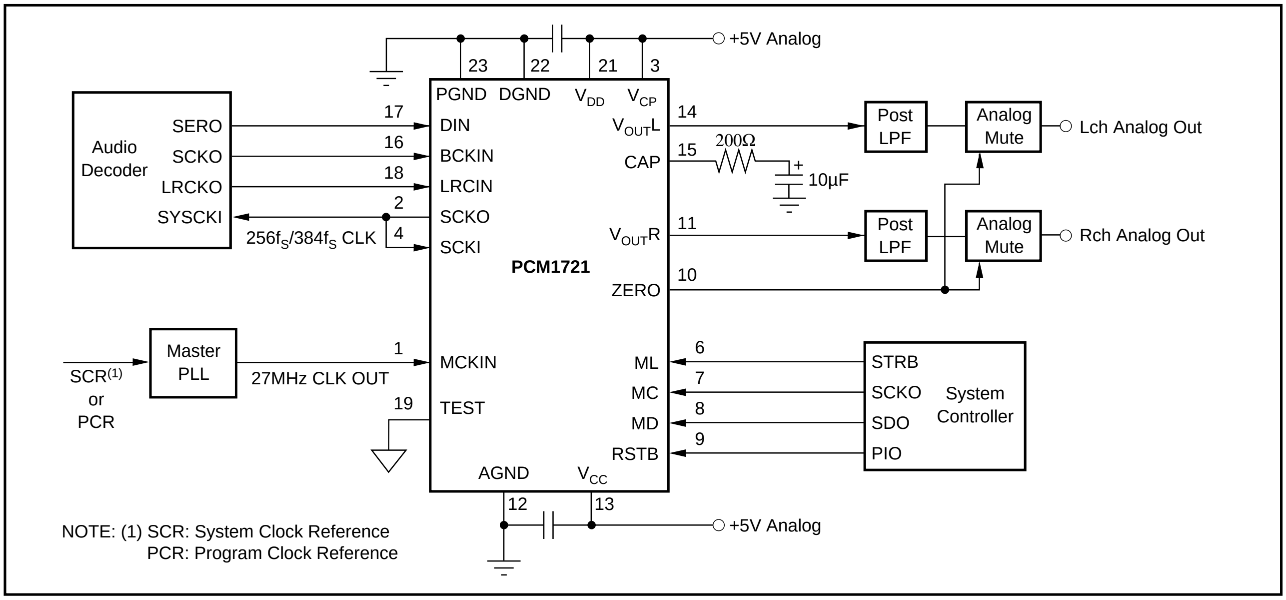


FIGURE 1. External Master Clock Input.

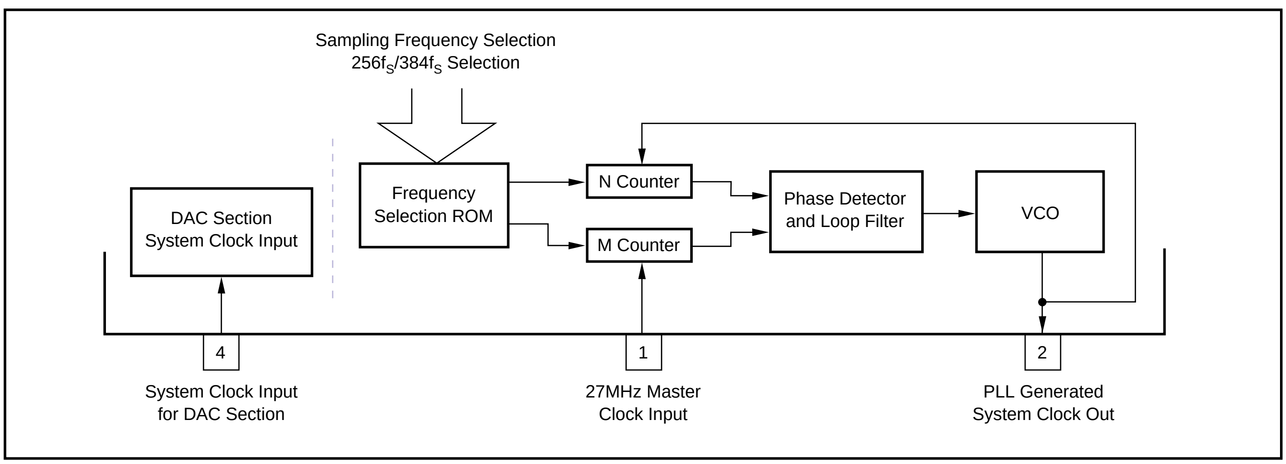


FIGURE 2. PPL Block Diagram.

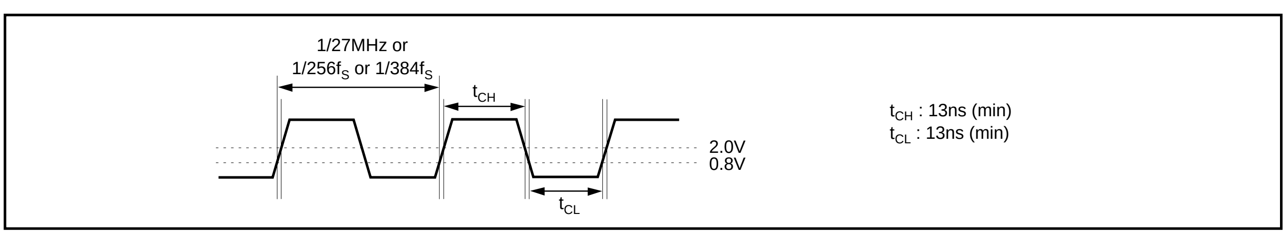


FIGURE 3. MCKI, SCKI Input Timing.

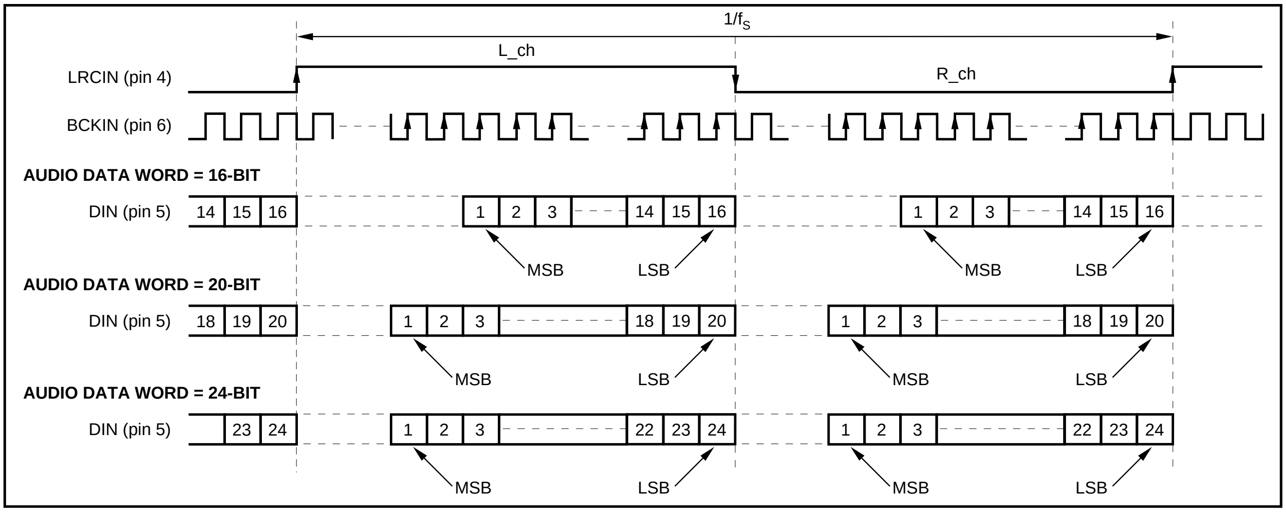


FIGURE 4. "Normal" Data Input Timing.

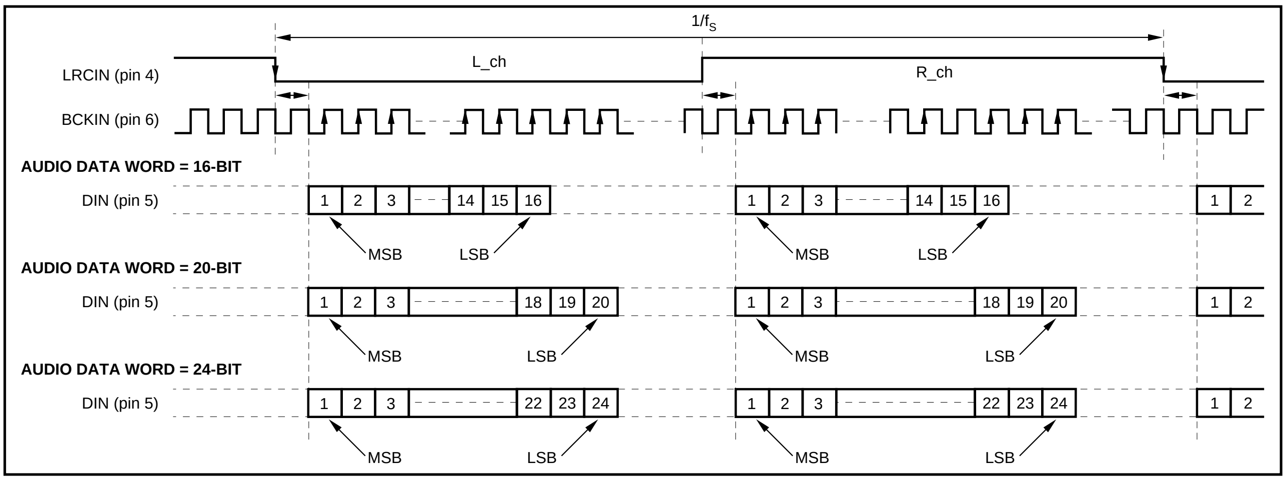
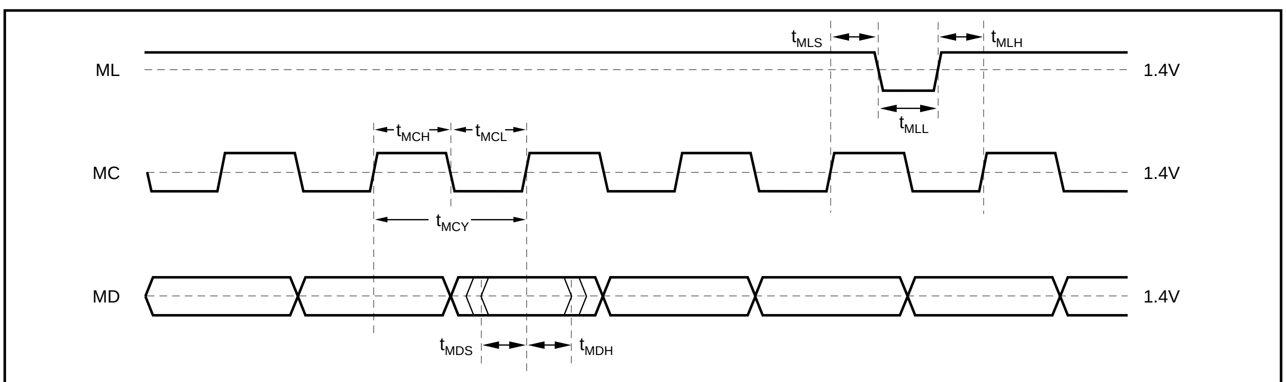


FIGURE 5. "I^{2}S" Data Input Timing.



MC Pulse Cycle Time	: t_{MCY}	: 100ns (min)
MC Pulse Width LOW	: t_{MCL}	: 50ns (min)
MC Pulse Width HIGH	: t_{MCH}	: 50ns (min)
MD Set-up Time	: t_{MDS}	: 30ns (min)
MC Hold Time	: t_{MDH}	: 30ns (min)
ML Low Level Time	: t_{MLL}	: 30ns + 1SYSCLK (min)
ML Set-up Time	: t_{MLS}	: 30ns (min)
ML Hold Time	: t_{MLH}	: 30ns (min)

FIGURE 6. Serial Interface Timing.

	Sampling Frequencies-LRCIN (kHz)		
Half of Standard Sampling Freq	16	22.05	24
Standard Sampling Freq	32	44.1	48
Double of Standard Sampling Freq	64	88.2	96

TABLE I. Sampling Frequencies.

PCM1721's internal PLL can be programmed for nine different sampling frequencies (LRCIN), as shown in Table I. The internal sampling clocks generated by the various programmed frequencies are shown in Table II. Because of finite limitations in the PLL's M and N counters, errors associated with specific frequencies are shown.

	HALF OF STANDARD SAMPLING FREQUENCY						STANDARD SAMPLING FREQUENCY						DOUBLE OF STANDARD SAMPLING FREQUENCY						FREQ ERROR
	$256f_S$ (kHz)			$384f_S$ (kHz)			$256f_S$ (kHz)			$384f_S$ (kHz)			$256f_S$ (kHz)			$384f_S$ (kHz)			%
INTERNAL SYSTEM CLOCK (MHz)	16	22.05	24	16	22.05	24	32	44.1	48	32	44.1	48	64	88.2	96	64	88.2	96	
4.096	4.0982																		0.0537
5.6448		5.64543																	0.0112
6.144			6.13634																–0.1247
6.144				6.13634															–0.1247
8.4672					8.46604														–0.0137
9.216						9.21426													–0.0189
8.192							8.18849												–0.0428
11.2896								11.29087											0.0112
12.288									12.2946										0.0537
12.288										12.2946									0.0537
16.934											16.93215								–0.0133
18.432												18.42851							–0.0189
16.384													16.37699						–0.0428
22.5792														22.58174					0.0112
24.576															24.5892				0.0537
24.576																24.5892			0.0537
33.8688																	33.8643		–0.0133
36.864																		36.85702	–0.0189

TABLE II. Sampling Frequencies vs Internal System Clock.

FUNCTION	DEFAULT MODE
Input Audio Data Format Selection Normal Format I^2S Format	Normal Format
Input Audio Data Bit Selection 16/20/24 Bits	16 Bits
Input LRCIN Polarity Selection Lch/Rch = High/Low Lch/Rch = Low/High	Lch/Rch = High/Low
De-emphasis Control	OFF
Soft Mute Control	OFF
Attenuation Control Lch, Rch Individually Lch, Rch Common	0dB Lch, Rch Individually Fixed
Infinite Zero Detection Circuit Control	OFF
Operation Enable (OPE)	Enabled
Sample Rate Selection Internal System Clock Selection $256f_S$ $384f_S$ Double Sampling Rate Selection Standard Sampling Rate—44.1/48/32kHz Double Sampling Rate—88.2/96/32kHz Half Sampling Rate—22.05/24/16kHz Sampling Frequency 44.1kHz Group 48kHz Group 32kHz Group	$384f_S$ Standard Sampling Rate 44.1kHz
Analog Output Mode L, R, Mono, Mute	Stereo

TABLE III. Selectable Functions.

SPECIAL FUNCTIONS

PCM1721 includes several special functions, including digital attenuation, digital de-emphasis, soft mute, data format selection and input word resolution. These functions are controlled using a three-wire interface. MD (pin 8) is used for the program data, MC (pin 7) is used to clock in the program data, and ML (pin 6) is used to latch in the program data. Table III lists the selectable special functions.

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	res	res	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DEM	MUT
MODE3	res	res	res	res	res	A1	A0	IZD	SF1	SF0	DSR1	DSR0	SYS	ATC	LRP	I²S

PROGRAM REGISTER BIT MAPPING

PCM1721's special functions are controlled using four program registers which are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table IV shows the complete mapping of the four registers and Figure 7 illustrates the serial interface timing.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	AL (7:0) LDL A (1:0) Res	DAC Attenuation Data for Lch Attenuation Data Load Control for Lch Register Address Reserved
Register 1	AR (7:0) LDL A (1:0) Res	DAC Attentuation Data for Rch Attenuation Data Load Control for Rch Register Address Reserved
Register 2	MUT DEM OPE IW (1:0) PL (3:0) A (1:0) res	Left and Right DACs Soft Mute Control De-emphasis Control Left and Right DACs Operation Control Input Audio Data Bit Select Output Mode Select Register Address Reserved
Register 3	I²S LRP ATC SYS DSR (1:0) SF (1:0) IZD A (1:0) Res	Audio Data Format Select Polarity of LRCIN (pin 7) Select Attenuator Control System Clock Select Double Sampling Rate Select Sampling Rate Select Infinite Zero Detection Circuit Control Register Address Reserved

TABLE IV. Internal Register Mapping.

REGISTER 0 (A1 = 0, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

ATT = [20 log10 (ATT_DATA/255)] dB

ATTENUATION DATA LOAD CONTROL, LCH

Bit 8 (LDL) is used to simultaneously set analog outputs of Lch and Rch. An output level is controlled by AL[0:7] attenuation data when this bit is set to 1. When set to 0, an output level is not controlled and remains at the previous attenuation level. A LDR bit in Register 1 has an equivalent function as the LDL. When one of LDL or LDR is set to 1, the output level of the left and right channel is simultaneously controlled. The attenuation level is given by:

ATT = 20 log (y/256) (dB), where y = x, when $0 \le x \le 254$

y = x + 1, when x = 255

X is the user-determined step number, an integer value between 0 and 255.

Example:

let x = 255

$$\mathrm{ATT} = 20\log\left(\frac{255+1}{256}\right) = 0\mathrm{dB}$$

let x = 254

$$\mathrm{ATT} = 20\log\left(\frac{254}{256}\right) = -0.068\mathrm{dB}$$

let x = 1

$$\mathrm{ATT} = 20\log\left(\frac{1}{256}\right) = -48.16\mathrm{dB}$$

let x = 0

$$\mathrm{ATT} = 20\log\left(\frac{0}{256}\right) = -\infty$$

REGISTER 1 (A1 = 0, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

REGISTER 2 (A1 = 1, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	PL3	PL2	PL1	PL0	IW1	IW0	OPE	DEM	MUTE

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and output format. Bit 0 is used for soft mute: a “HIGH” level on bit 0 will cause the output to be muted (this is ramped down in the digital domain, so no “click” is audible). Bit 1 is used to control de-emphasis. A “LOW” level on bit 1 disables de-emphasis, while a “HIGH” level enables de-emphasis.

Bit 2, (OPE) is used for operational control. Table V illustrates the features controlled by OPE.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
OPE = 1	Zero	Forced to BPZ(1)	Enabled
	Other	Forced to BPZ(1)	Enabled
OPE = 0	Zero	Controlled by IZD	Enabled
	Other	Normal	Enabled

TABLE V. Operation Enable (OPE) Function.

OPE controls the operation of the DAC: when OPE is “LOW”, the DAC will convert all non-zero input data. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be forced to zero only if IZD is “HIGH”. When OPE is “HIGH”, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

	DATA INPUT	DAC OUTPUT
IZD = 1	Zero	Forced to BPZ(1)
	Other	Normal
IZD = 0	Zero	Zero(2)
	Other	Normal

TABLE VI. Infinite Zero Detection (IZD) Function.

	DATA INPUT	DAC OUTPUT	SOFTWARE MODE INPUT
RSTB = “HIGH”	Zero	Controlled by OPE and IZD	Enabled
	Other	Controlled by OPE and IZD	Enabled
RSTB = “LOW”	Zero	Forced to BPZ(1)	Disabled
	Other	Forced to BPZ(1)	Disabled

TABLE VII. Reset (RSTB) Function.

NOTE: (1) $\Delta\Sigma$ is disconnected from output amplifier. (2) $\Delta\Sigma$ is connected to output amplifier.

Bits 3 (IW0) and 4 (IW1) are used to determine input word resolution. PCM1721 can be set up for input word resolutions of 16, 20, or 24 bits:

Bit 4 (IW1)	Bit 3 (IW0)	Input Resolution
0	0	16-bit Data Word
0	1	20-bit Data Word
1	0	24-bit Data Word
0	0	Reserved

Bits 5, 6, 7, and 8 (PL0:3) are used to control output format. The output of PCM1721 can be programmed for 16 different states, as shown in Table VIII.

PL0	PL1	PL2	PL3	Lch OUTPUT	Rch OUTPUT	NOTE
0	0	0	0	MUTE	MUTE	MUTE
0	0	0	1	MUTE	R	
0	0	1	0	MUTE	L	
0	0	1	1	MUTE	(L + R)/2	
0	1	0	0	R	MUTE	
0	1	0	1	R	R	
0	1	1	0	R	L	REVERSE
0	1	1	1	R	(L + R)/2	
1	0	0	0	L	MUTE	
1	0	0	1	L	R	STEREO
1	0	1	0	L	L	
1	0	1	1	L	(L + R)/2	
1	1	0	0	(L + R)/2	MUTE	
1	1	0	1	(L + R)/2	R	
1	1	1	0	(L + R)/2	L	
1	1	1	1	(L + R)/2	(L + R)/2	MONO

TABLE VIII. Programmable Output Format.

REGISTER 3 (A1 = 1, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	IZD	SF1	SF0	DSR1	DSR0	SYS	ATC	LRP	I^2S

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency and infinite zero detection.

Bits 0 (I^2S) and 1 (LRP) are used to control the input data format. A “LOW” on bit 0 sets the format to “Normal” (MSB-first, right-justified Japanese format) and a “HIGH” sets the format to I^2S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is “LOW”, left channel data is assumed when LRCIN is in a “HIGH” phase and right channel data is assumed when LRCIN is in a “LOW” phase. When bit 1 is “HIGH”, the polarity assumption is reversed.

Bit 2 (ATC) is used for controlling the attenuator. When bit 2 is “HIGH”, the attenuation data loaded in program Register 0 is used for both left and right channels. When bit 2 is “LOW”, the attenuation data for each register is applied separately to left and right channels.

Bit 3 (SYS) is the system clock selection. When bit 3 is “LOW”, the system clock frequency is set to $384f_S$. When bit 3 is “HIGH”, the system clock frequency is set to $256f_S$.

Bits 4 (DSR0) and 5 (DSR1) are used to control multiples of the sampling rate:

DSR1	DSR0	Multiple	
0	0	Normal	32/44.1/48kHz
0	1	Double	64/88.2/96kHz
1	0	One-half	16/22.05/24kHz
1	1	Reserved	Not Defined

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency:

SF1	SF0	Sampling Frequency	
0	0	44.1kHz group	22.05/44.1/88.2kHz
0	1	48kHz group	24/48/96kHz
1	0	32kHz group	16/32/64kHz
1	1	Reserved	Not Defined

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is "LOW", the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is "HIGH", the zero detect feature is enabled. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be immediately forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1721 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

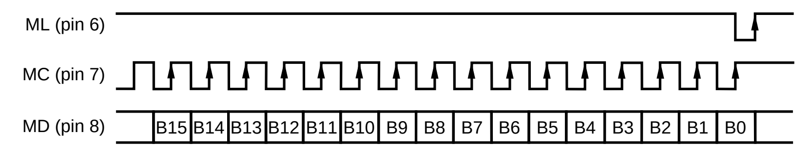
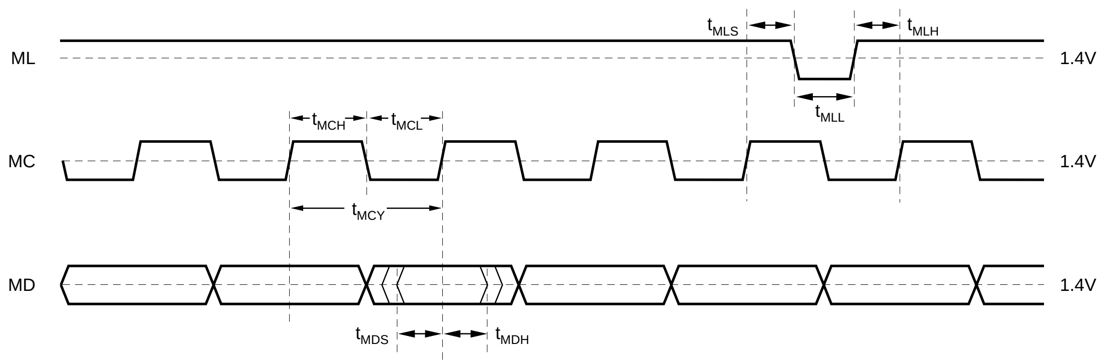


FIGURE 7. Serial Interface Timing.



MC Pulse Cycle Time	: t_{MCY}	: 100ns (min)
MC Pulse Width LOW	: t_{MCL}	: 50ns (min)
MC Pulse Width HIGH	: t_{MCH}	: 50ns (min)
MD Set-up Time	: t_{MDS}	: 30ns (min)
MC Hold Time	: t_{MDH}	: 30ns (min)
ML Low Level Time	: t_{MLL}	: 30ns + 1SYSCLK (min)
ML Set-up Time	: t_{MLS}	: 30ns (min)
ML Hold Time	: t_{MLH}	: 30ns (min)

FIGURE 8. Program Register Input Timing.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1721:

$$T_D = 11.125 \times 1/f_S$$

For f_S = 44.1kHz, T_D = 11.125/44.1kHz = 251.4µs

Applications using data from a disc or tape source, such as CD audio, CD-Interactive, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1721 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 24kHz is shown in Figure 9. The higher frequency rolloff of the filter is shown in Figure 10. If the user's application has the PCM1721 driving a wideband amplifier, it is recommended to use an external low pass filter. A simple 3rd-order filter is shown in Figure 11. For some applications, a passive RC filter or 2nd-order filter may be adequate.

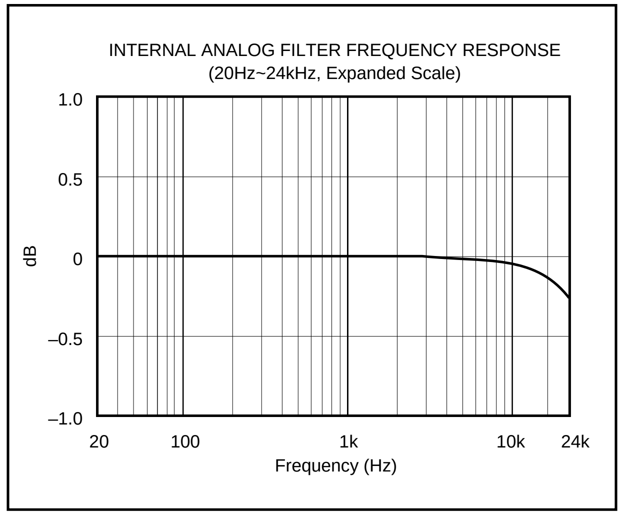


FIGURE 9. Low Pass Filter Frequency Response.

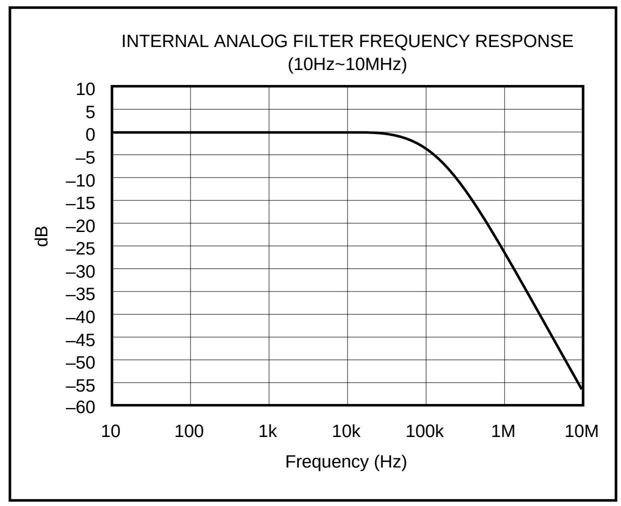


FIGURE 10. Low Pass Filter Wideband Frequency Response.

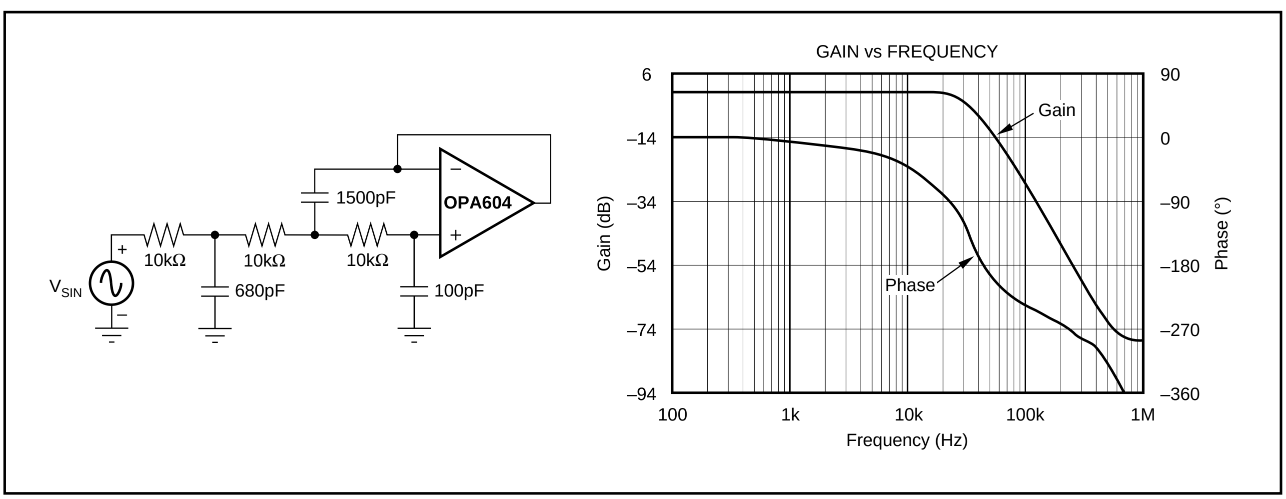


FIGURE 11. 3rd-Order LPF.

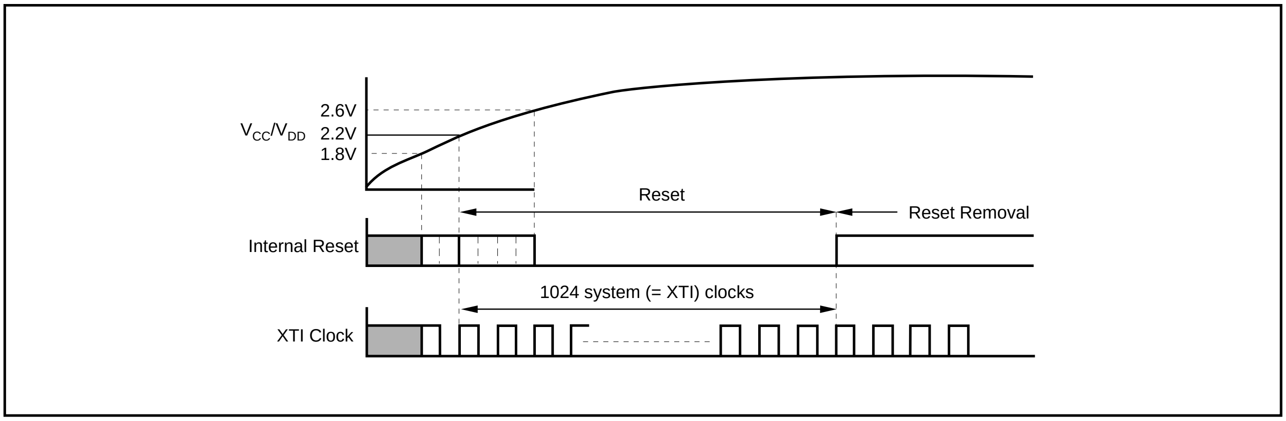


FIGURE 12. Internal Power-On Reset Timing.

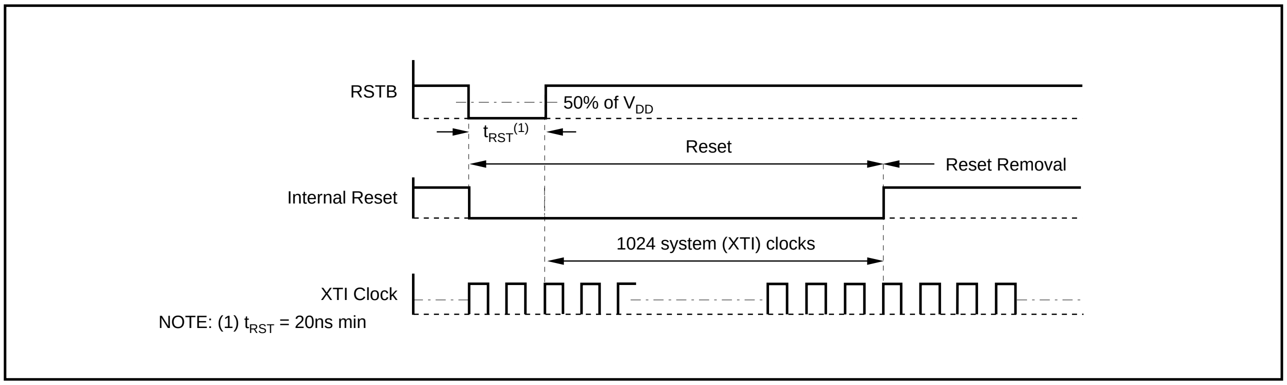


FIGURE 13. RSTB-Pin Reset Timing.

Reset

PCM1721 has both internal power-on reset circuit and the RSTB pin (pin 9) which accepts an external forced reset by RSTB = LOW. For internal power on reset, initialize (reset) is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 12 illustrates the timing of internal power on reset.

PCM1721 accepts an external forced reset when RSTB = L. During RSTB = L, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialize (1024 system clocks count after RSTB = H.) Figure 13 illustrates the timing of RSTB pin reset.

POWER SUPPLY CONNECTIONS

PCM1721 has three power supply connections: digital (V_{DD}), analog (V_{CC}), and PLL (V_{CP}). Each connection also has a separate ground return pin. It is acceptable to use a common +5V power supply for all three power pins. If separate supplies are used without a common connection, the delta between the supplies during ramp-up time must be less than 0.6V. An application circuit to avoid a power-on latch-up condition is shown in Figure 14.

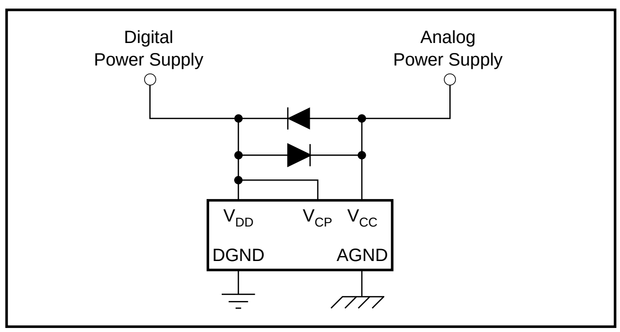


FIGURE 14. Latch-up Prevention Circuit.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 17 for optimal values of bypass capacitors. Its is also recommended to include a 0.1µF ceramic capacitor in parallel with the 10µF tantalum capacitor.

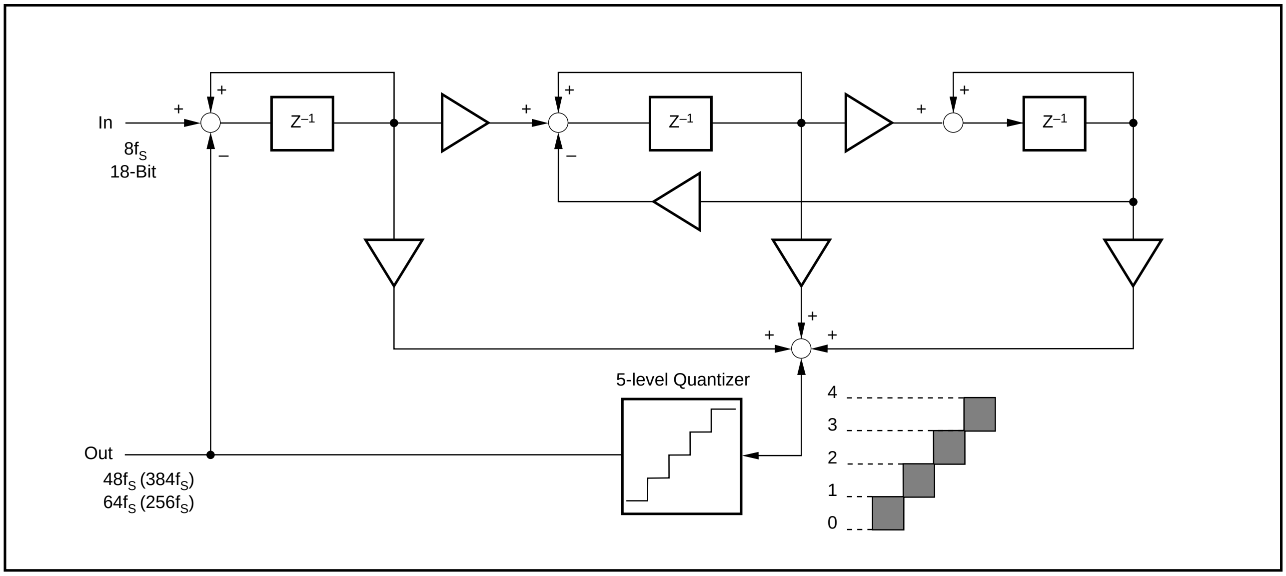


FIGURE 15. 5-Level ΔΣ Modulator Block Diagram.

THEORY OF OPERATION

The delta-sigma section of PCM1721 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format.

A block diagram of the 5-level delta-sigma modulator is shown in Figure 15. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $48f_S$ for a $384f_S$ system clock, and $64f_S$ for a $256f_S$ system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 16.

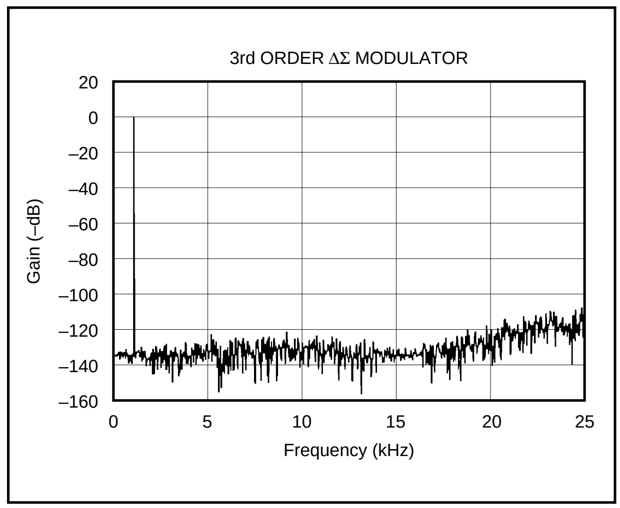


FIGURE 16. Quantization Noise Spectrum.

AC-3 APPLICATION CIRCUIT

A typical application for PCM1721 is AC-3 5.1 channel audio decoding and playback. This circuit uses PCM1721 to develop the audio system clock from the 27MHz video clock, with the SCKO pin used to drive the AC-3 decoder and two PCM1720 units, the non-PLL version of PCM1721.

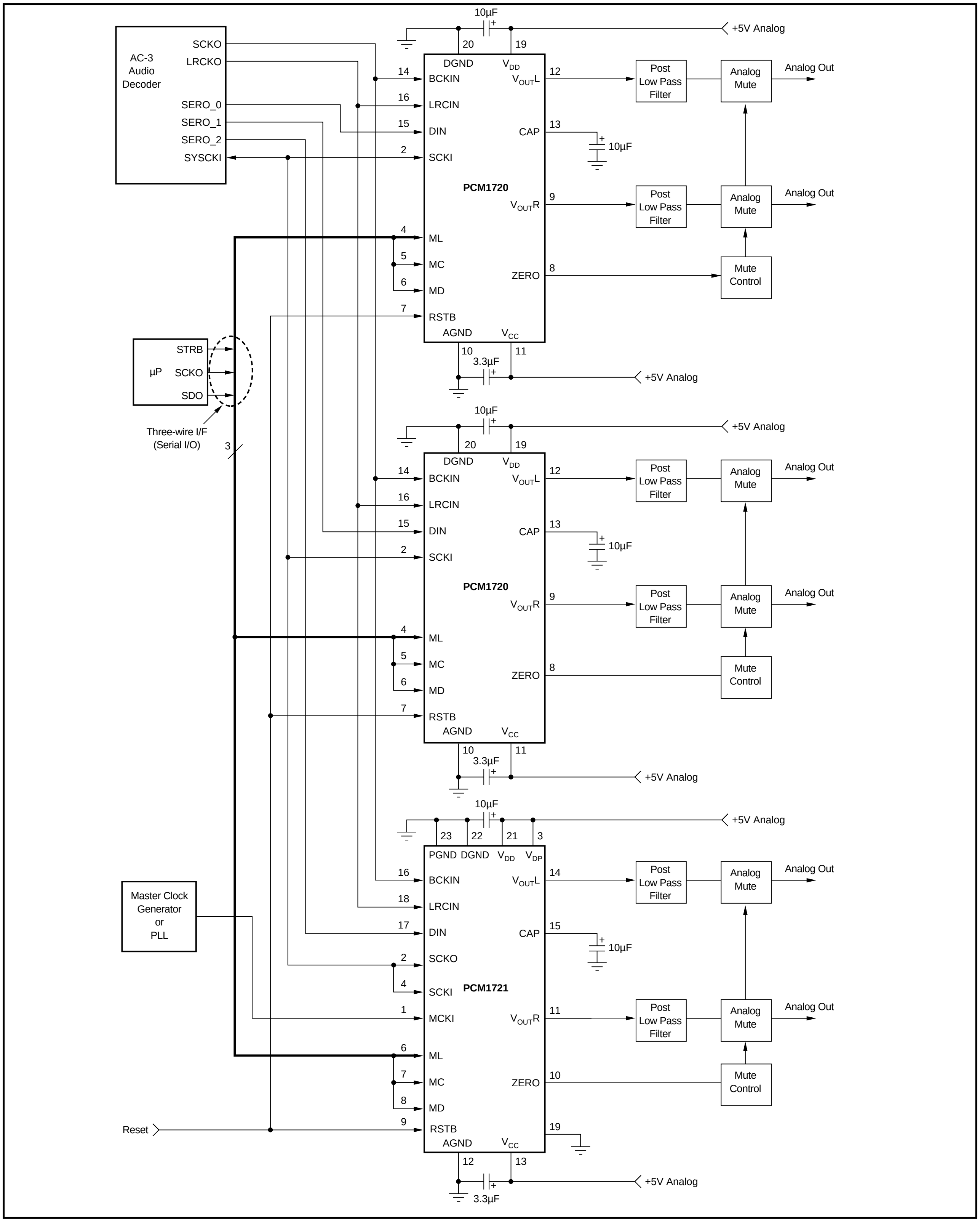


FIGURE 17. Connection Diagram for a 6-Channel AC-3 Application.