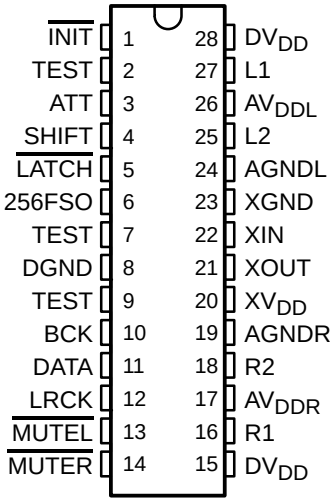
SLAS077D – SEPTEMBER 1993 – REVISED NOVEMBER 1995

- **Single 5-V Power Supply**
- **Sample Rates (F_S) up to 48 kHz**
- **18-Bit Resolution**
- **Pulse-Width-Modulation (PWM) Output**
- **Deemphasis Filter for Sample Rates of 32, 37.8, 44.1, and 48 kHz**
- **Mute With Zero-Data-Detect Flags**
- **Digital Attenuation to –60 dB**
- **Total Harmonic Distortion of 0.004% Maximum**
- **Total-Channel Dynamic Range of 96 dB Minimum**
- **Serial-Port Interface**
- **Differential Architecture**
- **CMOS Technology**
- **2s-Complement Data Format**

DWB PACKAGE
(TOP VIEW)



description

The TMS57014A is a stereo oversampled-sigma-delta digital-to-analog converter (DAC) designed for use in systems such as compact disks, digital audio tapes, multimedia, and video cassette recorders. The device provides high-resolution signal conversion. This device consists of two identical synchronous conversion paths for left and right audio channels. Other overhead functions provide on-chip timing and control.

Additional features include muting, attenuation, deemphasis, and zero-data detection. Control words (16-bit) from a host controller or processor implement these functions.

The TMS57014A is characterized for operation from 0°C to 70°C.

AVAILABLE OPTION†

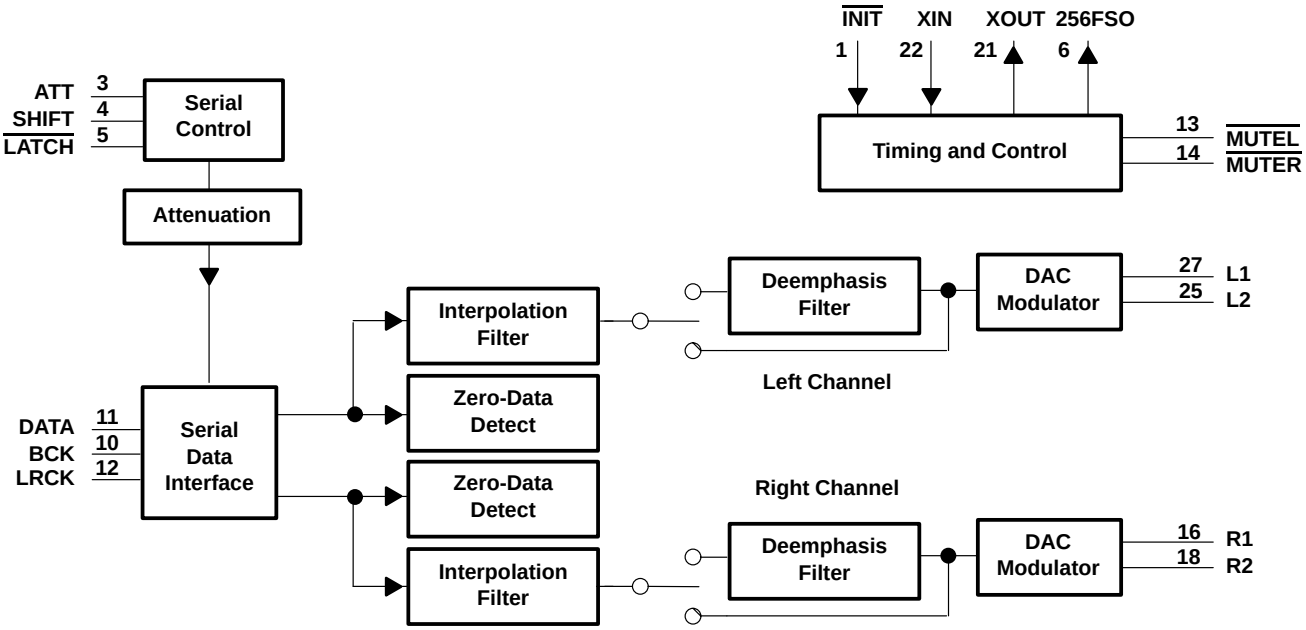
T_A	PACKAGE
	SMALL OUTLINE (DWB)
0°C to 70°C	TMS57014ADWBLE

† Available on tape and reel (LE) only.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



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Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ATT	3	I	Serial control data. ATT is a 16-bit word configured as LSB first (see Tables 2, 3, and 4).
AV_{DDL}	26	I	Analog power supply (left channel)
AV_{DDR}	17	I	Analog power supply (right channel)
AGNDL	24	I	Analog ground (left channel)
AGNDR	19	I	Analog ground (right channel)
BCK	10	I	Bit clock input. BCK clocks serial audio data into the device.
DATA	11	I	Audio data input. DATA can be configured as 16 or 18 bits with MSB or LSB first. DATA is 2s complement.
DV_{DD}	15, 28	I	Digital supply
DGND	8	I	Digital ground
$\overline{\text{INIT}}$	1	I	Reset. When $\overline{\text{INIT}}$ is brought low, the device is reset. The device is activated on the rising edge of $\overline{\text{INIT}}$. The LRCK signal must be applied to the device for a reset to occur.
$\overline{\text{LATCH}}$	5	I	Serial-control data latch. Control data loads into the internal registers when $\overline{\text{LATCH}}$ is brought low.
LRCK	12	I	Left/right clock. LRCK signifies whether the serial data is associated with the left-channel DAC (when high) or the right-channel DAC (when low).
$\overline{\text{MUTEL}}$	13	O	Left-channel mute flag active. When the left channel is mute or the data through the channel remains at zero for the system-register selected time, $\overline{\text{MUTEL}}$ is brought low.
$\overline{\text{MUTER}}$	14	O	Right-channel mute flag active. When the right channel is mute or the data through the channel remains at zero for the system-register selected time, $\overline{\text{MUTER}}$ is brought low.
L1	27	O	Left PWM output 1
L2	25	O	Left PWM output 2
R1	16	O	Right PWM output 1
R2	18	O	Right PWM output 2
SHIFT	4	I	Shift clock. SHIFT clocks the control data into the internal registers.
TEST	2, 7, 9	I	All TEST inputs should be tied low.
XIN	22	I	Master clock in. XIN derives all the key logic signals of the device. XIN runs at 512 F_S, where F_S is the sample rate.
XOUT	21	O	Master clock out
XV_{DD}	20	I	Power supply for clock section
XGND	23	I	Ground for clock section
256FSO	6	O	System clock out. 256FSO reflects the master clock input divided by 2. The rate is 256Fs, where F_S is the sample rate.

detailed description

The TMS57014A incorporates an interpolation impulse-response filter (FIR) and oversampled modulator. The pulse-width modulation (PWM) digital output feeds into an external low-pass filter to recover the analog audio signal.

Two control registers configure the device, the attenuation register controls the attenuation range and the system register controls additional functions (see register set section).

reset/initialization

When $\overline{\text{INIT}}$ is brought low, an internal reset signal becomes active approximately 120 cycles of the sampling frequency (F_S) after the falling edge of $\overline{\text{INIT}}$. Under this condition, all internal circuits are initialized and the PWM output is held at zero data (50% duty cycle). When $\overline{\text{INIT}}$ is brought high, the internal reset signal goes inactive for a maximum of five LRCK periods after the rising edge of $\overline{\text{INIT}}$. At this point, internal clocks are synchronous with LRCK and the PWM output is valid (see Figure 1). The LRCK signal must be applied for proper initialization.

reset/initialization (continued)

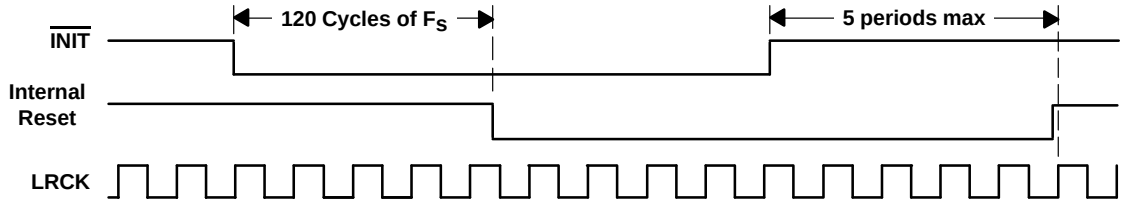

Figure 1. Reset Timing Relationships

timing and control

The timing and control circuit generates and distributes necessary clocks throughout this design. XIN is the external master clock input. The sample rate of the data paths is set as LRCK = XIN/512. With a fixed oversampling ratio of 32x and each PWM output value requiring 16 XIN cycles, the effect of changing XIN is shown in Table 1.

The DAC can be operated at any conversion rate between 48 kHz and 32 kHz by choosing the appropriate master-clock frequency. Some of the functions of the converter, such as the deemphasis filter, operate only at the frequencies in Table 1.

Table 1. Master Clock to Sample Rate Comparison

XIN (MHz)	256FSO (MHz)	LRCK (kHz)
24.5760	12.2880	48.0
22.5792	11.2896	44.1
19.3536	9.6768	37.8
16.3840	8.1920	32.0

digital-audio data interface

The conversion cycle is synchronized to the rising edge of LRCK, and the data must meet the setup requirements specified in the timing requirements table. The input data is 16 or 18 bits with the MSB or LSB first as selected in the system register. The BCK frequency must be equal to or greater than 32 F_S for 16-bit data or 36 F_S for 18-bit data where F_S is the sample rate. Figure 2 illustrates the input timing.

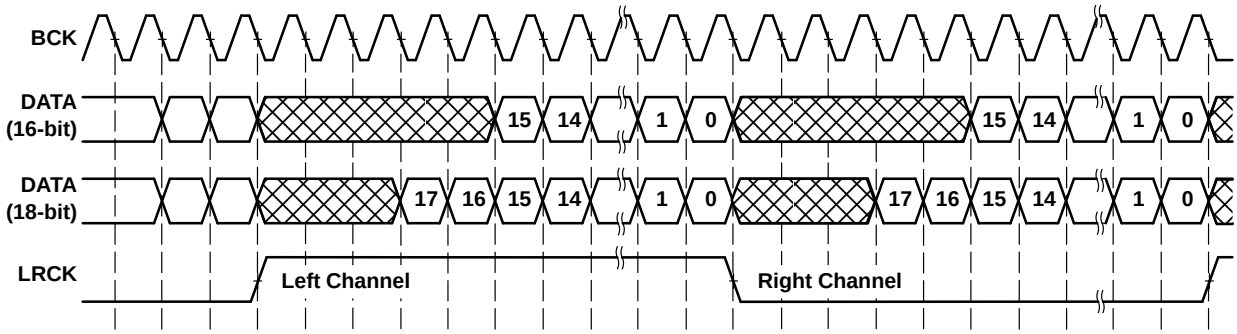

Figure 2. Audio-Data Input Timing

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serial-control interface

This device uses the least-significant-bit-first format. Therefore, for a 16-bit word, D15 is the most significant bit and D0 is the least significant bit. Unless otherwise specified, all values are in 2s-complement format.

serial-control-data input

The 16-bit control-data input implements the device-control functions. The TMS57014A has two registers for this data: the system register and the attenuation register. The system register contains most of the system configuration information, and the attenuation register controls audio output level, deemphasis, and mute. Figure 3 illustrates the input timing for ATT, SHIFT, and $\overline{\text{LATCH}}$. The data loads internally on the falling edge of $\overline{\text{LATCH}}$. The shift clock should be high for the $\overline{\text{LATCH}}$ setup time before $\overline{\text{LATCH}}$ goes low.

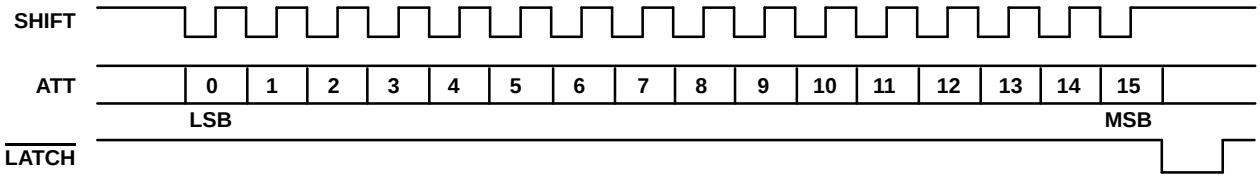

Figure 3. Control-Data-Input Timing

mute

When mute is activated, the output PWM becomes zero data (50% duty cycle). The two mute flags, $\overline{\text{MUTEL}}$ and $\overline{\text{MUTER}}$, are independently set low based on the data in the respective channel being zero. This function becomes active under the following conditions:

1. When the zero-data detector detects that the input data has been zero for 2500 cycles of F_S or 12500 cycles of F_S (as selected in the control registers), output is 50% duty cycle.
2. When the MUTE register value is set high by means of the serial-control data.
3. When $\overline{\text{INIT}}$ is active (low), output is 50% duty cycle.

zero-data detect

After the input data remains zero for 2500 or 12500 cycles of F_S as set by the system register (D4, D5), the channel-mute flag becomes active. Zero-data detection is available for both channels independently, so the two outputs ($\overline{\text{MUTER}}$ and $\overline{\text{MUTEL}}$) indicate that zero data has been detected on the respective channel. The zero-detect register value in the serial-control data selects the detection period. The mute flag returns high immediately when nonzero input data is received.

deemphasis filter

Four sets of deemphasis-filter coefficients support four sampling rates (F_S): 32, 37.8, 44.1, and 48 kHz. Internal register values select the filter coefficients. The internal register values enable or disable the filter. Figure 4 illustrates the deemphasis characteristics.

Many audio sources have been recorded with preemphasis characteristics that are the inverse of the deemphasis characteristics shown in Figure 4. This device provides reconstruction of the original frequency response.

deemphasis filter (continued)

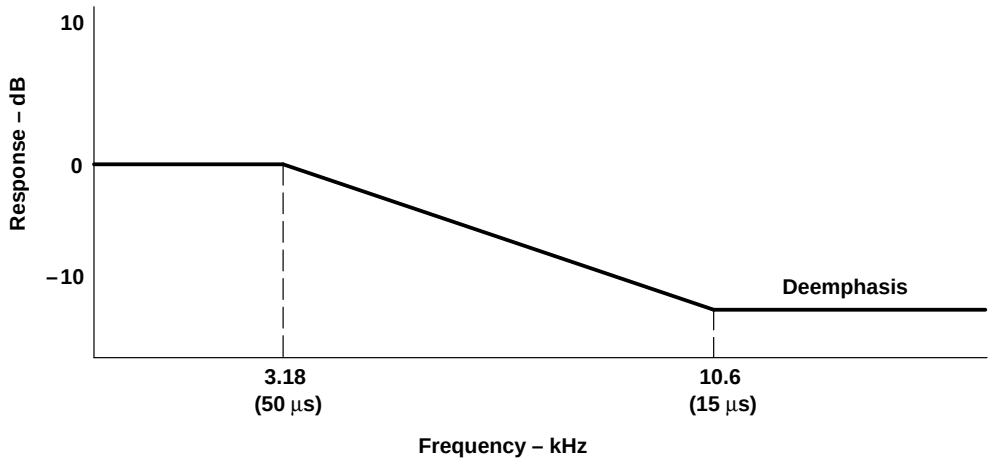

Figure 4. Deemphasis Characteristics

digital attenuation

A value selected in the internal attenuation register determines the attenuation of the digital-audio-data input. The attenuation value is 11 bits long with a valid range of hex values from 400h to 000h. A data value of 001h corresponds to an attenuation value of –60 dB and a data value of 400h corresponds to 0 dB. The attenuation function is nonlinear (see equation 1). Figure 5 illustrates the attenuation function in dB. The default attenuation value is 400h.

$$\text{Attenuation} = 20 \log \left(\frac{\text{attenuation data}}{1024} \right) \quad (1)$$

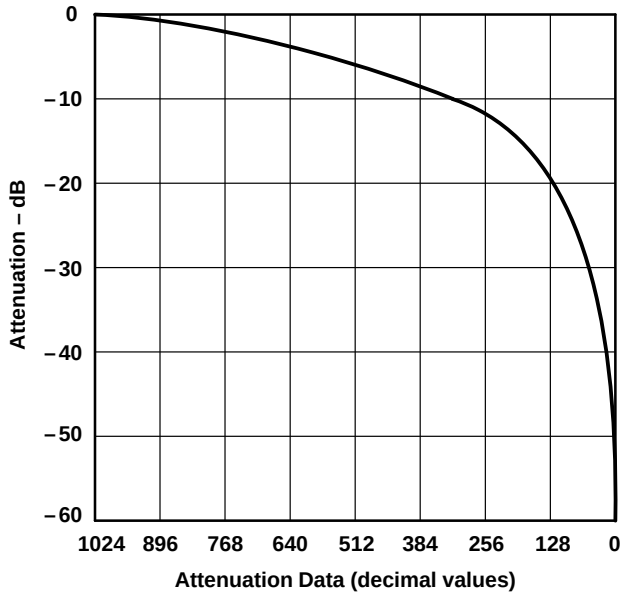

Figure 5. Digital Attenuation Characteristics

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register set

Table 2 contains the register-set selection. Tables 3 and 4 list the bit functions.

Table 2. Register-Set Selection

BITS		DESCRIPTION
15	14	
0	0	Attenuation register
0	1	System register
1	x	Invalid condition†

† Bit 15 should always be set to 0 when writing data for proper operation.

Table 3. Attenuation-Register Bit Functions

BITS‡				FUNCTION
13	12	11	10 – 0	
0	—	—	—	Deemphasis off
1	—	—	—	Deemphasis on
—	0	—	—	Channel mute off
—	1	—	—	Channel mute on
—	—	0	—	Bit 11 must be low
—	—	—	0	Digital attenuation, mute
—	—	—	1	Digital attenuation, –60.2 dB§
—	—	—	2	Digital attenuation, –54.2 dB§
—	—	—	3	Digital attenuation, –50.7 dB§
—	—	—	. . .	
—	—	—	1FF	Digital attenuation, –6.04 dB§
—	—	—	200	Digital attenuation, –6.02 dB§
—	—	—	201	Digital attenuation, –6.00 dB§
—	—	—	. . .	
—	—	—	3FF	Digital attenuation, –0.01 dB§
—	—	—	400	Digital attenuation, 0.00 dB§

‡ Default value = 0400h

§ The attenuation values shown are typical values. Refer to the digital attenuation section for a description of the attenuation function.

Table 4. System-Register Bit Functions

BITS†								FUNCTION
13	12	11–6	5	4	3–2	1	0	
0	—	—	—	—	—	—	—	MSB first, audio data
1	—	—	—	—	—	—	—	LSB first, audio data
—	0	—	—	—	—	—	—	16-bit, audio data
—	1	—	—	—	—	—	—	18-bit, audio data
—	—	0	—	—	—	—	—	Bits 11–6 must be low
—	—	—	0	—	—	—	—	Zero data detect period (2500 cycles of F_{sy})
—	—	—	1	—	—	—	—	Zero data detect period (12500 cycles of F_{sy})
—	—	—	—	0	—	—	—	Bit 4 must be low
—	—	—	—	—	0	—	—	Deemphasis – 44.1 kHz
—	—	—	—	—	1	—	—	Deemphasis – 48.0 kHz
—	—	—	—	—	2	—	—	Deemphasis – 37.8 kHz
—	—	—	—	—	3	—	—	Deemphasis – 32.0 kHz
—	—	—	—	—	—	0	—	LRCK and PWM are not synchronized
—	—	—	—	—	—	1	—	LRCK and PWM synchronized
—	—	—	—	—	—	—	0	Bit 0 must be low

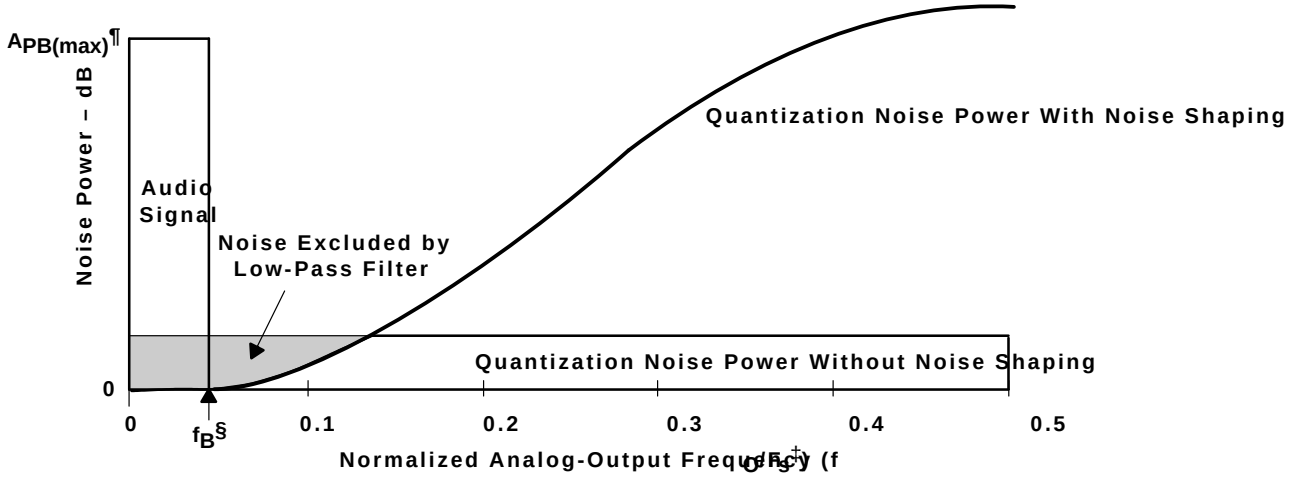
† Default value = 0000h

interpolation filter

The interpolation filter used prior to the DAC increases the digital-data rate from the LRC oversampled rate by interpolating with a ratio of 1:32. The oversampling modulator receives t filter with deemphasis as an option.

DAC modulator

The DAC is a third-order modulator with 32 times oversampling. The DAC provides high-resolu performance using a 15-value PWM output as shown in Figure 6.



‡ f_O is the output frequency at the low-pass filter shown in Figure 7.
§ f_B is the highest frequency of interest within the baseband.
¶ $A_{PB(max)}$ is the passband maximum amplitude.

Figure 6. Oversampling Noise Power With and Without Noise Shaping

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PWM output (L2 – L1 and R2 – R1)

The L2 – L1 and the R2 – R1 output pairs are PWM signals with the L2 – L1 differential pulse duration determining the left-channel analog voltage and the R2 – R1 differential pulse duration determining the right-channel analog voltage.

Each DAC left and right output consists of 15 levels of PWM and provides a differential signal as the input to two external differential amplifiers configured as a low-pass filter to produce the left and right audio outputs (see Figure 7).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Analog supply voltage range, left and right, AV_{DDL}, AV_{DDR} (see Note 1) . . . . . –0.3 V to 7 V
Digital supply voltage range, DV_{DD} (see Note 2) . . . . . –0.3 V to 7 V
Clock supply voltage range, XV_{DD} (see Note 3) . . . . . –0.3 V to 7 V
Output voltage range, V_O: L1, L2 . . . . . –0.3 V to AV_{DDL} + 0.3 V
R1, R2 . . . . . –0.3 V to AV_{DDR} + 0.3 V
Input voltage range, V_I . . . . . –0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Case temperature for 10 seconds, T_C . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values for maximum ratings are with respect to AGNDL and AGNDR respectively.
2. Voltage values for maximum ratings are with respect to DGND.
3. Voltage values for maximum ratings are with respect to XGND.

recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
Analog supply voltage, left and right, AV_{DDL}, AV_{DDR}		4.75	5	5.25	V
Digital supply voltage, DV_{DD}		4.75	5	5.25	V
Clock supply voltage, XV_{DD}		4.75	5	5.25	V
High-level input voltage, V_{IH}	XIN	0.9 V_{DD}			V
	All other digital inputs	0.76 V_{DD}			
Low-level input voltage, V_{IL}	XIN			0.1 V_{DD}	V
	All other digital inputs			0.24 V_{DD}	
Load resistance at PWM, R_L			10		kΩ
Master clock frequency at XIN		16.3		24.6	MHz
Operating free-air temperature, T_A		0		70	°C

NOTE 4: DV_{DD}, AV_{DDL}, XV_{DD} and AV_{DDR} tied together represents V_{DD}.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

digital interface, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$ (see Note 4)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	256FSO	$I_O = -0.4$ mA	$V_{DD}-0.5$			V
		L1, L2, R1, R2	$I_O = -12$ mA	$V_{DD}-0.5$			
		XOUT	$I_O = -1.2$ mA	$V_{DD}-0.5$			
		$\overline{MUTEL}$, $\overline{MUTER}$	$I_O = -1$ mA	$V_{DD}-0.5$			
V_{OL}	Low-level output voltage	256FSO	$I_O = 0.4$ mA			0.4	V
		L1, L2, R1, R2	$I_O = 12$ mA			0.5	
		XOUT	$I_O = 1.2$ mA			0.5	
		$\overline{MUTEL}$, $\overline{MUTER}$	$I_O = 1$ mA			0.4	
I_{IH}	High-level input current, any digital input				±1	±5	µA
I_{IL}	Low-level input current, any digital input				±1	±5	µA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All typical values are at $T_A = 25°C$.
NOTE 4: DV_{DD}, AV_{DDL}, XV_{DD} and AV_{DDR} tied together represents V_{DD}.

supplies, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, no load

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Analog power supply current	AV_{DDL} and AV_{DDR} are shorted together		15		mA
Digital power supply current			15		mA
Total device supply current over operating temperature range				60	mA
Power dissipation				350	mW

† All typical values are at $T_A = 25°C$.

DAC modulator, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, sample rate ($F_S$) = 44.1 kHz, full-scale input sine wave at 1 kHz, $T_A = 25°C$, bandwidth is 20 Hz to 20 kHz

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Resolution	See Note 5		18			bits
Signal-to-noise ratio	A-weighted, 20 Hz to 20 kHz, See Figure 10, Table 5, and Note 5	Deemphasis not selected	96	100		dB
Total harmonic distortion	20 Hz to 20 kHz, See Note 5			0.003%	0.004%	

† All typical values are at $T_A = 25°C$.
NOTE 5: These specifications are measured at the output (V_O) of the low-pass filter shown in Figure 7.

filter characteristics, $AV_{DD} = DV_{DD} = 5\ V \pm 5\%$, deemphasis disabled

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Pass-band ripple	Sample rate (F_S) = 48 kHz, See Note 5	–0.002		0.002	dB
Stop-band attenuation		75			dB
Pass band (–3 dB) (DAC)	See Note 5	0		0.46 F_S	kHz
Stop band		0.54 F_S			kHz
Group delay			29/F_S		s

† All typical values are at $T_A = 25°C$.
NOTE 5: These specifications are measured at the output (V_O) of the low-pass filter shown in Figure 7.

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timing requirements (see Figures 8 and 9 and Note 6)

		MIN	MAX	UNIT
t_{w1}	Pulse duration, BCK	160		ns
t_{su1}	Setup time, DATA before BCK↑	20		ns
t_{h1}	Hold time, DATA after BCK↑	20		ns
t_{su2}	Setup time, LRCK before BCK↑	50		ns
t_{h2}	Hold time, LRCK after BCK↑	50		ns
t_{w2}	Pulse duration, SHIFT	100		ns
t_{su3}	Setup time, ATT before SHIFT↑	20		ns
t_{h3}	Hold time, ATT after SHIFT↑	20		ns
t_{w3}	Pulse duration, $\overline{\text{LATCH}}$	100		ns
t_{su4}	Setup time, $\overline{\text{LATCH}}$ before SHIFT↑	100		ns
t_{h4}	Hold time, $\overline{\text{LATCH}}$ after SHIFT↑	t_{w2} + 20		ns

NOTE 6: All timing measurements were taken at the $V_{DD}/2$ voltage level.

PARAMETER MEASUREMENT INFORMATION

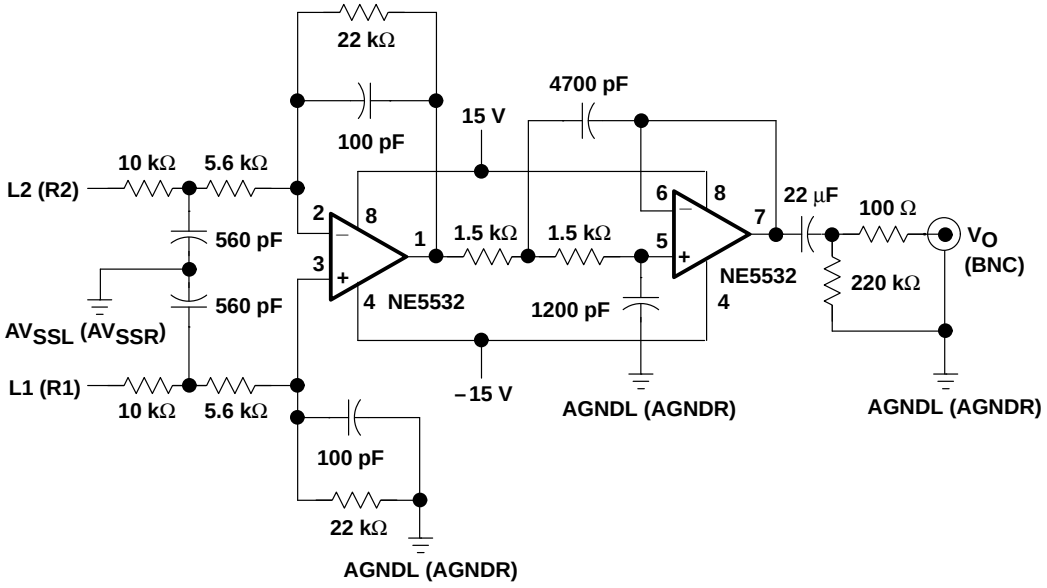

Figure 7. Analog Low-Pass Filter Recommended for Measuring the Dynamic Specifications of the TMS57014A

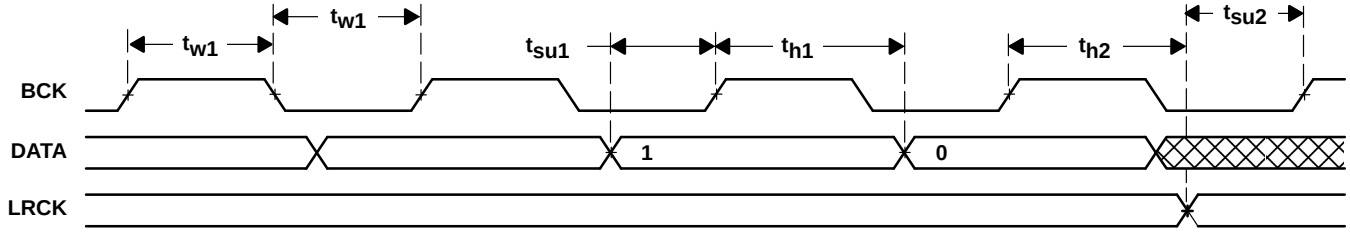

Figure 8. Audio-Data Serial Timing

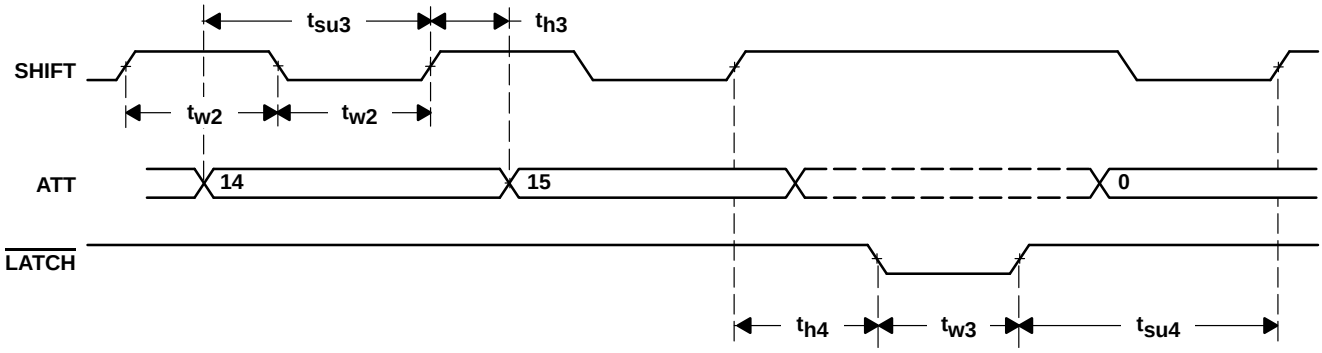

Figure 9. Control-Data Serial Timing

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PARAMETER MEASUREMENT INFORMATION

Table 5. A-Weighted Data

FREQUENCY	A WEIGHTING (dB)	FREQUENCY	A WEIGHTING (dB)
25	–44.6 ±2	800	–0.1 ±1
31.5	–39.2 ±2	1000	0 ±0
40	–34.5 ±2	1250	0.6 ±1
50	–30.2 ±2	1600	1.0 ±1
63	–26.1 ±2	2000	1.2 ±1
80	–22.3 ±2	2500	1.2 ±1
100	–19.1 ±1	3150	1.2 ±1
125	–16.1 ±1	4000	1.0 ±1
160	–13.2 ±1	5000	0.5 ±1
200	–10.8 ±1	6300	–0.1 ±1
250	–8.6 ±1	8000	–1.1 ±1
315	–6.5 ±1	10000	–2.4 ±1
400	–4.8 ±1	12500	–4.2 ±2
500	–3.2 ±1	16000	–6.5 ±2
630	–1.9 ±1		

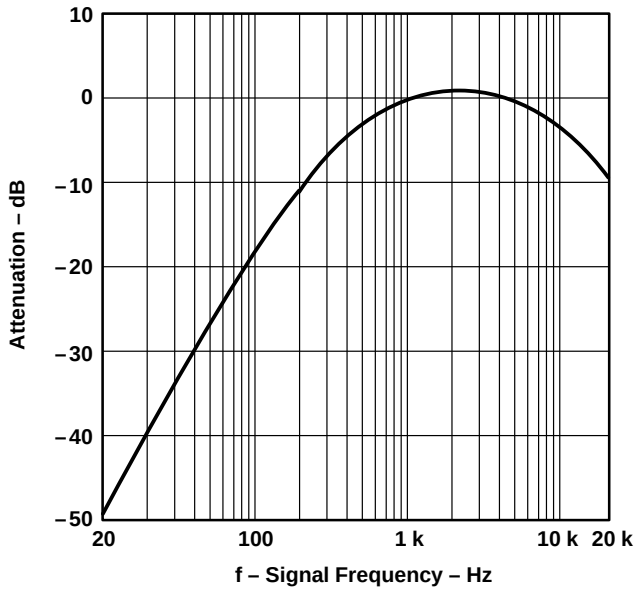


Figure 10. A-Weighted Function

APPLICATION INFORMATION

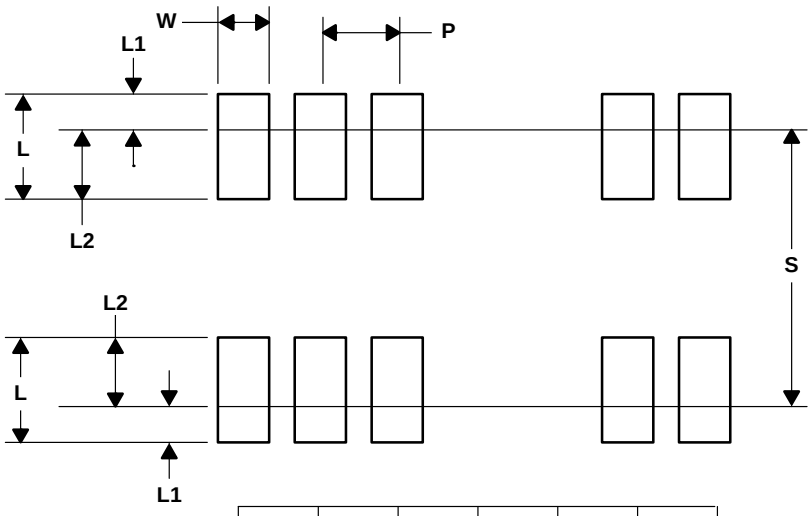
circuit and layout considerations

The designer should follow these guidelines for the best device performance.

- Separate digital and analog ground planes should be used. All digital device functions should be over the digital ground plane, and all analog device functions should be over the analog ground plane. The ground planes should be connected at only one point to the direct power supply, and this is usually at the connector edge of the board.
- A single crystal-controlled clock should synchronously generate all digital signals
- All power supply lines should include a 0.1-μF and a 1-μF capacitor. When clock noise is excessive, a toroidal inductance of 10 μH should be placed in series with XV_{DD} before connecting to DV_{DD}.
- The digital input control signals should be buffered when they are generated off the card.
- Clock jitter should be minimized, and precautions taken to prevent clock overshoot. This minimizes any high-frequency coupling to the analog output.

PCB footprint

Figure 11 shows the printed-circuit-board (PCB) land pattern for the TMS57014A small-outline package.



P	S	W	L	L1	L2
1.27	9.53	0.76	1.55	0.64	0.91

NOTE A: All linear dimensions are in millimeters.

Figure 11. Land Pattern for PCB Layout

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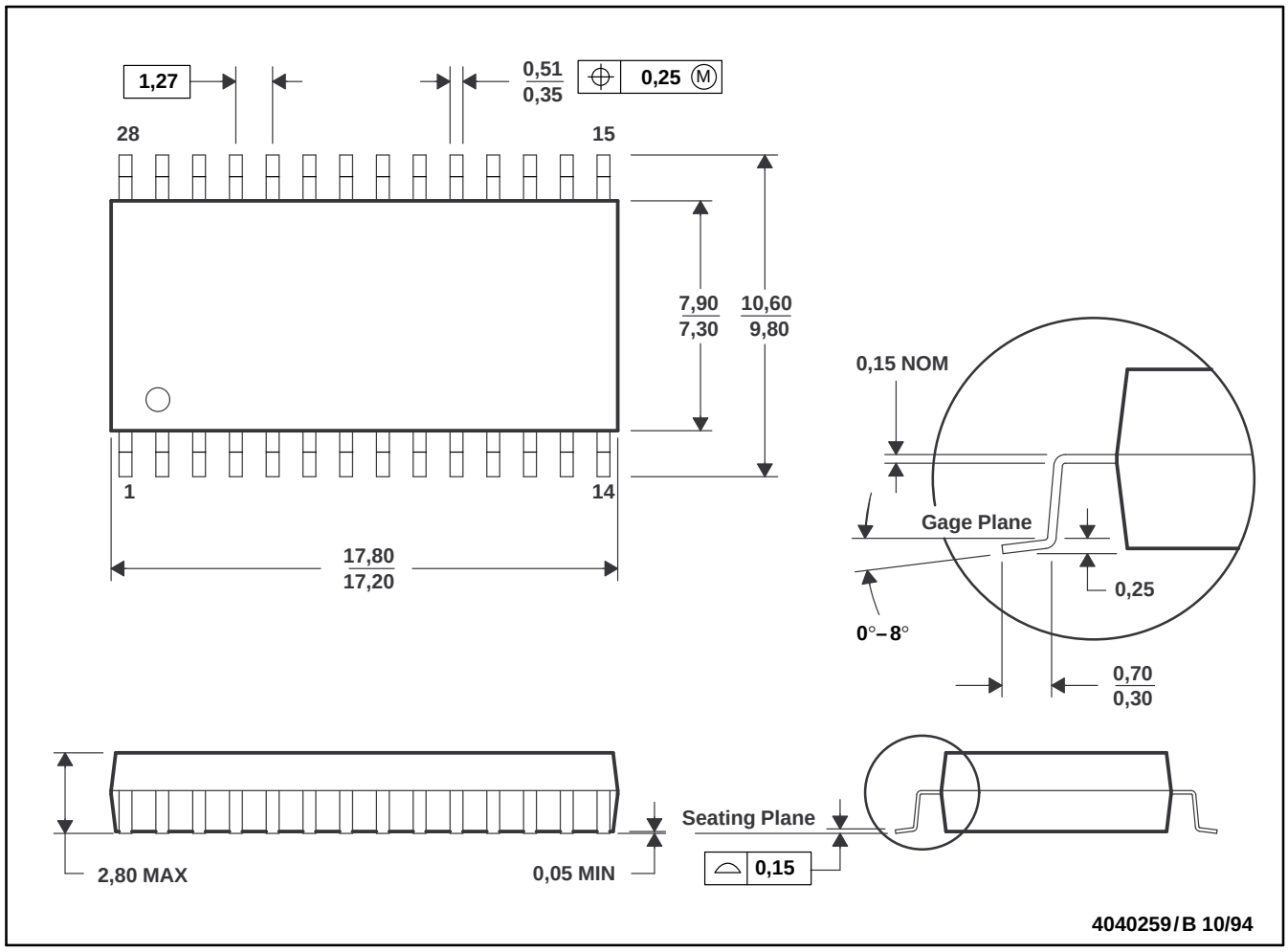
MECHANICAL DATA

DWB (R-PDSO-G28) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusion.

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