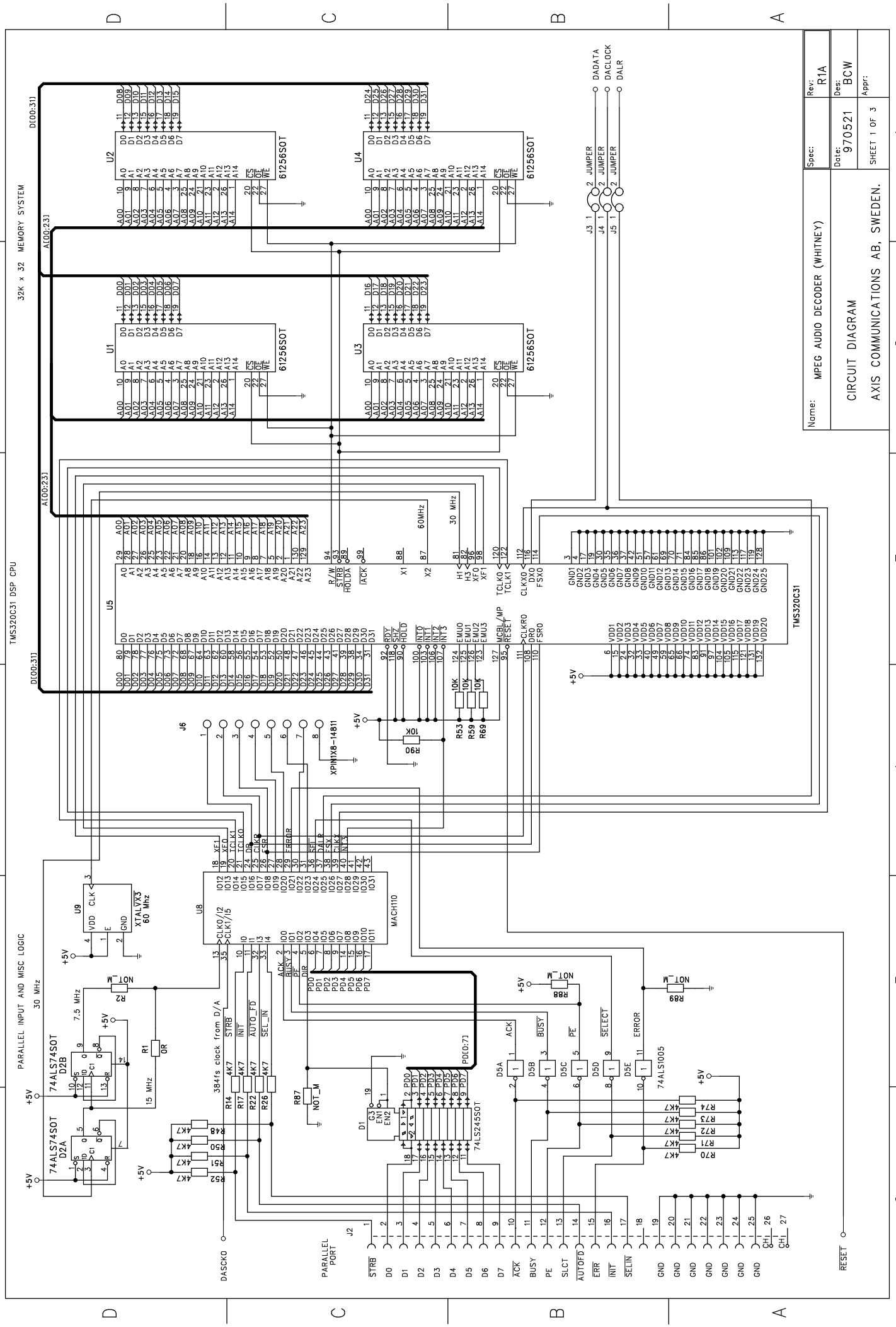
Name: MPEG AUDIO DECODER (WHITNEY)
Spec:
Rev: R1A
Date: 970521
Des: BCW
Appr:
SHEET 1 OF 3
CIRCUIT DIAGRAM
AXIS COMMUNICATIONS AB, SWEDEN.
32K x 32 MEMORY SYSTEM
TMS320C31 DSP CPU
PARALLEL INPUT AND MISC LOGIC
PARALLEL PORT
U1
U2
U3
U4
U5
U8
U9
J2
J3
J4
J5
J6
D1
D2A
D2B
R1
R2
R87
R88
R89
R90
R53
R59
R69
R70
R71
R72
R73
R74
R48
R50
R51
R52
R14
R17
R22
R26
61256SOT
TMS320C31
MACH110
74ALS74SOT
74ALS1005
74LS245SOT
XTALVX3
60 Mhz
30 MHz
7.5 MHz
15 MHz
384fs clock from D/A
DADATA
DACLOCK
DALR
JUMPER
DASCKO
RESET
STRB
D0
D1
D2
D3
D4
D5
D6
D7
ACK
BUSY
PE
SLCT
AUTOFD
ERR
INIT
SELIN
GND
+5V
NOT_M
10K
4K7
OR