XC4000XV Family
Field Programmable Gate Arrays

May 5, 1998 (Version 1.1) — Advance Product Specification

XC4000XV FPGAs

Note: This data sheet describes the XC4000XV devices. This information does not necessarily apply to the other Xilinx families: XC4000, XC4000A, XC4000D, XC4000H, or XC4000L, XC4000E, XC4000EX, XC4000XL. For information on these devices, see the Xilinx WEBLINX at http://www.xilinx.com.

- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization

XC4000XV Electrical Features

- Low-Voltage Device Functions at 2.3 - 2.7 Volts
- 5.0 V TTL compatible I/O
- 3.3 V LVTTL, LVCMOS compatible I/O
- 12-mA, 24-mA current sink capability
- 40% lower power than XC4000XL Devices

Additional XC4000XV Features

- **Advanced Technology** — 0.25 µm SRAM CMOS process
- **Proven Architecture** — Industry standard XC4000X architecture
- **Highest Performance** — Internal performance beyond 100MHz
- **Lowest Power** — 2.5 V technology plus segmented routing architecture
- **Easy to Use** — Interfaces to any combination of 3.0 V and 5.0 V TTL-compatible devices
- **Software Compatibility** — Supported by Alliance/Foundation Series Software M1.4
- **Package Compatibility** — Footprint compatible with XC4000XL devices (except for 2.5 V power pins)

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Table 1: The XC4000XV Field Programmable Gate Array

Device	Logic Cells	Max. Logic Gates (No RAM)	Max.RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	PROM Size
XC40125XV	10,982	125,000	147,968	80,000 - 250,000	68 x 68	4,624	10,336	448	2,797,040
XC40150XV	12,312	150,000	165,888	100,000 - 300,000	72 x 72	5,184	11,520	448	3,373,448
XC40200XV	16,758	200,000	225,792	130,000 - 400,000	84 x 84	7,056	15,456	448	4,551,056
XC40250XV	20,102	250,000	270,848	180,000 - 500,000	92 x 92	8,464	18,400	448	5,433,888

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM*

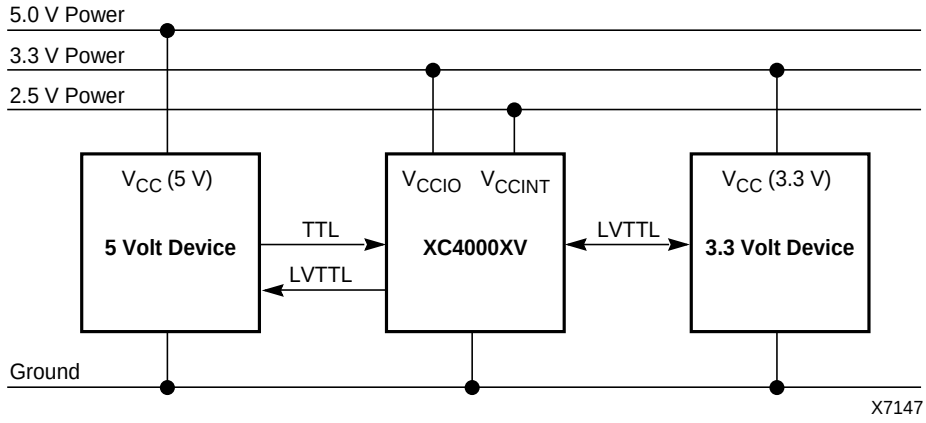
Introduction

XC4000 Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

Differences between the XC4000XV and XC4000XL FPGAs

- **VCCINT (2.5 Volt) Power Supply Pins**
  XC4000XV FPGAs are logically identical to XC4000EX and XC4000XL FPGAs. The I/O functionality is identical to XC4000XL FPGAs. The only difference between XV and XL is a separate lower core voltage of 2.5V for XV, which is named VCCINT. The pins assigned to the VCCINT supply are named in the pinout guide for the XC40125XV FPGA
- **Lower Power**
  XC4000XV devices require 40% less power than equivalent XL devices
- **Increased Drive**
  XC4000XV outputs can optionally sink 24-mA each.
- **Increased Routing**
  The XC40150XV, XC40200XV, and XC40250XV have enhanced routing. Eight routing channels of octal length have been added to each row of CLBs.



	V_{OUT}_max	V_{IH}	V_{IL}	V_{OH}	V_{OL}
TTL	5.5	2.0	0.8	2.4	0.4
LVTTL	3.6	2.0	0.8	2.4	0.4
LVCMOS	3.6	50% of VCCIO	30% of VCCIO	90% of VCCIO	10% of VCCIO

Figure 1: XV Power supply and signaling environment

XC4000XV Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns.All specifications are representative of worst- case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. For design considerations requiring more detailed timing information, see the appropriate family a.c. supplements available on the Xilinx WEBLINX at http://www.xilinx.com.

Absolute Maximum Ratings

Symbol	Description			Units
V_{CCINT}	Supply voltage relative to GND		-0.5 to 3.0	V
V_{CCIO}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CC}	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes: 1. Maximum DC overshoot or undershoot above V_{cc} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.3	2.7	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	2.3	2.7	V
V_{CCIO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~50% of V_{CC}.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DRINT}	V_{CCINT} Data Retention Supply Voltage (below which configuration data may be lost)		2.1		V
V_{DRIO}	V_{CCIO} Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			5	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

XC4000XV Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	
From pad through Global Low Skew buffer, to any clock K	T_{GLS}	XC40125XV	6.3	5.4	ns
From pad through Global Early buffer, to any IOB clock for BUFGEs # 1, 2, 5, & 6	T_{GE_1256}	XC40125XV	5.4	4.7	ns
From pad through Global Early buffer, to any IOB clock for BUFGEs # 3, 4, 7, & 8	T_{GE_3478}	XC40125XV	6.6	5.7	
			Advance		

XC4000XV CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

Description	Speed Grade Symbol	-2 Min	-2 Max	-1 Min	-1 Max	Units
Combinatorial Delays						
F/G inputs to X/Y outputs	T_{ILO}		1.4		1.2	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		2.4		2.1	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		2.1		1.8	ns
C inputs via SR/H0 via H to X/Y outputs	T_{HH0O}		2.1		1.8	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		1.9		1.7	ns
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		2.1		1.8	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CBYP}		0.8		0.7	ns
CLB Fast Carry Logic						
Operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		1.6		1.4	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		2.9		2.5	ns
Initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		1.1		0.9	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		2.5		2.2	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.3		0.2	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.4		0.25	ns
Sequential Delays						
Clock K to Flip-Flop outputs Q	T_{CKO}		1.3		1.2	ns
Clock K to Latch outputs Q	T_{CKLO}		1.3		1.2	ns
Setup Time before Clock K						
F/G inputs	T_{ICK}	1.1		0.9		ns
F/G inputs via H	T_{IHCK}	2.1		1.8		ns
C inputs via H0 through H	T_{HH0CK}	1.8		1.5		ns
C inputs via H1 through H	T_{HH1CK}	1.6		1.4		ns
C inputs via H2 through H	T_{HH2CK}	1.8		1.5		ns
C inputs via DIN	T_{DICK}	0.8		0.7		ns
C inputs via EC	T_{ECCK}	0.9		0.8		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.5		0.4		ns
CIN input via F/G	T_{CCK}	2.2		1.9		ns
CIN input via F/G and H	T_{CHCK}	3.2		2.7		ns
Hold Time after Clock K						
F/G inputs	T_{CKI}	0.0		0.0		ns
F/G inputs via H	T_{CKIH}	0.0		0.0		ns
C inputs via SR/H0 through H	T_{CKHH0}	0.0		0.0		ns
C inputs via H1 through H	T_{CKHH1}	0.0		0.0		ns
C inputs via DIN/H2 through H	T_{CKHH2}	0.0		0.0		ns
C inputs via DIN/H2	T_{CKDI}	0.0		0.0		ns
C inputs via EC	T_{CKEC}	0.0		0.0		ns
C inputs via SR, going Low (inactive)	T_{CKR}	0.0		0.0		ns
Clocks						
Clock High time	T_{CH}	3.0		2.5		ns
Clock Low time	T_{CL}	3.0		2.5		ns
Set/Reset Direct						
Width (High)	T_{RPW}	2.8		2.5		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		2.8		2.4	ns
Global Set/Reset						
Minimum GSR Pulse Width	T_{MRW}		17.3		15.0	ns
Delay from GSR input to any Q	T_{MRQ}		32.9		28.6	ns
Toggle Frequency (MHz) (for export control purposes)	F_{TOG}		166		200	MHz
		Advance				

XC4000XV RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XV devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	**Speed Grade**		**-2**		**-1**		**Units**
	Size	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Write Operation							
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	9 9		7.7 7.7		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	4.5 4.5		3.9 3.9		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	2.0 2.0		1.8 1.7		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0.0 0.0		0.0 0.0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	2.0 2.5		1.7 2.1		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0.0 0.0		0.0 0.0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	1.9 1.8		1.6 1.5		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0.0 0.0		0.0 0.0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		6.5 7.7		5.6 6.7	ns ns
R**ead Operation**							
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	4.5 6.5		2.6 3.8		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		1.4 2.4		1.3 2.2	ns ns
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	1.1 2.1		0.9 1.8		ns ns
			Advance				

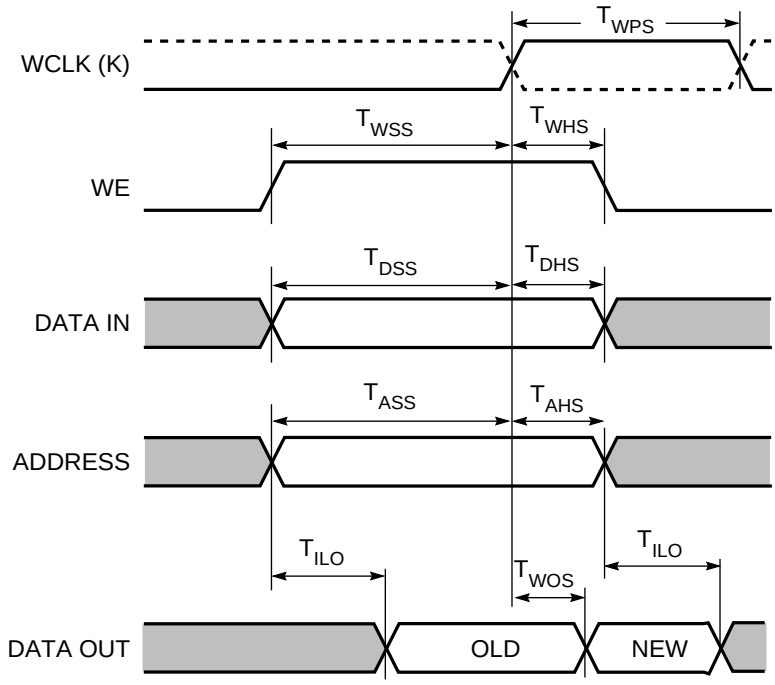
XC4000XV CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XV devices and are expressed in nanoseconds unless otherwise noted.

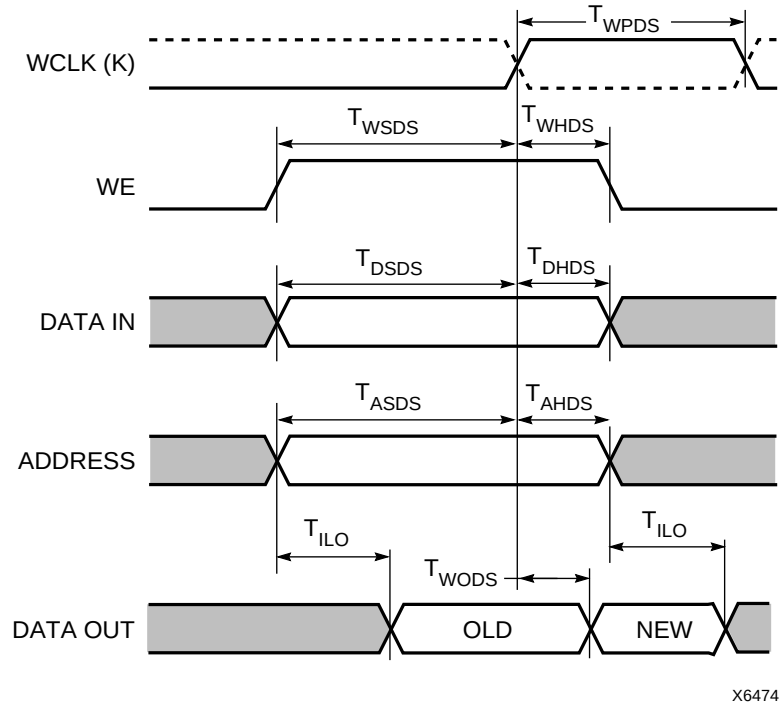
Dual Port RAM	**Speed Grade**		**-2***		**-1**		**Units**
	Size	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Address write cycle time (clock K period)	16x1	T_{WCDS}	9		7.7		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	4.5		3.9		ns
Address setup time before clock K	16x1	T_{ASDS}	2.1		1.8		ns
Address hold time after clock K	16x1	T_{AHDS}	0.0		0.0		ns
DIN setup time before clock K	16x1	T_{DSDS}	2.3		2.0		ns
DIN hold time after clock K	16x1	T_{DHDS}	0.0		0.0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.9		1.6		ns
WE hold time after clock K	16x1	T_{WHDS}	0.0		0.0		ns
Data valid after clock K	16x1	T_{WODS}		7.5		6.5	ns
			Advance				

Note: Timing for 16 x1 RAM option is identical to16 x 2 RAM.

XC4000XV CLB RAM Synchronous (Edge-Triggered) Write Timing



XC4000XV CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

XC4000XV Output Flip-Flop, Clock to Out

		Speed Grade	-2	-1	Units
Description	**Symbol**	**Device**	**Max**	**Max**	
Global Low Skew Clock to Output using OFF	T_{ICKOF}	XC40125XV	9.0	7.8	ns
Global Early Clock to Output using OFF for BUFGEs # 1, 2, 5, & 6	T_{ICKEOF_1256}	XC40125XV	8.1	7.1	ns
Global Early Clock to Output using OFF for BUFGEs # 3, 4, 7, & 8	T_{ICKEOF_3478}	XC40125XV	9.3	7.1	ns
For output SLOW option add	T_{SLOW}	All Devices	2.3	2.0	ns
OFF = Output Flip Flop			**Advance**		

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.

Capacitive Load Factor

Figure 1 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 1 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

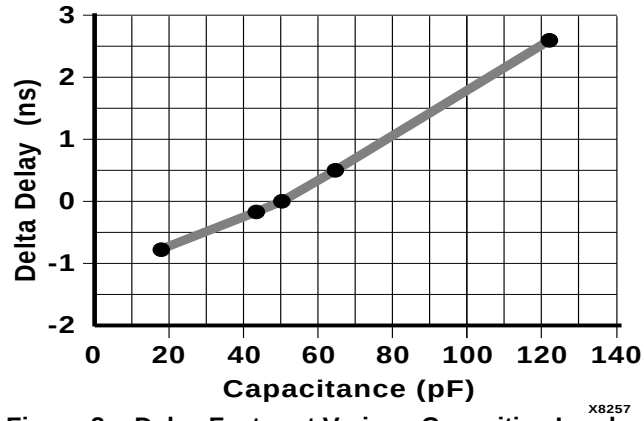


Figure 2: Delay Factor at Various Capacitive Loads

Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

XC4000XV Global Low Skew Clock, Set-Up and Hold

		Speed Grade	-2	-1	Units
Description	**Symbol**	**Device**	**Min**	**Min**	
Input Setup and Hold Times Using Global Low Skew Clock & IFF					
No Delay	T_{PSN}/T_{PHN}	XC40125XV	1.1 / 6.6	0.9 / 5.7	ns
Partial Delay	T_{PSP}/T_{PHP}	XC40125XV	11.3 / 0.0	9.8 / 0.0	ns
Full Delay	T_{PSD}/T_{PHD}	XC40125XV	9.7 / 0.0	8.4 / 0.0	ns
			Advance		

IFF = Input Flip-Flop or Latch

Notes: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

XC4000XV BUFGE #s 3, 4, 7, & 8 Global Early Clock, Set-Up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade	-2	-1	Units
Description	**Symbol**	**Device**	**Min**	**Min**	
Input Setup and Hold Times					
No Delay, Global Early Clock and IFF, Global Early Clock and FCL	T_{PSEN}/T_{PHEN} T_{PFSEN}/T_{PFHEN}	XC40125XV	1.1 / 6.6	0.9 / 5.7	ns
Partial Delay, Global Early Clock and IFF, Global Early Clock and FCL	T_{PSEP}/T_{PHEP} T_{PFSEP}/T_{PFHEP}	XC40125XV	12.7 / 0.0	11.0 / 0.0	ns
Full Delay, Global Early Clock and IF**F**	T_{PSED}/T_{PHED}	XC40125XV	11.1 / 0.0	9.6 / 0.0	ns
IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch			**Advance**		

Notes: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XC4000XV BUFGE #s 1, 2, 5, & 6 Global Early Clock, Set-Up and Hold for IFF and FCL

		Speed Grade	-2	-1	Units
Description	**Symbol**	**Device**	**Min**	**Min**	
Input Setup and Hold Times					
No Delay,Global Early Clock and IFF, Global Early Clock and FCL	T_{PSEN}/T_{PHEN} T_{PFSEN}/T_{PFHEN}	XC40125XV	1.4 / 5.5	1.2 / 4.7	ns
Partial Delay, Global Early Clock and IFF, Global Early Clock and FCL	T_{PSEP}/T_{PHEP} T_{PFSEP}/T_{PFHEP}	XC40125XV	14.5 / 0.0	12.6 / 0.0	ns
Full Delay, Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC40125XV	12.9 / 0.0	11.2 / 0.0	ns
IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch			**Advance**		

Notes: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XC4000XV IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)**.**

Speed Grade		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Clocks						
Clock Enable (EC) to Clock (IK)	T_{ECIK}	0.0		0.0		ns
Delay from Fast Capture Latch enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	1.1		0.9		ns
Setup Times						
Pad to Clock (IK), no delay	T_{PICK}	1.1		0.9		ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	1.3		1.1		ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	0.7		0.6		ns
Hold Times						
All Hold Times		0.0		0.0		ns
Global Set/Reset						
Minimum GSR Pulse Width	T_{MRW}	17.3		15.0		ns
Delay from GSR input to any Q - XC40125XV	T_{RRI}	32.9		28.6		ns
Propagation Delays						
Pad to I1, I2	T_{PID}		0.6		0.4	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}		0.8		0.7	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}		1.0		0.8	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}		1.3		1.0	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}		1.4		1.1	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}		2.4		2.0	ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Advance

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XC4000XV IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

		-2		-1		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Clocks						
Clock High	T_{CH}	3.0		2.5		ns
Clock Low	T_{CL}	3.0		2.5		ns
Propagation Delays (See Note 1)						
Clock (OK) to Pad	T_{OKPOF}		2.7		2.4	ns
Output (O) to Pad	T_{OPF}		2.1		1.9	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		3.8		3.3	ns
3-state to Pad active and valid	T_{TSONF}		3.8		3.3	ns
Output (O) to Pad via Fast Output MUX	T_{OFPF}		2.6		2.2	ns
Select (OK) to Pad via Fast MUX	T_{OKFPF}		2.4		2.1	ns
Setup and Hold Times						
Output (O) to clock (OK) setup time	T_{OOK}	0.2		0.2		ns
Output (O) to clock (OK) hold time	T_{OKO}	0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}	0.0		0.0		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}	0.3		0.2		ns
Global Set/Reset						
Minimum GSR pulse width	T_{MRW}	17.3		15.0		ns
Delay from GSR input to any Pad - XC40125XV	T_{RPO}	35.5		30.9		ns
Slew Rate Adjustment						
For output SLOW option add	T_{SLOW}		2.3		2.0	ns

Note: Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads.

Advance

Pin Locations for XC40125XV Devices

XC40125XV Pad Name	BG432	BG560	PG559
VCCIO	VCCIO	VCCIO*	VCCIO*
I/O (A8)	D17	A17	AB6
I/O (A9)	A17	B18	AB4
I/O	C17	C18	AA7
I/O	B17	E18	AC1
I/O	-	D18	AA5
I/O	-	A19	AA3
GND	GND*	GND*	GND*
I/O (A19)	C18	C19	Y8
I/O (A18)	D18	D19	AB2
I/O	B18	E19	Y6
I/O	A19	B20	AA1
I/O (A10)	B19	C20	Y4
I/O (A11)	C19	D20	W7
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	D19	A21	W5
I/O	A20	E20	V6
I/O	B20	B21	V4
I/O	C20	C21	Y2
I/O	B21	D21	U3
I/O	D20	B22	U7
I/O	-	E21	V2
I/O	-	C22	U5
GND	GND*	GND*	GND*
I/O	-	D22	T4
I/O	-	A23	U1
I/O	C21	C23	R3
I/O	A22	E22	R5
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	B22	B24	T8
I/O	C22	D23	T2
VCCINT	B23	C24	VCCINT*
I/O	-	-	P4
I/O	A24	A25	R7
GND	GND*	GND*	GND*
I/O	D22	E23	N3
I/O	C23	B25	R1
I/O	B24	D24	N5
I/O	C24	C25	P2
I/O	-	B26	M4
I/O	-	E24	L1
I/O	-	C26	L3
I/O	-	D25	P8
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	-	A27	N7
I/O	-	A28	K2
I/O	D23	E25	M6
I/O	B25	C27	J1
I/O	A26	D26	L5
I/O	C25	B28	H2
I/O (A12)	D24	B29	K4
I/O (A13)	B26	E26	J3
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	A27	C28	L7
I/O	D25	D27	J5
I/O	C26	B30	G1

XC40125XV Pad Name	BG432	BG560	PG559
I/O	B27	C29	H4
I/O	A28	E27	F2
I/O	D26	A31	G5
GND	GND*	GND*	GND*
I/O	C27	D28	H6
I/O	B28	C30	K8
I/O	D27	D29	D2
I/O	B29	E28	J7
I/O (A14)	C28	D30	F4
I/O, GCK8 (A15)	D28	E29	E3
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O, GCK1 (A16)	D29	B33	C1
I/O (A17)	C30	F29	C3
VCCINT	E28	E30	VCCINT*
I/O	-	-	F6
I/O	E29	D31	A3
I/O (TDI)	D30	F30	H8
I/O (TCK)	D31	C33	D4
GND	GND*	GND*	GND*
I/O	F28	G29	D6
I/O	F29	E31	C5
I/O	E30	D32	E7
I/O	E31	G30	B4
I/O	G28	F31	H10
I/O	G29	H29	G9
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	-	E32	F8
I/O	-	E33	D8
I/O	F30	H30	B6
I/O	F31	G31	E9
I/O	H28	J29	A7
I/O	H29	F33	G11
I/O	G30	G32	H14
I/O	H30	J30	F12
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	-	H31	G13
I/O	-	K29	E11
I/O	-	H32	B8
I/O	-	J31	D10
I/O	J28	K30	A9
I/O	J29	H33	G15
I/O	H31	L29	B10
I/O	J30	K31	H16
GND	GND*	GND*	GND*
I/O	K28	L30	C9
I/O	-	-	E13
VCCINT	K29	K32	VCCINT*
I/O (TMS)	K30	J33	A11
I/O	K31	M29	D12
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	-	L31	C11
I/O	-	M30	B14
I/O	L29	L32	G17
I/O	L30	M31	E15
GND	GND*	GND*	GND*
I/O	M30	N29	D14

XC40125XV Pad Name	BG432	BG560	PG559
I/O	M28	L33	A15
I/O	-	N30	C13
I/O	-	N31	B16
I/O	M29	M32	E17
I/O	M31	P29	F18
I/O	N31	P30	A17
I/O	N28	N33	G19
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	N29	P31	D16
I/O	N30	P32	C15
I/O	P30	R29	B18
I/O	P28	R30	H20
I/O	P29	R31	B20
I/O	R31	R33	E19
GND	GND*	GND*	GND*
I/O	R30	T31	D18
I/O	R28	T29	F20
I/O	-	T30	G21
I/O	-	T32	C17
VCCINT	R29	U32	VCCINT*
I/O	-	-	D20
I/O	T31	U31	E21
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	T30	U29	C21
I/O	T29	U30	F22
I/O	-	U33	A21
I/O	-	V32	D22
I/O	U31	V31	B22
I/O	U30	V29	G23
GND	GND*	GND*	GND*
I/O	U28	V30	E23
I/O	U29	W33	C23
I/O	V30	W31	A23
I/O	V29	W30	D24
I/O	V28	W29	B24
I/O	W31	Y32	H24
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	W30	Y31	F24
I/O	W29	Y30	E25
I/O	-	AA33	B26
I/O	-	Y29	D26
I/O	W28	AA32	A27
I/O	Y31	AA31	G25
I/O	Y30	AA30	B28
I/O	Y29	AB32	C27
GND	GND*	GND*	GND*
I/O	Y28	AA29	F26
I/O	AA30	AB31	E27
I/O	-	AB30	A29
I/O	-	AC33	D28
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	AA29	AC31	G27
I/O	AB31	AB29	B30
VCCINT	AB30	AD32	VCCINT*
I/O	-	-	C29
I/O	AB29	AC30	E29
GND	GND*	GND*	GND*
I/O	AB28	AD31	D30

XC40125XV Pad Name	BG432	BG560	PG559
I/O	AC30	AE33	A33
I/O	AC29	AC29	C31
I/O	AC28	AE32	B34
I/O	-	AD30	H28
I/O	-	AE31	A35
I/O	-	AF32	G29
I/O	-	AD29	E31
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	-	AF31	D32
I/O	-	AE30	C35
I/O	AD31	AG33	C33
I/O	AD30	AH33	B36
I/O	AD29	AE29	H30
I/O	AD28	AG31	A37
I/O	AE30	AF30	G31
I/O	AE29	AH32	F32
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	AF31	AJ32	E33
I/O	AE28	AF29	D34
I/O	AF30	AH31	B38
I/O	AF29	AG30	G33
I/O	AG31	AK32	A41
I/O	AF28	AJ31	E35
GND	GND*	GND*	GND*
I/O	AG30	AG29	D36
I/O	AG29	AL33	F36
I/O	AH31	AH30	G35
I/O	-	-	H34
VCCINT	AG28	AK31	VCCINT*
I/O	AH30	AJ30	B40
I/O, GCK2	AJ30	AH29	E37
O (M1)	AH29	AK30	D38
GND	GND*	GND*	GND*
I (M0)	AH28	AJ29	C39
VCCIO	VCCIO*	VCCIO*	VCCIO*
I (M2)	AJ28	AN32	H36
I/O, GCK3	AK29	AJ28	F38
I/O (HDC)	AH27	AK29	C41
I/O	AK28	AL30	D40
I/O	AJ27	AK28	B42
I/O	AL28	AM31	J37
I/O ($\overline{\text{LDC}}$)	AH26	AJ27	K36
GND	GND*	GND*	GND*
I/O	AK27	AN31	H38
I/O	AJ26	AL29	D42
I/O	AL27	AK27	G39
I/O	AH25	AL28	C43
I/O	AK26	AJ26	F40
I/O	AL26	AM30	E41
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	AH24	AM29	L37
I/O	AJ25	AK26	J39
I/O	AK25	AL27	F42
I/O	AJ24	AJ25	H40
I/O	AH23	AN29	G43
I/O	AK24	AN28	J41
I/O	-	AK25	H42
I/O	-	AL26	N37

XC40125XV Pad Name	BG432	BG560	PG559
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	-	AJ24	P36
I/O	-	AM27	M38
I/O	-	AM26	J43
I/O	-	AK24	L39
I/O	AL24	AL25	K42
I/O	AH22	AJ23	K40
I/O	AJ23	AN26	L43
I/O	AK23	AL24	L41
GND	GND*	GND*	GND*
I/O	AJ22	AK23	R37
I/O	-	-	P42
VCCINT	AK22	AN25	VCCINT*
I/O	AL22	AJ22	T36
I/O	AJ21	AL23	N39
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	AH20	AM24	M40
I/O	AK21	AK22	R43
I/O	-	AM23	N41
I/O	-	AJ21	R39
GND	GND*	GND*	GND*
I/O	-	AL22	U37
I/O	-	AN23	T42
I/O	AJ20	AK21	P40
I/O	AH19	AM22	U43
I/O	AK20	AJ20	R41
I/O	AJ19	AL21	V42
I/O	AL20	AN21	U39
I/O	AH18	AK20	V38
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	AK19	AL20	W37
I/O	AJ18	AJ19	T40
I/O	AL19	AM20	Y42
I/O	AK18	AK19	U41
I/O	AH17	AL19	Y36
I/O	AJ17	AN19	V40
GND	GND*	GND*	GND*
I/O	-	AJ18	W39
I/O	-	AK18	AA43
I/O	AK17	AL18	Y38
I/O	AL17	AM18	Y40
I/O	AJ16	AK17	AA37
I/O ($\overline{\text{INIT}}$)	AK16	AJ17	AA39
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	AL16	AL17	AA41
I/O	-	-	AB38
VCCINT	AH15	AM17	VCCINT*
I/O	AL15	AN17	AB42
I/O	AJ15	AK16	AB40
I/O	-	AJ16	AC37
I/O	-	AL16	AC39
GND	GND*	GND*	GND*
I/O	AK15	AM16	AD36
I/O	AJ14	AL15	AC41
I/O	AH14	AK15	AD38
I/O	AK14	AJ15	AC43
I/O	AL13	AN15	AD40
I/O	AK13	AM14	AE39

XC40125XV Pad Name	BG432	BG560	PG559
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	AJ13	AL14	AE37
I/O	AH13	AK14	AF40
I/O	AL12	AJ14	AD42
I/O	AK12	AN13	AF42
I/O	AJ12	AM13	AF38
I/O	AK11	AL13	AG39
I/O	-	AK13	AG43
I/O	-	AJ13	AG37
GND	GND*	GND*	GND*
I/O	-	AM12	AH40
I/O	-	AL12	AJ41
I/O	AH12	AK12	AG41
I/O	AJ11	AN11	AK40
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	AL10	AJ12	AJ39
I/O	AK10	AL11	AH42
VCCINT	AJ10	AK11	VCCINT*
I/O	-	-	AH36
I/O	AK9	AM10	AL39
GND	GND*	GND*	GND*
I/O	AL8	AL10	AJ37
I/O	AH10	AJ11	AJ43
I/O	AJ9	AN9	AM40
I/O	AK8	AK10	AK42
I/O	-	AM9	AN41
I/O	-	AL9	AL41
I/O	-	AJ10	AR41
I/O	-	AM8	AK36
GND	GND	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	-	AK9	AL37
I/O	-	AL8	AN43
I/O	AJ8	AN7	AM38
I/O	AH9	AJ9	AP42
I/O	AK7	AL7	AN39
I/O	AL6	AK8	AR43
I/O	AJ7	AN6	AP40
I/O	AH8	AM6	AT40
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	AK6	AJ8	AN37
I/O	AL5	AL6	AR39
I/O	AH7	AK7	AT42
I/O	AJ6	AM5	BA43
I/O	AK5	AM4	AU43
I/O	AL4	AJ7	AU39
GND	GND*	GND*	GND*
I/O	AH6	AL5	AT38
I/O	AJ5	AK6	AP36
I/O	AK4	AN3	AR37
I/O	-	-	AV42
VCCINT	AH5	AK5	VCCINT*
I/O	AK3	AJ6	AV40
I/O, GCK4	AJ4	AL4	AW41
GND	GND*	GND*	GND*
DONE	AH4	AJ5	AY42
VCCIO	VCCIO*	VCCIO*	VCCIO*
$\overline{\text{PROGRAM}}$	AH3	AM1	BB42
I/O (D7)	AJ2	AH5	BC41

XC40125XV Pad Name	BG432	BG560	PG559
I/O, GCK5	AG4	AJ4	AV38
I/O	AG3	AK3	BA39
I/O	AH2	AH4	AT36
I/O	AH1	AL1	BB40
I/O	AF4	AG5	AY40
GND	GND*	GND*	GND*
I/O	AF3	AJ3	BA41
I/O	AG2	AK2	BB38
I/O	AG1	AG4	AY38
I/O	AE4	AH3	BC37
I/O	AE3	AF5	AW37
I/O	AF2	AJ2	AT34
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O (D6)	AF1	AJ1	AU35
I/O	AD4	AF4	AV36
I/O	AD3	AG3	BB36
I/O	AE2	AE5	AY36
I/O	AD2	AH1	BC35
I/O	AC4	AF3	AW35
I/O	-	AE4	AU33
I/O	-	AG2	AT30
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	-	AD5	AV32
I/O	-	AF2	AU31
I/O	-	AF1	AW33
I/O	-	AD4	BB34
I/O	AC3	AE3	AY34
I/O	AD1	AC5	BC33
I/O	AC2	AE1	AU29
I/O	AB4	AD3	AT28
GND	GND*	GND*	GND*
I/O	AB3	AC4	BA35
I/O	-	-	BB30
VCCINT	AB2	AD2	VCCINT*
I/O	AB1	AB5	AW31
I/O	AA3	AC3	AY32
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	-	AB4	BA33
I/O	-	AC1	AU27
I/O (D5)	AA2	AA5	BC29
I/O ($\overline{CS0}$)	Y2	AB3	AW29
GND	GND*	GND*	GND*
I/O	Y4	AB2	AY30
I/O	Y3	AA4	BA31
I/O	Y1	AA3	BB28
I/O	W1	Y5	AW27
I/O	-	AA1	BC27
I/O	-	Y4	AV26
I/O	W4	Y3	AU25
I/O	W3	Y2	AY28
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	W2	W5	BA29
I/O	V2	W4	AT24
I/O	V4	W3	BB26
I/O	V3	W1	AW25
I/O	U1	V3	BB24
I/O	U2	V5	AY26
GND	GND*	GND*	GND*

XC40125XV Pad Name	BG432	BG560	PG559
I/O	U4	V4	AV24
I/O	U3	V2	AU23
I/O	-	U2	BA27
I/O	-	U1	BC23
I/O (D4)	T1	U5	AY24
I/O	T2	U4	AW23
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O (D3)	T3	U3	BA23
I/O ($\overline{RS}$)	R1	T2	AV22
VCCINT	R2	T3	VCCINT*
I/O	-	-	AY22
I/O	-	T5	BB22
I/O	-	T4	AU21
I/O	R4	R1	AW21
GND	GND*	GND*	GND*
I/O	R3	R3	BA21
I/O	P2	R4	BC21
I/O	P3	R5	AY20
I/O	P4	P2	BB20
I/O	N1	P3	AT20
I/O	N2	P4	AV20
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND	GND*	GND*
I/O	N3	N1	AW19
I/O	N4	P5	AY18
I/O	M1	N2	BB18
I/O	M2	N3	AU19
I/O	-	N4	BC17
I/O	-	M2	BA17
I/O	M3	N5	AV18
I/O	M4	M3	AW17
GND	GND*	GND*	GND*
I/O (D2)	L2	M4	AY16
I/O	L3	L1	BB16
I/O	-	L3	AU17
I/O	-	M5	BA15
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	K1	K2	AW15
I/O	K2	L4	BC15
VCCINT	K3	J1	VCCINT*
I/O	-	-	AY14
I/O	K4	K3	BA13
GND	GND*	GND*	GND*
I/O	J2	L5	AT16
I/O	J3	J2	BB14
I/O	J4	K4	AU15
I/O	H1	J3	BC11
I/O	-	H2	AW13
I/O	-	K5	BB10
I/O	-	H3	AY12
I/O	-	J4	BA11
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	H2	G1	AT14
I/O	H3	F1	AU13
I/O	H4	J5	AV12
I/O	G2	G3	BC9
I/O	G3	H4	AW11
I/O	F1	F2	BB8
I/O	-	E2	AY10

XC40125XV Pad Name	BG432	BG560	PG559
I/O	-	H5	AU11
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O (D1)	G4	F3	BA9
I/O ($\overline{RCLK}$ $\overline{RDY}$/$\overline{BUSY}$)	F2	G4	AW9
I/O	F3	D2	BC7
I/O	E1	E3	AY8
I/O	F4	G5	AV8
I/O	E2	C1	AT10
GND	GND*	GND*	GND*
I/O	E3	F4	AU9
I/O	D1	D3	BB6
I/O	E4	B3	AW7
I/O	D2	F5	BC3
I/O (D0, DIN)	C2	E4	AY6
I/O, GCK6 (DOUT)	D3	D4	BB4
CCLK	D4	C4	BA5
VCCIO	VCCIO*	VCCIO*	VCCIO*
O, TDO	C4	E6	BA3
GND	GND*	GND*	GND*
I/O (A0, $\overline{WS}$)	B3	D5	AT8
I/O, GCK7 (A1)	D5	A2	AV6
VCCINT	B4	D6	VCCINT*
I/O	-	-	BB2
I/O	C5	A3	AY4
I/O	A4	E7	AR7
I/O	D6	C5	AP8
GND	GND*	GND*	GND*
I/O	B5	B4	AT6
I/O	C6	D7	AY2
I/O (CS1, A2)	A5	C6	AU5
I/O (A3)	D7	E8	BA1
I/O	B6	B5	AV4
I/O	A6	A5	AW3
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	D8	D8	AN7
I/O	C7	C7	AR5
I/O	B7	E9	AV2
I/O	D9	A6	AT4
I/O	B8	B7	AU1
I/O	A8	D9	AR3
I/O	-	C8	AT2
I/O	-	E10	AL7
VCCIO	VCCIO*	VCCIO*	VCCIO*
GND	GND*	GND*	GND*
I/O	-	B8	AK8
I/O	-	A8	AM6

XC40125XV Pad Name	BG432	BG560	PG559
I/O	-	D10	AN5
I/O	-	C9	AR1
I/O	D10	E11	AP4
I/O	C9	A9	AN3
I/O	B9	C10	AP2
I/O	C10	D11	AJ7
GND	GND*	GND*	GND*
I/O	B10	B10	AH8
I/O	-	-	AL5
VCCINT	A10	E12	VCCINT*
I/O	C11	C11	AN1
I/O	D12	B11	AM4
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O	B11	D12	AL3
I/O	C12	A11	AJ5
I/O	-	E13	AK2
I/O	-	C12	AG7
GND	GND*	GND*	GND*
I/O	-	B12	AK4
I/O	-	D13	AJ3
I/O	D13	C13	AG5
I/O	B12	E14	AJ1
I/O	C13	A13	AF6
I/O	A12	D14	AH2
I/O	D14	C14	AE7
I/O	B13	B14	AH4
GND	GND*	GND*	GND*
VCCIO	VCCIO*	VCCIO*	VCCIO*
I/O (A4)	C14	E15	AG3
I/O (A5)	A13	D15	AD8
I/O	B14	C15	AG1
I/O	D15	A15	AF4
I/O (A21)	C15	C16	AE5
I/O (A20)	B15	E16	AD6
GND	GND*	GND*	GND*
I/O	-	D16	AD4
I/O	-	B16	AF2
I/O	A15	B17	AC7
I/O	-	-	AD2
VCCINT	C16	C17	VCCINT*
I/O (A6)	B16	E17	AC5
I/O (A7)	A16	D17	AC3
GND	GND*	GND*	GND*

1/29/98

* Pads labelled GND*, VCCIO*, or VCCINT* are internally bonded to Ground or VCCIO planes within the package. They have no direct connection to any specific package pin.

Additional XC40125XV Package Pins

PG559

VCCIO Pins						
A13	A31	A43	B2	C7	C19	C25
C37	F14	F30	G3	G7	G37	G41
N1	N43	P6	P38	W3	W41	AE3
AE41	AK6	AK38	AL1	AL43	AU3	AU7
AU37	AU41	AV14	AV30	BA7	BA19	BA25
BA37	BC1	BC13	BC31	BC43	-	-
VCCINT Pins**						
H12	H18	H26	H32	M8	M36	V8
V36	AF8	AF36	AM8	AM36	AT12	AT18
AT26	AT32	-	-	-	-	-
GND Pins						
A5	A19	A25	A39	B12	B32	E1
E5	E39	E43	F10	F16	F28	F34
H22	K6	K38	M2	M42	T6	T38
W1	W43	AB8	AB36	AE1	AE43	AH6
AH38	AM2	AM42	AP6	AP38	AT22	AV10
AV16	AV28	AV34	AW1	AW5	AW39	AW43
BB12	BB32	BC5	BC19	BC25	BC39	-

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BG560

VCCIO Pins						
A4	A10	A16	A22	A26	A30	B2
B13	B19	B32	C3	C31	C32	D1
D33	E5	H1	K33	M1	N32	R2
T33	V1	W32	AA2	AB33	AD1	AF33
AK1	AK4	AK33	AL2	AL3	AL31	AM2
AM15	AM21	AM32	AN4	AN8	AN12	AN18
AN24	AN30	-	-	-	-	-
GND Pins						
A7	A12	A14	A18	A20	A24	A29
A32	B1	B6	B9	B15	B23	B27
B31	C2	E1	F32	G2	G33	J32
K1	L2	M33	P1	P33	R32	T1
V33	W2	Y1	Y33	AB1	AC32	AD33
AE2	AG1	AG32	AH2	AJ33	AL32	AM3
AM11	AM19	AM25	AM28	AM33	AM7	AN2
AN5	AN10	AN14	AN16	AN20	AN22	AN27
N.C. Pins						
A1	A33	AC2	AN1	AN33	-	-

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BG432

VCCIO Pins						
A1	A11	A21	A31	D11	D21	L1
L4	L28	L31	AA1	AA4	AA28	AA31
AH11	AH21	AL1	AL11	AL21	AL31	C3
C29	AJ3	AJ29				
GND Pins						
A2	A3	A7	A9	A14	A18	A23
A25	A29	A30	B1	B2	B30	B31
C1	C31	D16	G1	G31	J1	J31
P1	P31	T4	T28	V1	V31	AC1
AC31	AE1	AE31	AH16	AJ1	AJ31	AK1
AK2	AK30	AK31	AL2	AL3	AL7	AL9
AL14	AL18	AL23	AL25	AL29	AL30	
N.C. Pins						
C8					-	-

** VCCINT pins must be connected to VCC in package compatible XC4085XL-PG559