Development Systems Descriptions

It's simple to order a Xilinx Development System. Just choose a Foundation or Alliance Series and a few options. Give your local Xilinx Sales Office a call for information about our evaluation kits.

Foundation Series

- Foundation Base System (PC)
- Foundation Base-Express System (PC)
- Foundation Standard System (PC)
- Foundation Express System (PC)

Alliance Series

- Alliance Base (PC or Workstation)
- Alliance Standard (PC or Workstation)

Alliance Series Options

- VIEWlogic Workview Office Standard Development System Options (PC)

Foundation Series: Foundation Base System (PC)

Overview

The Foundation Series provides a complete, ready-to-use design system for the design of Xilinx programmable logic devices. The Foundation Base System provides design entry (schematic and Abel HDL), simulation, and device implementation tools for a broad array of FPGA and CPLD devices targeted for low density and high volume applications.

System Features

- Project manager
- Schematic editor
- Integrated HDL editor with support for the Abel 6 HDL
- Functional and timing simulator
- EDIF, VHDL (VITAL compliant), and Verilog / SDF design interfaces
- Device implementation software for Xilinx CPLDs and FPGAs
- Comprehensive on-line help, on-line documentation, and software tutorials
- Software maintenance, including hotline support and software updates

Device Support

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X Up to XC4010E/X
  - Spartan
  - XC3x00A/L
  - XC5200 Up to XC5210 FPGAs

Required Hardware Environment

- Windows 95 and Windows NT 4.0 compatible PCs
- Minimum memory requirements: 32 MB RAM, 32-64 MB Virtual Memory
- CD-ROM drive

Package Features - Foundation Base System

Feature	FND BAS	FND STD	FND BSX	FND EXP
CPLD Devices	√	√	√	√
FPGA Devices	√[1]	√	√[1]	√
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
HDL Editor	√	√	√	√
Graphical State Editor	√	√	√	√
ABEL 6 Entry / Synthesis	√	√	√	√
VHDL Entry / Synthesis			√	√
Verilog Entry / Synthesis			√	√
Schematic-centric Synthesis	√	√	√	√
HDL-centric Synthesis				√
Simulator	√	√	√	√
Device Implementation	√	√	√	√
Maintenance[2]	√	√	√	√

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Notes:
1. Spartan, XC3x00A/X, XC4000E/X up to XC4010E/X, and XC5200 up to XC5210.
2. A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information.

Foundation Series: Foundation Base-Express System with VHDL/Verilog Synthesis(PC)

Overview

The Foundation Series provides a complete, ready-to-use design system for the design of Xilinx programmable logic devices. The Foundation Express System incorporates advanced synthesis technology from Synopsys, and provides design entry (schematic and HDL), VHDL and Verilog synthesis, simulation, and device implementation tools for a broad array of FPGA and CPLD devices targeted for low density and high volume applications.

System Features

- Project manager
- Schematic editor
- Integrated HDL editor with support for VHDL, Verilog, and Abel 6 HDL
- VHDL and Verilog synthesis, including compilation and optimization
- Functional and timing simulator
- EDIF, VHDL (VITAL compliant), and Verilog / SDF design interfaces
- Device implementation software for Xilinx CPLDs and FPGAs
- Comprehensive on-line help, on-line documentation, and software tutorials
- Software maintenance, including hotline support and software updates

Device Support

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X Up to XC4010E/X
  - Spartan
  - XC3x00A/L
  - XC5200 Up to XC5210 FPGAs

Required Hardware Environment

- Windows 95 and Windows NT 4.0 compatible PCs
- Minimum memory requirements: 32 MB RAM, 32-64 MB Virtual Memory
- CD-ROM drive

Package Features - Foundation Base-Express System

Feature	FND BAS	FND STD	FND BSX	FND EXP
CPLD Devices	√	√	√	√
FPGA Devices	√[1]	√	√[1]	√
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
HDL Editor	√	√	√	√
Graphical State Editor	√	√	√	√
ABEL 6 Entry / Synthesis	√	√	√	√
VHDL Entry / Synthesis			√	√
Verilog Entry / Synthesis			√	√
Schematic-centric Synthesis	√	√	√	√
HDL-centric Synthesis				√
Simulator	√	√	√	√
Device Implementation	√	√	√	√
Maintenance[2]	√	√	√	√

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Notes:
1. Spartan, XC3x00A/L, XC4000E/X up to XC4010E/X, and XC5200 up to XC5210.
2. A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information.

Foundation Series: Foundation Standard System (PC)

Overview

The Foundation Series provides a complete, ready-to-use design system for the design of Xilinx programmable logic devices. The Foundation Standard System provides design entry (schematic and Abel HDL), simulation, and device implementation tools for all Xilinx CPLDs and Xilinx FPGAs.

System Features

- Project manager
- Schematic editor
- Integrated HDL editor with support for the Abel 6 HDL
- Functional and timing simulator
- EDIF, VHDL (VITAL compliant), and Verilog / SDF design interfaces
- Device implementation software for Xilinx CPLDs and FPGAs
- Comprehensive on-line help, on-line documentation, and software tutorials
- Software maintenance, including hotline support and software updates

Device Support

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X
  - Spartan
  - XC3x00A/L
  - XC5200

Required Hardware Environment

- Windows 95 and Windows NT 4.0 compatible PCs
- Minimum memory requirements
  - Small Devices (< 10K gates): 32 MB RAM, 32-64 MB Virtual Memory
  - Medium Devices (10K to 30K gates): 64 MB RAM, 64-128 MB Virtual Memory
  - Large Devices (> 30K gates): 128 MB RAM, 128-256 MB Virtual Memory
- CD-ROM drive

Package Features - Foundation Base System

Feature	FND BAS	FND STD	FND BSX	FND EXP
CPLD Devices	√	√	√	√
FPGA Devices	√[1]	√	√[1]	√
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
HDL Editor	√	√	√	√
Graphical State Editor	√	√	√	√
ABEL 6 Entry / Synthesis	√	√	√	√
VHDL Entry / Synthesis			√	√
Verilog Entry / Synthesis			√	√
Schematic-centric Synthesis	√	√	√	√
HDL-centric Synthesis				√
Simulator	√	√	√	√
Device Implementation	√	√	√	√
Maintenance[2]	√	√	√	√

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Notes:
1. Spartan, XC3x00A/L, XC4000E/X up to XC4010E/X, and XC5200 up to XC5210.
2. A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information.

Foundation Series: Foundation Express System (PC)

Overview

The Foundation Series provides a complete, ready-to-use design system for the design of Xilinx programmable logic devices. The Foundation Express System incorporates advanced synthesis technology from Synopsys, and provides design entry (schematic and HDL), VHDL and Verilog synthesis, simulation, and device implementation tools for all Xilinx CPLDs and Xilinx FPGAs.

System Features

- Project manager
- Schematic editor
- Integrated HDL editor with support for VHDL, Verilog, and Abel 6 HDL
- VHDL and Verilog synthesis, including compilation and optimization
- Functional and timing simulator
- EDIF, VHDL (VITAL compliant), and Verilog / SDF design interfaces
- Device implementation software for Xilinx CPLDs and FPGAs
- Comprehensive on-line help, on-line documentation, and software tutorials
- Software maintenance, including hotline support and software updates

Device Support

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X
  - Spartan
  - XC3x00A/L
  - XC5200

Required Hardware Environment

- Windows 95 and Windows NT 4.0 compatible PCs
- Minimum memory requirements
  - Small Devices (< 10K gates): 32 MB RAM, 32-64 MB Virtual Memory
  - Medium Devices (10K to 30K gates): 64 MB RAM, 64-128 MB Virtual Memory
  - Large Devices (> 30K gates): 128 MB RAM, 128-256 MB Virtual Memory
- CD-ROM drive

Package Features - Foundation Base System

Feature	FND BAS	FND STD	FND BSX	FND EXP
CPLD Devices	√	√	√	√
FPGA Devices	√[1]	√	√[1]	√
Libraries and Interface	√	√	√	√
Schematic Editor	√	√	√	√
HDL Editor	√	√	√	√
Graphical State Editor	√	√	√	√
ABEL 6 Entry / Synthesis	√	√	√	√
VHDL Entry / Synthesis			√	√
Verilog Entry / Synthesis			√	√
Schematic-centric Synthesis	√	√	√	√
HDL-centric Synthesis				√
Simulator	√	√	√	√
Device Implementation	√	√	√	√
Maintenance[2]	√	√	√	√

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Notes:
1. Spartan, XC3x00A/L, XC4000E/X up to XC4010E/X, and XC5200 up to XC5210.
2. A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information.

Alliance Series: Alliance Base (PC or Workstation)

Overview

Next generation FPGA/CPLD design solutions leveraging "Open Systems" integration with premier EDA partners for devices up to 10,000 gates.

Base System Features:

- EDA Libraries & Interfaces
- Design Manager and Flow Engine
- LogiBLOX Module Generator
- Gate Optimizer
- Complete HDL design methodology support
- Incremental design capabilities
- Place and route utilizing SMARTspecs
- Re-entrant router
- Multi-pass PAR
- Timing Analyzer
- Standard netlist and backannotation (EDIF, SDF, VITAL VHDL and Verilog)
- Xchecker Hardware Debugger (workstation only)

Package Includes:

- Alliance Quick Start Guide
- Alliance Release Document
- Answer Database
- Core Technology CD
- CAE Libraries CD
- On-line Documentation CD with DynaText browser
- Hardware Cable
- Demoboard

Device Support:

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X Up to XC4010E/X
  - Spartan
  - XC3x00A/L
  - XC5200 Up to XC5210 FPGAs

Libraries and Interfaces

Cadence

- Concept schematic libraries and Verilog-XL simulation models

Mentor

- Falcon Framework schematic capture library and ModelSim simulation models
- Leonardo synthesis libraries and interfaces are available from Mentor or Exemplar Logic

Synopsys

- HDL Design Solutions (VHDL and Verilog)
- Design Compiler, FPGA Compiler II, FPGA Express, VSS
- Vital Simulation models
- DesignWare arithmetic modules

* No libraries required to support FPGA Express

VIEWlogic

- Workview Office schematic capture library and functional and timing simulation interface

Exemplar

- Leonardo and Galileo synthesis libraries and interfaces are available from Exemplar Logic

Synplicity

- Synplify synthesis libraries and interfaces are available from Synplicity

Model Technology

- ModelSim, V-System HDL simulation libraries and interface

Contact your local EDA sales office to purchase these EDA tools.

Support and Updates Include:

- Answers Database - http://www.xilinx.com or Answers electronic book included.
- Hotline Telephone Support
- Apps FAX and E-Mail
- Online Documentation
- World Wide Web Access
- Technical Newletter
- Extensive Application Notes
- Software Updates (for in-maintenance customers)
  - A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information

Required Hardware Environment (PC)

- Fully IBM compatible PC486/Pentium
  - NEC98 supported
- Windows 95, Windows NT 4.0
  - Chinese, Korean and Japanese versions
- Minimum 300 Mbytes hard-disk space
- CD-ROM drive
- VGA display
- Serial port mouse
- One parallel and two serial ports
- 32 MB RAM (Use additional RAM to increase performance)
- 32 MB - 64 MB Virtual Memory

Required Hardware Environment (Workstation)

- Ultra Sparc (or equivalent)
  - Sun OS 4.1.3 and 4.1.4
  - Solaris 2.5
- HP715 (or equivalent)
  - HP-UX 10.2
- RS6000
  - AIX 4.1.5 (no GUIs)
- 64 MB RAM (Use additional to increase performance)
- 64MB min Swap Space
- Color Monitor

Alliance Series: Alliance Standard (PC or Workstation)

Overview

Next generation FPGA/CPLD design solutions leveraging "Open Systems" integration with premier EDA partners for unlimited gate capacity.

Base System Features:

- EDA Libraries & Interfaces
- Design Manager and Flow Engine
- LogiBLOX Module Generator
- Gate Optimizer
- Full HDL design methodology support
- Incremental design capabilities
- Place and route utilizing SMARTspecs
- Re-entrant router
- Multi-pass PAR
- Timing Analyzer
- Standard netlist and backannotation (EDIF, SDF, VITAL VHDL and Verilog)
- Xchecker Hardware Debugger (workstation only)

Package Includes:

- Alliance Quick Start Guide
- Alliance Release Document
- Answer Database
- Core Technology CD
- CAE Libraries CD
- On-line Documentation CD with DynaText browser
- Hardware Cable
- Demoboard

Device Support:

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X
  - Spartan
  - XC3x00A/L
  - XC5200

Libraries and Interfaces

Cadence

- Concept schematic libraries and Verilog-XL simulation models

Mentor

- Falcon Framework schematic capture library and ModelSim simulation models
- Leonardo synthesis libraries and interfaces are available from Mentor or Exemplar Logic

Synopsys

- HDL Design Solutions (VHDL and Verilog)
- Design Compiler, FPGA Compiler II, FPGA Express, VSS
- Vital Simulation models
- DesignWare arithmetic modules

* No libraries required to support FPGA Express

VIEWlogic

- Workview Office schematic capture library and functional and timing simulation interface

Exemplar

- Leonardo and Galileo synthesis libraries and interfaces are available from Exemplar Logic

Synplicity

- Synplify synthesis libraries and interfaces are available from Synplicity

Model Technology

- ModelSim, V-System HDL simulation libraries and interface

Contact your local EDA sales office to purchase these EDA tools.

Support and Updates Include:

- Answers Database - http://www.xilinx.com or Answers electronic book included.
- Hotline Telephone Support
- Apps FAX and E-Mail
- Online Documentation
- World Wide Web Access
- Technical Newletter
- Extensive Application Notes
- Software Updates (for in-maintenance customers)
  - A period of maintenance is included with new design system licenses, after which annual maintenance contracts may be purchased. Contact your Xilinx sales representative for more information

Required Hardware Environment (PC)

- Fully IBM compatible PC486/Pentium
  - NEC98 supported
- Windows 95, Windows NT 4.0
  - Chinese, Korean and Japanese versions
- Minimum 300 Mbytes hard-disk space
- CD-ROM drive
- VGA display
- Serial port mouse
- One parallel and two serial ports
- Small Devices: (8K or <) XC9536 - XC95108; XC4003E - XC4008E; XC4005XL - XC4008XL
  - 32 MB RAM (Use additional RAM to increase performance)
  - 32 -64 MB Virtual Memory
- Medium Devices: (10K- 28K) XC95144 - XC95216; XC4010E - XC4025E; XC4028EX - XC4036EX; XC4010XL - XC4028XL
  - 64 MB RAM (Use additional RAM to increase performance)
  - 64-128 MB Virtual Memory
- Large Devices: (36K or >) XC4036XL - XC4062XL
  - 128K RAM (Use additional RAM to increase performance)
  - 128 - 256 MB Virtual Memory

Required Hardware Environment (Workstation)

- Ultra Sparc (or equivalent)
  - Sun OS 4.1.3 and 4.1.4
  - Solaris 2.5
- HP715 (or equivalent)
  - HP-UX 10.2
- RS6000
  - AIX 4.1.5 (no GUIs)
- Small Devices: (28K or <) XC4000E; XC4028EX - XC4036EX; XC4005XL - XC4028XL
  - 64 MB RAM (Use additional RAM to increase performance)
  - 64MB min Swap Space
- Large Devices (36K or >) XC4036XL - XC4062XL
  - 128 MB RAM (Use additional RAM to increase performance)
  - 128 MB min Swap Space
- Color Monitor

Alliance Series Options (PC)

Overview

VIEWlogic Workview Office schematic capture and gate simulator development system with libraries and interfaces for Xilinx FPGAs and CPLDs.

Workview Office Standard Features:

- Workview Office schematic editor
- Workview Office gate simulator
- Libraries and interfaces
- Hotline support
- Software maintenance for 90-days

Libraries Support:

- CPLDs:
  - XC9500
- FPGAs:
  - XC4000E/X
  - Spartan
  - XC3x00A/L
  - XC5200

Support and Updates Include:

- Answers Database - http://www.xilinx.com or Answers electronic book included.
- Hotline Telephone Support
- Apps FAX and E-Mail
- Software Updates (for in-maintenance customers)
- Online Documentation
- World Wide Web Access
- Technical Newletter
- Extensive Application Notes

Required Hardware Environment:

- Fully IBM compatible PC486/Pentium
- Windows 95, Windows NT 4.0
  - Chinese, Korean and Japanese versions
- Minimum 500 Mbytes hard-disk space
- CD-ROM drive
- VGA display
- Serial port mouse
- One parallel and two serial ports
- 64 Mbytes RAM recommended (increase to improve performance)