XC4000E High-Reliability Features

- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XC4000E output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Available in class Q fully compliant QML and Military temperature range only
  - Certified to MIL-PRF-38535, appendix A QML (Qualified Manufacturers Listing)

Xilinx High-Reliability

XC4000E family is supplied under the following standard microcircuit drawings (SMDs):

XC4005E 5962-97522
XC4010E 5962-97523
XC4013E 5962-97524
XC4025E 5962-97525

For more information contact DSCC (Defense Supply Center Columbus) Columbus, Ohio.

Table 1: XC4000E Field Programmable Gate Arrays

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. Decode Inputs per side	Max. User I/O	Packages
XC4005E	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112	PG156, CB164
XC4010E	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160	PG191, CB196
XC4013E	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192	PG223, CB228
XC4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256	PG299, CB228

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

XC4000E Switching Characteristics

XC4000E Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C

Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000E Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_C = -55°C to +125°C		4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
T_{IN}	Input signal transition time			250	ns

Note: At case temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output Measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.
All specifications are subject to change without notice.

XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)			50	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)			16	pF
I_{RIN*}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		-0.02	-0.25	mA
I_{RLL*}	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with the development system Tie option.
* Characterized Only.

XC4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

		Speed Grade	-4	
Description	**Symbol**	**Device**	**Max**	**Units**
From pad through Primary buffer, to any clock K	T_{PG}	XC4005E	7.0	ns
		XC4010E	11.0	ns
		XC4013E	11.5	ns
		XC4025E	12.5	ns
From pad through Secondary buffer, to any clock K	T_{SG}	XC4005E	7.5	ns
		XC4010E	11.5	ns
		XC4013E	12.0	ns
		XC4025E	13.0	ns

XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	
Description	**Symbol**	**Device**	**Max**	**Units**
TBUF driving a Horizontal Longline (LL):				
I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XC4005E XC4010E XC4013E XC4025E	5.0 8.0 9.0 11.0	ns ns ns ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XC4005E XC4010E XC4013E XC4025E	6.0 10.5 11.0 12.0	ns ns ns ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XC4005E XC4010E XC4013E XC4025E	7.0 8.5 8.7 11.0	ns ns ns ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	XC4005E XC4010E XC4013E XC4025E	1.8 3.0 3.5 4.0	ns ns ns ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 1)	T_{PUS}	XC4005E XC4010E XC4013E XC4025E	23.0 29.0 32.0 42.0	ns ns ns ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XC4005E XC4010E XC4013E XC4025E	10.0 13.5 15.0 18.0	ns ns ns ns

Note 1: These values include a minimum load. Use the static timing analyzer to determine the delay for each destination.

XC4000E Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	
Description	**Symbol**	**Device**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4005E	9.5	ns
		XC4010E	15.0	ns
		XC4013E	16.0	ns
		XC4025E	18.0	ns
Full length, both pull-ups, inputs from internal logic	T_{WAFL}	XC4005E	12.5	ns
		XC4010E	18.0	ns
		XC4013E	19.0	ns
		XC4025E	21.0	ns
Half length, one pull-up, inputs from IOB I-pins	T_{WAO}	XC4005E	10.5	ns
		XC4010E	16.0	ns
		XC4013E	17.0	ns
		XC4025E	19.0	ns
Half length, one pull-up, inputs from internal logic	T_{WAOL}	XC4005E	12.5	ns
		XC4010E	18.0	ns
		XC4013E	19.0	ns
		XC4025E	21.0	ns

Notes: These delays are specified from the decoder input to the decoder output.
Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

XC4000E CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

	Speed Grade	-4		Units
Description	**Symbol**	**Min**	**Max**	
Combinatorial Delays				
F/G inputs to X/Y outputs	T_{ILO}		3.9	ns
F/G inputs via H to X/Y outputs	T_{IHO}		5.9	ns
C inputs via H to X/Y outputs	T_{HH1O}		4.9	ns
CLB Fast Carry Logic				
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		4.4	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		6.8	ns
Initialization inputs (F1, F3) to COUT	T_{INCY}		2.9	ns
CIN through function generators to X/Y outputs	T_{SUM}		5.0	ns
CIN to COUT, bypass function generators	T_{BYP}		1.0	ns
Sequential Delays				
Clock K to outputs Q	T_{CKO}		5.0	ns
Setup Time before Clock K				
F/G inputs	T_{ICK}	4.0		ns
F/G inputs via H	T_{IHCK}	6.1		ns
C inputs via H1 through H	T_{HH1CK}	5.0		ns
C inputs via H2 through H	T_{HH2CK}	4.8		ns
C inputs via DIN	T_{DICK}	3.0		ns
C inputs via EC	T_{ECCK}	4.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	4.2		ns

XC4000E CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the static timing analyzer and used in the simulator.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

		Speed Grade	-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	
Hold Time after Clock K					
F/G inputs	T_{CKI}		0		ns
F/G inputs via H	T_{CKIH}		0		ns
C inputs via H1 through H	T_{CKHH1}		0		ns
C inputs via DIN	T_{CKDI}		0		ns
C inputs via EC	T_{CKEC}		0		ns
C inputs via SR, going Low (inactive)	T_{CKR}		0		ns
Clock					
Clock High time	T_{CH}		4.5		ns
Clock Low time	T_{CL}		4.5		ns
Set/Reset Direct					
Width (High)	T_{RPW}		5.5		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}			6.5	ns
Master Set/Reset					
Width (High or Low)	T_{MRW}	4005E	13.0		ns
		4010E	55.0		ns
		4013E	70.0		ns
		4025E	112.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}	4005E		23.0	ns
		4010E		60.0	ns
		4013E		77.0	ns
		4025E		134.0	ns

XC4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

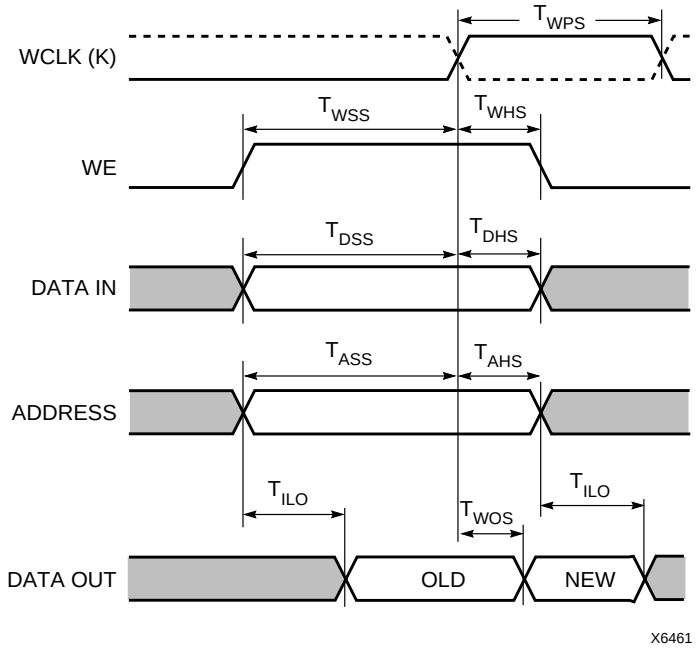
Single Port RAM	**Speed Grade**		**-4**		**Units**
	Size	**Symbol**	**Min**	**Max**	
Write Operation					
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	15.0 15.0		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	7.5 7.5	1 ms 1 ms	ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	2.8 2.8		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0 0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	3.5 2.5		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0 0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	2.2 2.2		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0 0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		10.3 11.6	ns ns

Notes: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Applicable Read timing specifications are identical to Level-Sensitive Read timing.

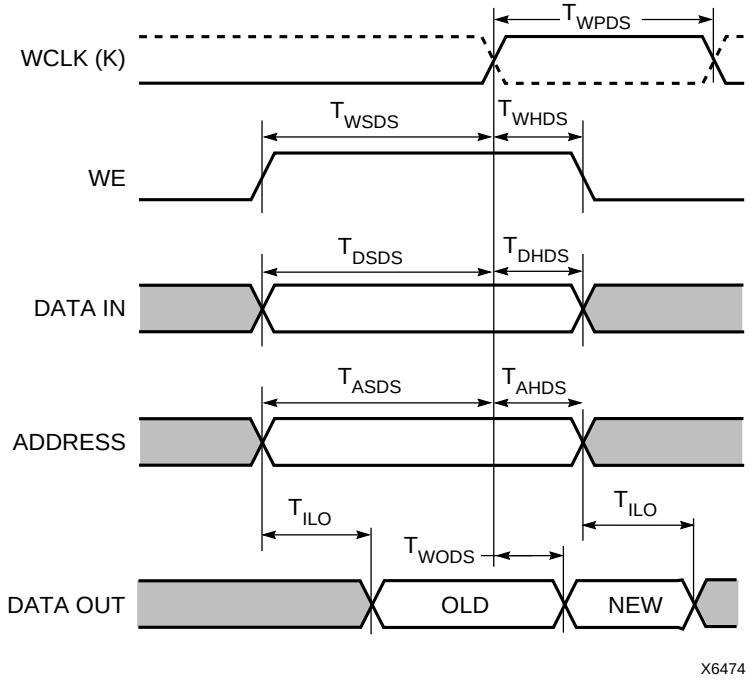
Dual-Port RAM	**Speed Grade**		**-4**		**Units**
	Size	**Symbol**	**Min**	**Max**	
Write Operation					
Address write cycle time (clock K period)	16x1	T_{WCDS}	15.0		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	7.5	1 ms	ns
Address setup time before clock K	16x1	T_{ASDS}	2.8		ns
Address hold time after clock K	16x1	T_{AHDS}	0		ns
DIN setup time before clock K	16x1	T_{DSDS}	2.2		ns
DIN hold time after clock K	16x1	T_{DHDS}	0		ns
WE setup time before clock K	16x1	T_{WSDS}	2.2		ns
WE hold time after clock K	16x1	T_{WHDS}	0.3		ns
Data valid after clock K	16x1	T_{WODS}		10.0	ns

Note: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XC4000E CLB RAM Synchronous (Edge-Triggered) Write Timing



XC4000E CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



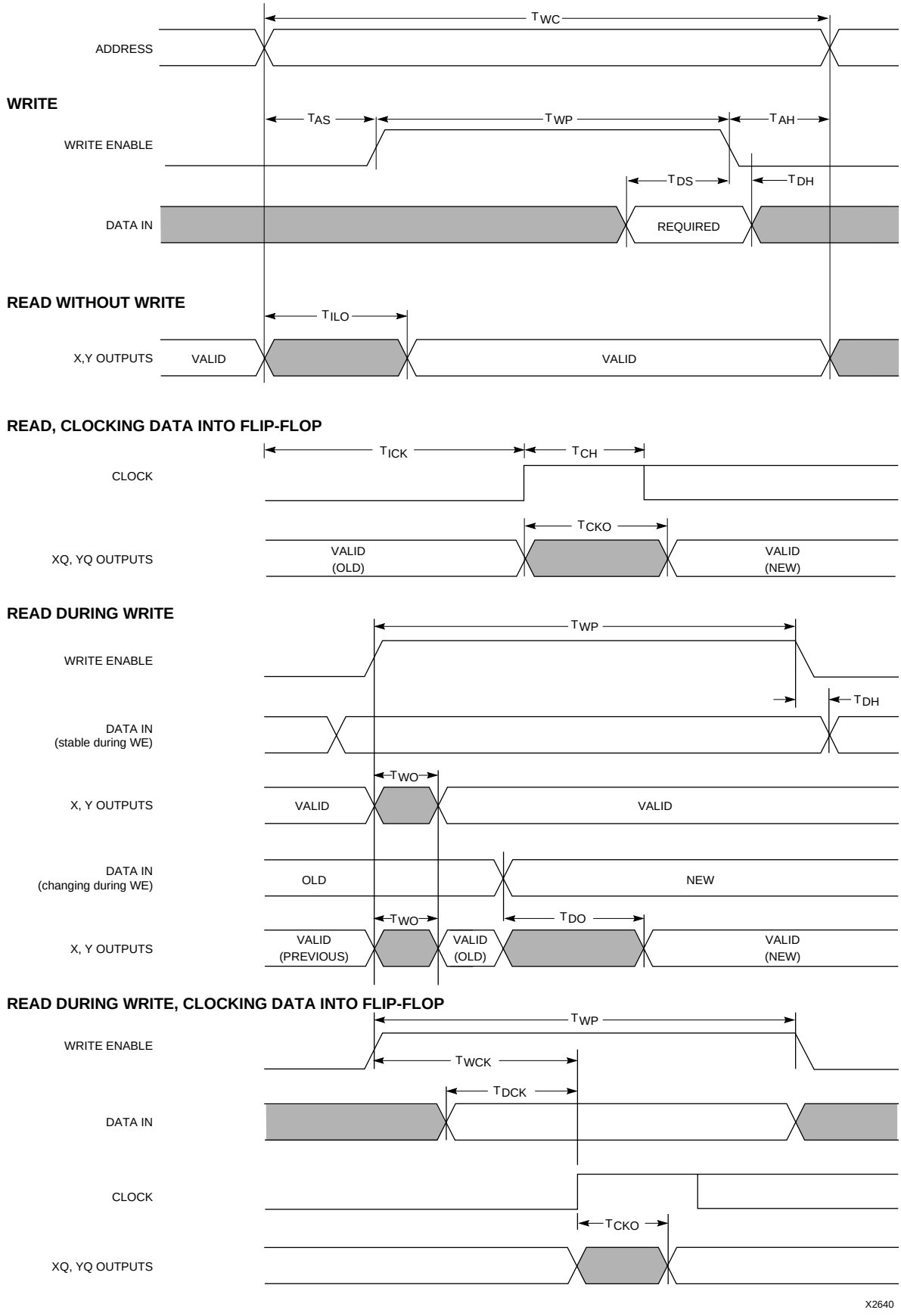
XC4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

		Speed Grade	-4		Units
Description	**Size**	**Symbol**	**Min**	**Max**	
Write Operation					
Address write cycle time	16x2 32x1	T_{WC} T_{WCT}	8.0 8.0		ns ns
Write Enable pulse width (High)	16x2 32x1	T_{WP} T_{WPT}	4.0 4.0		ns ns
Address setup time before WE	16x2 32x1	T_{AS} T_{AST}	2.0 2.0		ns ns
Address hold time after end of WE	16x2 32x1	T_{AH} T_{AHT}	2.5 2.0		ns ns
DIN setup time before end of WE	16x2 32x1	T_{DS} T_{DST}	4.0 5.0		ns ns
DIN hold time after end of WE	16x2 32x1	T_{DH} T_{DHT}	2.0 2.0		ns ns
Read Operation					
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	4.5 6.5		ns ns
Data valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		3.9 5.9	ns ns
Read Operation, Clocking Data into Flip-Flop					
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	4.0 6.1		ns ns
Read During Write					
Data valid after WE goes active (DIN stable before WE)	16x2 32x1	T_{WO} T_{WOT}		10.0 12.0	ns ns
Data valid after DIN (DIN changes during WE)	16x2 32x1	T_{DO} T_{DOT}		9.0 11.0	ns ns
Read During Write, Clocking Data into Flip-Flop					
WE setup time before clock K	16x2 32x1	T_{WCK} T_{WCKT}	8.0 9.6		ns ns
Data setup time before clock K	16x2 32x1	T_{DCK} T_{DCKT}	7.0 8.0		ns ns

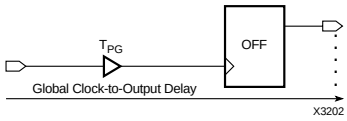
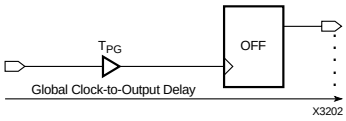
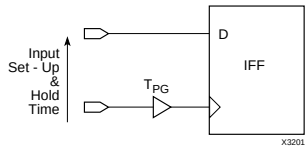
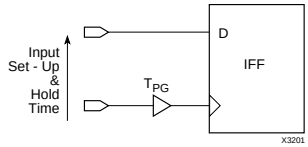
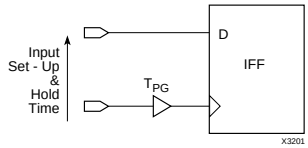
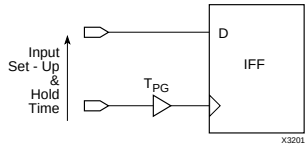
Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XC4000E CLB Level-Sensitive RAM Timing Characteristics



XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

		Speed Grade	-4	Units
Description	**Symbol**	**Device**		
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4005E XC4010E XC4013E XC4025E	14.0 16.0 16.5 17.0	ns ns ns ns
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XC4005E XC4010E XC4013E XC4025E	18.0 20.0 20.5 21.0	ns ns ns ns
Input Setup Time, using IFF (no delay) 	T_{PSUF} (Min)	XC4005E XC4010E XC4013E XC4025E	2.0 1.9 1.6 1.5	ns ns ns ns
Input Hold Time, using IFF (no delay) 	T_{PHF} (Min)	XC4005E XC4010E XC4013E XC4025E	4.6 6.0 7.0 8.0	ns ns ns ns
Input Setup Time, using IFF (with delay) 	T_{PSU} (Min)	XC4005E XC4010E XC4013E XC4025E	8.5 8.5 8.5 9.5	ns ns ns ns ns ns ns ns
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XC4005E XC4010E XC4013E XC4025E	0 0 0 0	ns ns ns ns

OFF = Output Flip-Flop IFF = Input Flip-Flop or Latch

XC4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000E devices unless otherwise noted.

		Speed Grade	-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	
Propagation Delays (TTL Inputs)					
Pad to I1, I2	T_{PID}	All devices		3.0	ns
Pad to I1, I2 via transparent latch, no delay	T_{PLI}	All devices		6.0	ns
with delay	T_{PDLI}	XC4005E		12.0	ns
		XC4010E		12.2	ns
		XC4013E		12.6	ns
		XC4025E		15.0	ns
Propagation Delays					
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		6.8	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		7.3	ns
Hold Times (Note 1)					
Pad to Clock (IK), no delay	T_{IKPI}	All devices	0		ns
with delay	T_{IKPID}	All devices	0		ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

		Speed Grade	-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	
Setup Times (TTL Inputs)					
Pad to Clock (IK), no delay	T_{PICK}	All devices	4.0		ns
with delay	T_{PICKD}	XC4005E	10.9		ns
		XC4010E	11.3		ns
		XC4013E	11.8		ns
		XC4025E	14.0		ns
					ns
					ns
					ns
					ns
(TTL or CMOS)					
Clock Enable (EC) to Clock (IK), no delay					
with delay	T_{ECIK}	All devices	3.5		ns
	T_{ECIKD}	XC4005E	10.4		ns
		XC4010E	10.7		ns
		XC4013E	11.1		ns
		XC4025E	14.0		ns
Global Set/Reset (Note 3)					
Delay from GSR net through Q to I1, I2	T_{RRI}	XC4005E		12.0	ns
GSR width		XC4010E		21.0	ns
GSR inactive to first active Clock (IK) edge		XC4013E		23.0	ns
		XC4025E		29.0	ns
	T_{MRW}	XC4005E	13.0		ns
		XC4010E	55.0		ns
		XC4013E	70.0		ns
		XC4025E	112.0		ns
	T_{RPO}	XC4005E		15.0	ns
		XC4010E		20.3	ns
		XC4013E		22.0	ns
		XC4025E		28.0	ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the static timing analyzer.

XC4000E IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000E devices unless otherwise noted.

	Speed Grade	-4		Units
Description	**Symbol**	**Min**	**Max**	
Propagation Delays (TTL Output Levels)				
Clock (OK) to Pad, fast	T_{OKPOF}		7.5	ns
slew-rate limited	T_{OKPOS}		11.5	ns
Output (O) to Pad, fast	T_{OPF}		8.0	ns
slew-rate limited	T_{OPS}		12.0	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}		10.0	ns
3-state to Pad active and valid, fast	T_{TSONF}		10.0	ns
slew-rate limited	T_{TSONS}		13.7	ns

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000E devices unless otherwise noted.

		Speed Grade	-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	
Setup and Hold					
Output (O) to clock (OK) setup time	T_{OOK}		5.0		ns
Output (O) to clock (OK) hold time	T_{OKO}		0		ns
Clock					
Clock High	T_{CH}		4.5		ns
Clock Low	T_{CL}		4.5		ns

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the static timing analyzer.

Device-Specific Pinout Tables

Pin Locations for XC4005E Devices

XC4005E Pad Name	PG 156†	CB 164	Bndry Scan
VCC	H3	P145	-
I/O (A8)	H1	P146	44
I/O (A9)	G1	P147	47
I/O	G2	P148	50
I/O	G3	P149	53
I/O (A10)	F1	P150	56
I/O (A11)	F2	P151	59
I/O	E1	P152	62
I/O	E2	P153	65
GND	F3	P154	-
I/O (A12)	E3	P157	68
I/O (A13)	C1	P158	71
I/O	C2	P160	74
I/O	D3	P161	77
I/O (A14)	B1	P162	80
I/O, SGCK1 (A15)	B2	P163	83
VCC	C3	P164	-
GND	C4	P1	-
I/O, PGCK1 (A16)	B3	P2	86
I/O (A17)	A1	P3	89
I/O	A2	P4	92
I/O	C5	P5	95
I/O, TDI	B4	P7	98
I/O, TCK	A3	P8	101
GND	C6	P10	-
I/O	B5	P11	104
I/O	B6	P12	107
I/O, TMS	A5	P13	110
I/O	C7	P14	113
I/O	B7	P15	116
I/O	A6	P16	119
I/O	A7	P17	122
I/O	A8	P18	125
GND	C8	P19	-
VCC	B8	P20	-
I/O	C9	P21	128
I/O	B9	P22	131
I/O	A9	P23	134
I/O	B10	P24	137
I/O	C10	P26	140
I/O	A10	P27	143
I/O	A11	P28	146
I/O	B11	P29	149
GND	C11	P30	-
I/O	B12	P32	152
I/O	A13	P33	155
I/O	A14	P34	158
I/O	C12	P35	161
I/O	B13	P37	164
I/O, SGCK2	B14	P38	167
O (M1)	A15	P39	170
GND	C13	P40	-
I (M0)	A16	P41	173
VCC	C14	P42	-
I (M2)	B15	P43	174
I/O, PGCK2	B16	P44	175
I/O (HDC)	D14	P45	178
I/O	C15	P46	181
I/O	D15	P48	184
I/O	E14	P49	187
I/O ($\overline{LDC}$)	C16	P50	190
GND	F14	P53	-
I/O	F15	P54	193
I/O	E16	P55	196
I/O	F16	P56	199
I/O	G14	P57	202
I/O	G15	P58	205
I/O	G16	P59	208
I/O	H16	P60	211
I/O ($\overline{INIT}$)	H15	P61	214
VCC	H14	P62	-
GND	J14	P63	-
I/O	J15	P64	217
I/O	J16	P65	220
I/O	K16	P66	223
I/O	K15	P67	226
I/O	K14	P68	229
I/O	L16	P69	232
I/O	M16	P70	235
I/O	L15	P71	238
GND	L14	P72	-
I/O	P16	P75	241
I/O	M14	P76	244
I/O	N15	P77	247
I/O	P15	P78	250
I/O	N14	P79	253
I/O, SGCK3	R16	P80	256
GND	P14	P81	-
DONE	R15	P82	-
VCC	P13	P83	-
$\overline{PROGRAM}$	R14	P84	-
I/O (D7)	T16	P85	259
I/O, PGCK3	T15	P86	262
I/O	R13	P87	265
I/O	P12	P89	268
I/O (D6)	T14	P90	271
I/O	T13	P91	274
GND	P11	P94	-
I/O	R11	P95	277
I/O	T11	P96	280
I/O (D5)	T10	P97	283
I/O ($\overline{CS0}$)	P10	P98	286
I/O	R10	P99	289
I/O	T9	P100	292
I/O (D4)	R9	P101	295
I/O	P9	P102	298
VCC	R8	P103	-
GND	P8	P104	-
I/O (D3)	T8	P105	301
I/O ($\overline{RS}$)	T7	P106	304
I/O	T6	P107	307
I/O	R7	P108	310
I/O (D2)	P7	P109	313
I/O	T5	P110	316
I/O	R6	P111	319
I/O	T4	P112	322
GND	P6	P113	-
I/O (D1)	T3	P115	325
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	P5	P116	328
I/O	R4	P117	331
I/O	R3	P119	334
I/O (D0, DIN)	P4	P120	337
I/O, SGCK4 (DOUT)	T2	P121	340
CCLK	R2	P122	-
VCC	P3	P123	-
O, TDO	T1	P124	0
GND	N3	P125	-
I/O (A0, $\overline{WS}$)	R1	P126	2
I/O, PGCK4 (A1)	P2	P127	5
I/O	N2	P128	8
I/O	M3	P130	11
I/O (CS1, A2)	P1	P131	14
I/O (A3)	N1	P132	17
GND	L3	P135	-
I/O	L2	P136	20
I/O	L1	P137	23
I/O (A4)	K3	P138	26
I/O (A5)	K2	P139	29
I/O	K1	P140	32
I/O	J1	P141	35
I/O (A6)	J2	P142	38
I/O (A7)	J3	P143	41
GND	H2	P144	-

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Additional XC4005E Package Pins

PG156

N.C. Pins			
A4	A12	D1	D2
D16	E15	M1	M2
M15	N16	R5	R12
T12	-	-	-

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CB164

N.C. Pins			
P6	P9	P25	P31
P36	P47	P51	P52
P73	P74	P88	P92
P93	P114	P118	P129
P133	P134	P155	P156
P159	-	-	-

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Pin Locations for XC4010E Devices

XC4010E Pad Name	PG 191†	CB 196	Bndry Scan
VCC	J4	P183	-
I/O (A8)	J3	P184	62
I/O (A9)	J2	P185	65
I/O (19)	J1	P186	68
I/O (18)	H1	P187	71
I/O	H2	P188	74
I/O	H3	P189	77
I/O (A10)	G1	P190	80
I/O (A11)	G2	P191	83
I/O	F1	P192	86
I/O	E1	P193	89
GND	G3	P194	-
I/O	F2	P195	92
I/O	D1	P196	95
I/O	C1	P197	98
I/O	E2	P198	101
I/O (A12)	F3	P199	104
I/O (A13)	D2	P200	107
I/O	B1	P201	110
I/O	E3	P202	113
I/O (A14)	C2	P203	116
I/O, SGCK1 (A15)	B2	P204	119
VCC	D3	P205	-
GND	D4	P1	-
I/O, PGCK1 (A16)	C3	P2	122
I/O (A17)	C4	P3	125
I/O	B3	P4	128
I/O	C5	P6	131
I/O, TDI	A2	P7	134
I/O, TCK	B4	P8	137
I/O	C6	P9	140
I/O	A3	P10	143
I/O	B5	P11	146
I/O	B6	P12	149
GND	C7	P13	-
I/O	A4	P14	152
I/O	A5	P15	155
I/O, TMS	B7	P16	158
I/O	A6	P17	161
I/O	C8	P18	164
I/O	A7	P19	167
I/O	B8	P20	170
I/O	A8	P21	173
I/O	B9	P22	176
I/O	C9	P23	179
GND	D9	P24	-
VCC	D10	P25	-
I/O	C10	P26	182
I/O	B10	P27	185
I/O	A9	P28	188
I/O	A10	P29	191
I/O	A11	P30	194
I/O	C11	P31	197
I/O	B11	P32	200
I/O	A12	P33	203
I/O	B12	P34	206
I/O	A13	P35	209
GND	C12	P36	-
I/O	B13	P37	212
I/O	A14	P38	215
I/O	A15	P39	218
I/O	C13	P40	221

XC4010E Pad Name	PG 191†	CB 196	Bndry Scan
I/O	B14	P41	224
I/O	A16	P42	227
I/O	B15	P43	230
I/O	C14	P44	233
I/O	A17	P45	236
I/O, SGCK2	B16	P46	239
O (M1)	C15	P47	242
GND	D15	P48	-
I (M0)	A18	P49	245
VCC	D16	P50	-
I (M2)	C16	P51	246
I/O, PGCK2	B17	P52	247
I/O (HDC)	E16	P53	250
I/O	C17	P55	253
I/O	D17	P56	256
I/O	B18	P57	259
I/O ($\overline{\text{LDC}}$)	E17	P58	262
I/O	F16	P59	265
I/O	C18	P60	268
I/O	D18	P61	271
I/O	F17	P62	274
GND	G16	P63	-
I/O	E18	P64	277
I/O	F18	P65	280
I/O	G17	P66	283
I/O	G18	P67	286
I/O	H16	P68	289
I/O	H17	P69	292
I/O	H18	P70	295
I/O	J18	P71	298
I/O	J17	P72	301
I/O ($\overline{\text{INIT}}$)	J16	P73	304
VCC	J15	P74	-
GND	K15	P75	-
I/O	K16	P76	307
I/O	K17	P77	310
I/O	K18	P78	313
I/O	L18	P79	316
I/O	L17	P80	319
I/O	L16	P81	322
I/O	M18	P82	325
I/O	M17	P83	328
I/O	N18	P84	331
I/O	P18	P85	334
GND	M16	P86	-
I/O	N17	P87	337
I/O	R18	P88	340
I/O	T18	P89	343
I/O	P17	P90	346
I/O	N16	P91	349
I/O	T17	P92	352
I/O	R17	P93	355
I/O	P16	P94	358
I/O	U18	P95	361
I/O, SGCK3	T16	P96	364
GND	R16	P97	-
DONE	U17	P98	-
VCC	R15	P99	-
$\overline{\text{PROGRAM}}$	V18	P100	-
I/O (D7)	T15	P101	367
I/O, PGCK3	U16	P102	370
I/O	T14	P104	373

XC4010E Pad Name	PG 191†	CB 196	Bndry Scan
I/O	U15	P105	376
I/O (D6)	V17	P106	379
I/O	V16	P107	382
I/O	T13	P108	385
I/O	U14	P109	388
I/O	V15	P110	391
I/O	V14	P111	394
GND	T12	P112	-
I/O	U13	P113	397
I/O	V13	P114	400
I/O (D5)	U12	P115	403
I/O ($\overline{\text{CS0}}$)	V12	P116	406
I/O	T11	P117	409
I/O	U11	P118	412
I/O	V11	P119	415
I/O	V10	P120	418
I/O (D4)	U10	P121	421
I/O	T10	P122	424
VCC	R10	P123	-
GND	R9	P124	-
I/O (D3)	T9	P125	427
I/O ($\overline{\text{RS}}$)	U9	P126	430
I/O	V9	P127	433
I/O	V8	P128	436
I/O	U8	P129	439
I/O	T8	P130	442
I/O (D2)	V7	P131	445
I/O	U7	P132	448
I/O	V6	P133	451
I/O	U6	P134	454
GND	T7	P135	-
I/O	V5	P136	457
I/O	V4	P137	460
I/O	U5	P138	463
I/O	T6	P139	466
I/O (D1)	V3	P140	469
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	V2	P141	472
I/O	U4	P142	475
I/O	T5	P143	478
I/O (D0, DIN)	U3	P144	481
I/O, SGCK4 (DOUT)	T4	P145	484
CCLK	V1	P146	-
VCC	R4	P147	-
O, TDO	U2	P148	0
GND	R3	P149	-
I/O (A0, $\overline{\text{WS}}$)	T3	P150	2
I/O, PGCK4 (A1)	U1	P151	5
I/O	P3	P153	8
I/O	R2	P154	11
I/O (CS1, A2)	T2	P155	14
I/O (A3)	N3	P156	17
I/O	P2	P157	20
I/O	T1	P158	23
I/O	R1	P159	26
I/O	N2	P160	29
GND	M3	P161	-
I/O	P1	P162	32
I/O	N1	P163	35
I/O (A4)	M2	P164	38
I/O (A5)	M1	P165	41
I/O	L3	P166	44

XC4010E Pad Name	PG 191†	CB 196	Bndry Scan
I/O	L2	P167	47
I/O	L1	P168	50
I/O	K1	P169	53
I/O (A6)	K2	P170	56
I/O (A7)	K3	P171	59
GND	K4	P172	-

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Additional XC4010E Package Pins

CB196

N.C. Pins			
P5	P54	P103	P152
P192	-	-	-

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Pin Locations for XC4013E Devices

XC4013E Pad Name	PG 223†	CB 228	Bndry Scan
VCC	J4	P201	-
I/O (A8)	J3	P202	74
I/O (A9)	J2	P203	77
I/O	J1	P204	80
I/O	H1	P205	83
I/O	H2	P206	86
I/O	H3	P207	89
I/O (A10)	G1	P208	92
I/O (A11)	G2	P209	95
VCC	-	P210	-
I/O	H4	P211	98
I/O	G4	P212	101
I/O	F1	P213	104
I/O	E1	P214	107
GND	G3	P215	-
I/O	F2	P216	110
I/O	D1	P217	113
I/O	C1	P218	116
I/O	E2	P219	119
I/O (A12)	F3	P220	122
I/O (A13)	D2	P221	125
I/O	F4	P222	128
I/O	E4	P223	131
I/O	B1	P224	134
I/O	E3	P225	137
I/O (A14)	C2	P226	140
I/O, SGCK1 (A15)	B2	P227	143
VCC	D3	P228	-
GND	D4	P1	-
I/O, PGCK1(A16)	C3	P2	146
I/O (A17)	C4	P3	149
I/O	B3	P4	152
I/O	C5	P5	155
I/O, TDI	A2	P6	158
I/O, TCK	B4	P7	161
I/O	C6	P8	164
I/O	A3	P9	167
I/O	B5	P10	170
I/O	B6	P11	173
I/O	D5	P12	176
I/O	D6	P13	179
GND	C7	P14	-
I/O	A4	P15	182
I/O	A5	P16	185
I/O, TMS	B7	P17	188
I/O	A6	P18	191
I/O	D7	P19	194
I/O	D8	P20	197
I/O	C8	P21	200
I/O	A7	P22	203
I/O	B8	P23	206
I/O	A8	P24	209
I/O	B9	P25	212
I/O	C9	P26	215
GND	D9	P27	-
VCC	D10	P28	-
I/O	C10	P29	218
I/O	B10	P30	221
I/O	A9	P31	224
I/O	A10	P32	227
I/O	A11	P33	230
I/O	C11	P34	233
I/O	D11	P35	236
I/O	D12	P36	239
VCC	-	P37	-
I/O	B11	P38	242
I/O	A12	P39	245
I/O	B12	P40	248
I/O	A13	P41	251
GND	C12	P42	-
I/O	D13	P43	254
I/O	D14	P44	257
I/O	B13	P45	260
I/O	A14	P46	263
I/O	A15	P47	266
I/O	C13	P48	269
I/O	B14	P49	272
I/O	A16	P50	275
I/O	B15	P51	278
I/O	C14	P52	281
I/O	A17	P53	284
I/O, SGCK2	B16	P54	287
O (M1)	C15	P55	290
GND	D15	P56	-
I (M0)	A18	P57	293
VCC	D16	P58	-
I (M2)	C16	P59	294
I/O, PGCK2	B17	P60	295
I/O (HDC)	E16	P61	298
I/O	C17	P62	301
I/O	D17	P63	304
I/O	B18	P64	307
I/O ($\overline{\text{LDC}}$)	E17	P65	310
I/O	F16	P66	313
I/O	C18	P67	316
I/O	D18	P68	319
I/O	F17	P69	322
I/O	E15	P70	325
I/O	F15	P71	328
GND	G16	P72	-
I/O	E18	P73	331
I/O	F18	P74	334
I/O	G17	P75	337
I/O	G18	P76	340
I/O	H16	P77	343
I/O	H17	P78	346
I/O	G15	P79	349
I/O	H15	P80	352
I/O	H18	P81	355
I/O	J18	P82	358
I/O	J17	P83	361
I/O ($\overline{\text{INIT}}$)	J16	P84	364
VCC	J15	P85	-
GND	K15	P86	-
I/O	K16	P87	367
I/O	K17	P88	370
I/O	K18	P89	373
I/O	L18	P90	376
I/O	L17	P91	379
I/O	L16	P92	382
I/O	L15	P93	385
I/O	M15	P94	388
VCC	-	P95	-
I/O	M18	P96	391
I/O	M17	P97	394
I/O	N18	P98	397
I/O	P18	P99	400
GND	M16	P100	-
I/O	N15	P101	403
I/O	P15	P102	406
I/O	N17	P103	409
I/O	R18	P104	412
I/O	T18	P105	415
I/O	P17	P106	418
I/O	N16	P107	421
I/O	T17	P108	424
I/O	R17	P109	427
I/O	P16	P110	430
I/O	U18	P111	433
I/O, SGCK3	T16	P112	436
GND	R16	P113	-
DONE	U17	P114	-
VCC	R15	P115	-
$\overline{\text{PROGRAM}}$	V18	P116	-
I/O (D7)	T15	P117	439
I/O, PGCK3	U16	P118	442
I/O	T14	P119	445
I/O	U15	P120	448
I/O	R14	P121	451
I/O	R13	P122	454
I/O (D6)	V17	P123	457
I/O	V16	P124	460
I/O	T13	P125	463

XC4013E Pad Name	PG 223†	CB 228	Bndry Scan
I/O	U14	P126	466
I/O	V15	P127	469
I/O	V14	P128	472
GND	T12	P129	-
I/O	R12	P130	475
I/O	R11	P131	478
I/O	U13	P132	481
I/O	V13	P133	484
I/O (D5)	U12	P134	487
I/O ($\overline{CS0}$)	V12	P135	490
I/O	T11	P136	493
I/O	U11	P137	496
I/O	V11	P138	499
I/O	V10	P139	502
I/O (D4)	U10	P140	505
I/O	T10	P141	508
VCC	R10	P142	-
GND	R9	P143	-
I/O (D3)	T9	P144	511
I/O ($\overline{RS}$)	U9	P145	514
I/O	V9	P146	517
I/O	V8	P147	520
I/O	U8	P148	523
I/O	T8	P149	526
I/O (D2)	V7	P150	529
I/O	U7	P151	532
VCC	-	P152	-

XC4013E Pad Name	PG 223†	CB 228	Bndry Scan
I/O	V6	P153	535
I/O	U6	P154	538
I/O	R8	P155	541
I/O	R7	P156	544
GND	T7	P157	-
I/O	R6	P158	547
I/O	R5	P159	550
I/O	V5	P160	553
I/O	V4	P161	556
I/O	U5	P162	559
I/O	T6	P163	562
I/O (D1)	V3	P164	565
I/O ($\overline{RCLK}$, RDY/$\overline{BUSY}$)	V2	P165	568
I/O	U4	P166	571
I/O	T5	P167	574
I/O (D0, DIN)	U3	P168	577
I/O, SGCK4 (DOUT)	T4	P169	580
CCLK	V1	P170	-
VCC	R4	P171	-
O, TDO	U2	P172	0
GND	R3	P173	-
I/O (A0, $\overline{WS}$)	T3	P174	2
I/O, PGCK4 (A1)	U1	P175	5
I/O	P3	P176	8
I/O	R2	P177	11

XC4013E Pad Name	PG 223†	CB 228	Bndry Scan
I/O (CS1, A2)	T2	P178	14
I/O (A3)	N3	P179	17
I/O	P4	P180	20
I/O	N4	P181	23
I/O	P2	P182	26
I/O	T1	P183	29
I/O	R1	P184	32
I/O	N2	P185	35
GND	M3	P186	-
I/O	P1	P187	38
I/O	N1	P188	41
I/O	M4	P189	44
I/O	L4	P190	47
VCC	-	P191	-
I/O (A4)	M2	P192	50
I/O (A5)	M1	P193	53
I/O	L3	P194	56
I/O	L2	P195	59
I/O	L1	P196	62
I/O	K1	P197	65
I/O (A6)	K2	P198	68
I/O (A7)	K3	P199	71
GND	K4	P200	-

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Pin Locations for XC4025E Devices

XC4025E Pad Name	CB 228	PG 299	Bndry Scan
VCC	P201	K1	-
I/O (A8)	P202	K2	98
I/O (A9)	P203	K3	101
I/O	P204	K5	104
I/O	P205	K4	107
I/O	P206	J1	110
I/O	P207	J2	113
I/O (A10)	P208	H1	116
I/O (A11)	P209	J3	119
I/O	-	J4	122
I/O	-	J5	125
I/O	-	H2	128
I/O	-	G1	131
VCC	P210	E1	-
I/O	P211	H3	134
I/O	P212	G2	137
I/O	P213	H4	140
I/O	P214	F2	143
GND	P215	F1	-
I/O	-	H5	146
I/O	-	G3	149
I/O	P216	D1	152
I/O	P217	G4	155
I/O	P218	E2	158
I/O	P219	F3	161
I/O (A12)	P220	G5	164
I/O (A13)	P221	C1	167
I/O	-	F4	170
I/O	-	E3	173
I/O	P222	D2	176

XC4025E Pad Name	CB 228	PG 299	Bndry Scan
I/O	P223	C2	179
I/O	P224	F5	182
I/O	P225	E4	185
I/O (A14)	P226	D3	188
I/O, SGCK1 (A15)	P227	C3	191
VCC	P228	A2	-
GND	P1	B1	-
I/O, PGCK1 (A16)	P2	D4	194
I/O (A17)	P3	B2	197
I/O	P4	B3	200
I/O	P5	E6	203
I/O, TDI	P6	D5	206
I/O, TCK	P7	C4	209
I/O	-	A3	212
I/O	-	D6	215
I/O	P8	E7	218
I/O	P9	B4	221
I/O	P10	C5	224
I/O	P11	A4	227
I/O	P12	D7	230
I/O	P13	C6	233
I/O	-	E8	236
I/O	-	B5	239
GND	P14	A5	-
I/O	P15	B6	242
I/O	P16	D8	245
I/O, TMS	P17	C7	248
I/O	P18	B7	251
VCC	-	A6	-
I/O	-	C8	254

XC4025E Pad Name	CB 228	PG 299	Bndry Scan
I/O	-	E9	257
I/O	-	A7	260
I/O	-	D9	263
I/O	P19	B8	266
I/O	P20	A8	269
I/O	P21	C9	272
I/O	P22	B9	275
I/O	P23	E10	278
I/O	P24	A9	281
I/O	P25	D10	284
I/O	P26	C10	287
GND	P27	A10	-
VCC	P28	A11	-
I/O	P29	B10	290
I/O	P30	B11	293
I/O	P31	C11	296
I/O	P32	E11	299
I/O	P33	D11	302
I/O	P34	A12	305
I/O	-	B12	308
I/O	-	A13	311
I/O	-	C12	314
I/O	-	D12	317
I/O	P35	E12	320
I/O	P36	B13	323
VCC	P37	A16	-
I/O	P38	A14	326
I/O	P39	C13	329
I/O	P40	B14	332
I/O	P41	D13	335

XC4025E Pad Name	CB 228	PG 299	Bndry Scan
GND	P42	A15	-
I/O	-	B15	338
I/O	-	E13	341
I/O	P43	C14	344
I/O	P44	A17	347
I/O	P45	D14	350
I/O	P46	B16	353
I/O	P47	C15	356
I/O	P48	E14	359
I/O	-	A18	362
I/O	-	D15	365
I/O	P49	C16	368
I/O	P50	B17	371
I/O	P51	B18	374
I/O	P52	E15	377
I/O	P53	D16	380
I/O, SGCK2	P54	C17	383
O (M1)	P55	A20	386
GND	P56	A19	-
I (M0)	P57	C18	389
VCC	P58	B20	-
I (M2)	P59	D17	390
I/O, PGCK2	P60	B19	391
I/O (HDC)	P61	C19	394
I/O	P62	F16	397
I/O	P63	E17	400
I/O	P64	D18	403
I/O ($\overline{\text{LDC}}$)	P65	C20	406
I/O	-	F17	409
I/O	-	G16	412
I/O	P66	D19	415
I/O	P67	E18	418
I/O	P68	D20	421
I/O	P69	G17	424
I/O	P70	F18	427
I/O	P71	H16	430
I/O	-	E19	433
I/O	-	F19	436
GND	P72	E20	-
I/O	P73	H17	439
I/O	P74	G18	442
I/O	P75	G19	445
I/O	P76	H18	448
VCC	-	VCC*	-
I/O	P77	J16	451
I/O	P78	G20	454
I/O	-	J17	457
I/O	-	H19	460
I/O	-	H20	463
I/O	-	J18	466
I/O	P79	J19	469
I/O	P80	K16	472
I/O	P81	J20	475
I/O	P82	K17	478
I/O	P83	K18	481
I/O ($\overline{\text{INIT}}$)	P84	K19	484
VCC	P85	L20	-
GND	P86	K20	-
I/O	P87	L19	487
I/O	P88	L18	490
I/O	P89	L16	493
I/O	P90	L17	496
I/O	P91	M20	499
I/O	P92	M19	502

XC4025E Pad Name	CB 228	PG 299	Bndry Scan
I/O	-	N20	505
I/O	-	M18	508
I/O	-	M17	511
I/O	-	M16	514
I/O	P93	N19	517
I/O	P94	P20	520
VCC	P95	T20	-
I/O	P96	N18	523
I/O	P97	P19	526
I/O	P98	N17	529
I/O	P99	R19	532
GND	P100	R20	-
I/O	-	N16	535
I/O	-	P18	538
I/O	P101	U20	541
I/O	P102	P17	544
I/O	P103	T19	547
I/O	P104	R18	550
I/O	P105	P16	553
I/O	P106	V20	556
I/O	-	R17	559
I/O	-	T18	562
I/O	P107	U19	565
I/O	P108	V19	568
I/O	P109	R16	571
I/O	P110	T17	574
I/O	P111	U18	577
I/O, SGCK3	P112	X20	580
GND	P113	W20	-
DONE	P114	V18	-
VCC	P115	X19	-
$\overline{\text{PROGRAM}}$	P116	U17	-
I/O (D7)	P117	W19	583
I/O, PGCK3	P118	W18	586
I/O	P119	T15	589
I/O	P120	U16	592
I/O	P121	V17	595
I/O	P122	X18	598
I/O	-	U15	601
I/O	-	T14	604
I/O (D6)	P123	W17	607
I/O	P124	V16	610
I/O	P125	X17	613
I/O	P126	U14	616
I/O	P127	V15	619
I/O	P128	T13	622
I/O	-	W16	625
I/O	-	W15	628
GND	P129	X16	-
I/O	P130	U13	631
I/O	P131	V14	634
I/O	P132	W14	637
I/O	P133	V13	640
VCC	-	X15	-
I/O (D5)	P134	T12	643
I/O ($\overline{\text{CS0}}$)	P135	X14	646
I/O	-	U12	649
I/O	-	W13	652
I/O	-	X13	655
I/O	-	V12	658
I/O	P136	W12	661
I/O	P137	T11	664
I/O	P138	X12	667
I/O	P139	U11	670

XC4025E Pad Name	CB 228	PG 299	Bndry Scan
I/O (D4)	P140	V11	673
I/O	P141	W11	676
VCC	P142	X10	-
GND	P143	X11	-
I/O (D3)	P144	W10	679
I/O ($\overline{\text{RS}}$)	P145	V10	682
I/O	P146	T10	685
I/O	P147	U10	688
I/O	P148	X9	691
I/O	P149	W9	694
I/O	-	X8	697
I/O	-	V9	700
I/O	-	U9	703
I/O	-	T9	706
I/O (D2)	P150	W8	709
I/O	P151	X7	712
VCC	P152	X5	-
I/O	P153	V8	715
I/O	P154	W7	718
I/O	P155	U8	721
I/O	P156	W6	724
GND	P157	X6	-
I/O	-	T8	727
I/O	-	V7	730
I/O	P158	X4	733
I/O	P159	U7	736
I/O	P160	W5	739
I/O	P161	V6	742
I/O	P162	T7	745
I/O	P163	X3	748
I/O (D1)	P164	U6	751
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P165	V5	754
I/O	-	W4	757
I/O	-	W3	760
I/O	P166	T6	763
I/O	P167	U5	766
I/O (D0, DIN)	P168	V4	769
I/O, SGCK4 (DOUT)	P169	X1	772
CCLK	P170	V3	-
VCC	P171	VCC*	-
O, TDO	P172	U4	0
GND	P173	GND*	-
I/O (A0, $\overline{\text{WS}}$)	P174	W2	2
I/O, PGCK4 (A1)	P175	V2	5
I/O	P176	R5	8
I/O	P177	T4	11
I/O (CS1, A2)	P178	U3	14
I/O (A3)	P179	V1	17
I/O	P180	R4	20
I/O	P181	P5	23
I/O	P182	U2	26
I/O	P183	T3	29
I/O	P184	U1	32
I/O	P185	P4	35
I/O	-	R3	38
I/O	-	N5	41
I/O	-	T2	44
I/O	-	R2	47
GND	P186	T1	-
I/O	P187	N4	50
I/O	P188	P3	53
I/O	P189	P2	56

XC4025E Pad Name	CB 228	PG 299	Bndry Scan
I/O	P190	N3	59
VCC	P191	R1	-
I/O	-	M5	62
I/O	-	P1	65
I/O	-	M4	68
I/O	-	N2	71
I/O (A4)	P192	N1	74
I/O (A5)	P193	M3	77
I/O	P194	M2	80
I/O	P195	L5	83
I/O	P196	M1	86
I/O	P197	L4	89
I/O (A6)	P198	L3	92
I/O (A7)	P199	L2	95
GND	P200	L1	-

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Ordering Information

Example for SMD Part: **5962-97523 01 Q X C**

- **5962** — Generic Standard Microcircuit Drawing (SMD) Prefix
- **97523** — Device Type
  - XC4005E = 97522
  - XC4010E = 97523
  - XC4013E = 97524
  - XC4025E = 97525
- **01** — Speed Grade
  - 01 = -4
- **Q** — QML Certified
- **X** — Package Type
  - X = Pin Grid
  - Y = Quad Flatpack (Base Mark)
  - Z = Quad Flatpack (Lid Mark)
- **C** — Lead Finish
  - C = Gold

Example for Military Tempeture Only Part: **XC4010E -4 PG 191 M**

- **XC4010E** — Device Type
  - XC4005E
  - XC4010E
  - XC4013E
  - XC4025E
- **-4** — Speed Grade
- **PG** — Package Type
  - CB = Top Braxed Ceramic Quad Flat Pack
  - PG = Ceramic Pin Grid Array
- **191** — Number of Pins
- **M** — Temperature Range
  - M = Military (T_C = -55° C to +125° C)