Choosing a Xilinx Product Family

XAPP 100 July 10, 1998 (Version 1.3)

Application Note by Peter Alfke

Summary

This Application Note describes the various Xilinx product families. Differences between the families are highlighted. The focus of the discussion is how to choose the appropriate family for a particular application.

Xilinx Families

Spartan ™, XC3000, XC4000, XC5000, XC9000

Table of Contents

Introduction

Xilinx offers Field-Programmable Logic circuits, mass-produced standard integrated circuits that the user can customize for the specific application.

Xilinx products offer the following advantages:

- High integration (less space, lower power, higher reliability, lower cost) than solutions based on existing standard devices like MSI and PALs.
- No non-recurring engineering charges and associated risk, typically required for mask-programmed gate array solutions.
- Fast design time and easy design modification, important for early time-to-market.
- Designs can be upgraded in the field for added functionality.

Some potential users might be confused by the wide diversity of Xilinx product offerings. This application note provides a broad overview from the user's perspective.

Xilinx offers programmable logic circuits in two distinctly different technologies.

- SRAM-based FPGAs, the original Xilinx offering, now encompassing the Spartan, XC3000, XC4000, and XC5200 series and their sub-families, like the XC3000A, XC3000L, XC3100A, XC4000E, XC4000EX, and XC4000XL.
- Flash-based complex PLDs, the XC9500 family.

SRAM-Based FPGAs

These families represent an ongoing evolution of the original Xilinx FPGA architecture, characterized by structural flexibility and an abundance of flip-flops. Logic is implemented in look-up tables, and is interconnected by a hierarchy of metal lines controlled by pass transistors.

Attractive systems features include on-chip bidirectional busses and individual output 3-state and slew-rate control, common reset for all flip-flops, and multiple global low-skew clock networks.

The configuration can be loaded while the devices are connected into a system, and can be changed an unlimited number of times by reloading the "bitstream," the series of bits used to program the device. Configuration must be reloaded whenever Vcc is re-applied. Reconfiguration takes 20 to 200 ms, during which time all outputs are inactive.

Static power consumption is very low, down to microwatts for some of the families. Dynamic power consumption is proportional to the clock frequency, and depends on the logic activity inside the device and on the outputs.

The description "SRAM-based" refers primarily to the standard high-volume manufacturing process, and secondarily to the fact that configuration data is stored in latches. Different from typical SRAMs, these latches use low-impedance active pull-up and pull-down transistors. An on-chip voltage monitor 3-states the outputs and initiates reconfiguration when Vcc drops significantly (to 3.2 V in a 5V system).

These FPGAs are available in different sizes and many different packages. Usually each device type is available in many package types. Any package can accommodate different sized devices with compatible pinouts, so the user can migrate to a larger or smaller device without changing the PC-board layout.

Overview of SRAM-Based FPGA Families

XC2000: Obsolete, do not use for new designs.

The Spartan FPGA families or the XC9500 CPLD family, may be an alternative.

XC2000L: 3.3V version of XC2000; obsolete, do not use for new designs. Use the SpartanXL family instead.

XC3000: Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible, XC3000A family.

XC3000A: Newest version of the XC3000 family

Five device types cover a complexity range from 1,300 to 7,500 gates, with 256 to 928 flip-flops. Logic is implemented in 4-input look-up tables; two tables can be combined to implement any logic function of five variables with only one combinatorial delay of 4 or 5 ns. Flip-flop toggle rate is over 110 MHz.

Global choice of input thresholds (1.2 V or 2.5V), output slew-rate control, and an on-chip crystal oscillator circuit are attractive system features.

- Use for medium-speed, medium-complexity applications.
- Accept lack of dedicated carry circuits, resulting in less efficient and slower arithmetic and counters than in XC4000 families. No on-chip RAM; data storage is thus limited to the available 256 to 928 flip flops.

XC3000L: 3.3V version of XC3000A

- Use for battery-operated applications.
- Accept significantly slower speed at 3.3V, compared to XC3000A at 5V.

XC3100: Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible XC3100A family.

XC3100A: Newest version of the high-speed XC3100 family.

XC3100A devices are functionally and bitstream identical with the XC3000A, and are available in the same packages with the same pinouts. The only difference is the higher speed of the XC3100A, with a look-up table delay of 1.5 to 4 ns, and the slightly higher standby current of 8 to 14 mA. One additional high-end family member, the XC3195A, can implement up to 9,000 gates and 1,320 flip-flops.

- Use for high performance design with system clock rates up to 100 MHz.
- Accept lack of dedicated carry circuits, resulting in less efficient and possibly slower arithmetic and counters than in XC4000. No on-chip RAM; data storage is thus limited to the available 256 to 1,320 flip-flops.

XC3100L: 3.3V version of XC3100A

- Use for 3.3V applications.
- Accept significantly slower speed at 3.3V, compared to XC3100A at 5V, as well as higher quiescent power and much higher powerdown current than XC3000L at 3.3V.

XC4000: Superseded

Don't use this family for new designs, since it has been superseded by the improved, but fully backwards compatible XC4000E family.

XC4000A: Superseded

Don't use this family for new designs, since it has been superseded by the improved, faster, less expensive, and pinout-compatible – but not bitstream-compatible – XC4000E family.

XC4000H: High I/O - count version of XC4000; obsolete, do not use for new designs.

XC4000E: Enhanced superset of the XC4000 family

The XC4000E family is recommended for new designs.

The ten devices in this family stretch from 2,000 to 25,000 logic gate complexity. The emphasis is on systems features and speed. The function generators are more versatile than in the XC3000-Series parts, and there is a dedicated carry network to speed up arithmetic and counters and make them more efficient. Most importantly, the function generators can be used as user RAM with asynchronous or synchronous write addressing, even as dual-port RAMs. This capability makes register files, shift registers and especially FIFOs faster and much more efficient than in any other FPGA. Dedicated carry logic can speed up wide arithmetic and long counters.

- Use for general-purpose logic and data-path logic that can take advantage of internal busses and fast arithmetic carry logic. Use for on-chip distributed RAMs, e.g. >50-MHz FIFOs up to 64 deep, 32 bits wide.

XC4000EX: Larger version of the XC4000E family.

Extension of the XC4000E family from 28k to 36k logic gates, with greatly increased routing resources, faster clocking options and more versatile output logic.

- Use for designs beyond 20,000 gate complexity.

XC4000XL: 3.3V FPGA

Complete family stretching from 5000 gates to >100,000 gates. Basic features are identical to the XC4000EX but with 5V tolerant input, even when Vcc is <3.0V.

- Use for 3.3V designs, and highest performance.

XC4000XLT: 3.3V FPGA, 5V PCI compatible

The XC4000XLT adds 5V VTT pins to the XC4000XL to enable the positive input signal clamping function required by 5V PCI specifications.

XC4000XV: 2.5V FPGA

SImilar architecture to XC4000EX (5V) and XC4000XL/T (3.3V). Together, these families are referred to as “XC4000X”. The XC4000XV extends the family to the largest FPGAs available, in the 250,000-500,000 system gate range. The XC4000XV family uses 0.25 micron technology, with a 2.5V core supply and a 3.3V I/O supply for 5V compatibility.

Spartan: 5V low-cost FPGA based on XC4000

The Spartan Series of FPGAs is the best high volume FPGA solution for ASIC replacement. Derived from the highly successful XC4000 architecture and spanning up to 40,000 system gates, the Spartan Series combines high performance, on-chip RAM, software cores, and low prices. The Spartan Series is the first FPGA that meets all the key requirements of ASIC designs for high volume production, and delivers unmatched benefits over competing PLDs.

SpartanXL™: 3.3 V version of Spartan FPGA

Similar architecture to 5V Spartan family, but providing higher speed, lower power, and lower cost using smaller process technology. The 5V and 3.3V families are together referred to as the Spartan Series.

XC5200: Low-cost FPGA

Architecture optimized for low cost, good routability, and the ability to lock pinout while internal logic is being modified. Dedicated carry structure similar to XC4000, but no RAM. Four-input function generators avoid the XC3000 input constraints. IOBs are less rigidly coupled to the internal matrix of CLBs and interconnects, which greatly improves the flexibility of pin-locked designs. IOBs have no flip-flops.

Performance is similar to XC3000A, but dedicated carry logic can speed up wide arithmetic and long counters.

- Use for medium-speed general-purpose logic, and for data-path logic that can take advantage of internal busses and fast arithmetic carry logic. Alternative to XC3000A at lower cost, and with additional benefits, such as dedicated carry for arithmetic and counters, improved routing, and ability to cope with locked pinout. High I/O count. Package pinout compatible with XC4000.
- Accept lack of internal RAM.

FLASH-Based CPLDs (XC9500)

These devices are extensions of the popular PAL architecture, implementing logic as wide AND gates, ORed together, driving either a flip-flop or an output directly. The simple logic structure makes these devices easy to understand, and results in both fast design compilation and short pin-to-pin delays. Wide input gating and fast system clock rates up to 150 MHz are attractive features for state machines and complex synchronous counters.

The XC9500 in-system programmable family, based on FLASH technology, eliminates the need for a separate programmer. These new devices also offer boundary scan (JTAG) to simplify board testing.

Overview of CPLD Families

XC7300: Superseded

Do not use for new designs. Use XC9500 instead.

XC9500: FLASH-Based CPLD

Six devices cover the range from 36 to 288 macrocells.

The new XC9500 family provides advanced in-system programming and test capabilities for high performance, general purpose logic integration.

- Delays are deterministic, and compile times are very short.
- Use for high-speed logic, short pin-to-pin delays, for state machines and flexible address decoding, and as PAL replacement.
- Accept higher power consumption and fewer available flip-flops compared to SRAM FPGA.

Selecting the Appropriate Xilinx Family

It is not always obvious which Xilinx family is the “right” choice for a particular application. To make a decision, start with the known data, the target application. Then address the following questions:

- What type of logic is used in the application?
- What special features are required?

Type of Logic

All Xilinx devices are general-purpose. Any family can implement any type of logic. There are, however, some features that make certain families more appropriate than others. The following items should be interpreted as “soft” suggestions, not as absolute, unequivocal choices.

1. For shortest pin-to-pin delays and fastest flip-flops:

Use XC9500, or, if fan-in is sufficient, XC3100A, XC4000E/X, or Spartan families.

XC9500 CPLDs have a PAL-like AND/OR structure that is inherently very fast. XC3100A has extremely fast logic blocks, but the single-level fan-in is limited to five.

XC4000E/X/Spartan families have a wider fan-in of nine. XC4000X FPGAs offer a very fast pin-to-pin path using a fast buffer and a 2-input function generator in the IOB.

2. For fastest state machines:

For encoded state machines, use XC9500.

For “one-hot” state machines, use XC3100A, XC4000E/X, XC5200, or Spartan families.

3. For fast counters/adders/subtractors/accumulators/comparators:

Use XC4000E/X, XC5200, Spartan or XC9500 families for wide functions.

Use XC3100A for fast, but short or simple counters.

Spartan, XC4000E/X, and XC5200 devices have dedicated carry-logic that is most effective over the range of 8 to 32 bits.

XC3100A achieves high speed for short word-length and simple operations (such as non-loadable counters) through its fast logic blocks.

4. For shortest design compilation time:

Use XC9500.

XC9500 achieves fast compilation through the simplicity of its PAL-like architecture.

5. For lowest cost per gate:

Use Spartan families.

6. For pinout compatibility within and between families:

Use XC4000E/X, XC5200.

These families are carefully designed to fit the same pinout in any given available package. This allows easy migration to different device sizes or families in the same package. The user can add logic or streamline the design or even use a less costly or faster family without any need to change the existing PC-board layout.

7. For Digital Signal Processing (multiply-accumulate) applications:

Use XC4000E/X or Spartan families.

The look-up-table architecture and the dedicated carry structure are very efficient for distributed arithmetic, a fast and effective way to implement fixed-point multiplication in digital filters.

Special Features Required

The fourteen items below describe specific features and characteristics available only in the listed families. These are, therefore, “hard” selection criteria.

8. For on-chip RAM:

Use XC4000E/X or Spartan families.

Has many 16x1 or 32x1 RAMs with synchronous write and dual-port capability.

9. For on-chip (bidirectional) bussing:

Use XC3000A, XC3100A, XC4000E/X, XC5200, XC9500, or Spartan families.

XC3000A, XC3100A, XC4000, Spartan and XC5200 families have horizontal Longlines that can be driven by internal 3-state drivers.

XC9500 devices implement busses indirectly using the wired-AND capability in the switch matrix.

10. For non-volatile single-chip solutions:

Use XC9500 or any HardWire device.

The SRAM-based devices require an external configuration source, which may be contained in the microprocessor’s memory. XC3000A and XC3000L devices can be used with a battery-backed-up supply, thus eliminating the need for external configuration storage.

11. For lowest possible static power consumption at 5V:

Use XC3000A and, to a lesser extent, Spartan, XC5200, XC4000E, XC4000EX families.

For Icc down to a few microamps, use XC3000A/L in powerdown. The other families consume a few milliamps.

Configurations for CMOS input thresholds on all inputs reduce supply current significantly.

12. For avoiding pin-locking problems with routing-intensive designs:

Use XC9500, XC4000EX, XC4000XL, XC5200.

XC9500 devices have special architectural features to enable pin locking.

XC4000EX, XC4000XL, and XC5200 provide additional routing channels, called VersaRing, between the core logic and the I/O.

13. For Boundary-Scan support:

Use Spartan, XC4000E, XC4000X, XC5200, or XC9500 families.

14. For rail-to-rail output voltage swing at 5V Vcc:

Use Spartan, XC3000A, XC3100A, XC4000E, XC4000EX, or XC5200 families.

(In XC4000E/EX, rail-to-rail is a user-option.)

XC9500 devices have a “totem-pole” output structure with lower Voh.

Spartan/XC4000E/EX devices can be configured with a global choice of either totem-pole or rail-to-rail outputs.

15. For 3.3V operation:

Use XC3000L, XC4000XL, or SpartanXL families.

16. For 5V operation Interfacing with 3.3V devices:

Use XC9500, Spartan or XC4000E/EX families.

Any Spartan/XC4000E/EX “totem-pole” output drives 3.3V inputs safely, and the TTL-like input threshold can be driven from 3.3V logic.

17. For In-system programmability:

Use all Xilinx families.

18. For PCI compatibility:

Use Spartan/XC4000E/XL and XC9500 families.

Target and Initiator designs are available for the XC4000E, XC4000XL, and Spartan families.

19. For Hi-Rel, military, or mil temperature-range applications:

Use XC4000E/X.

20. For battery-operated applications requiring low stand-by current:

Use XC3000A/L, Spartan, XC4000E/EX, XC5200 families.

XC3000L devices have inherently very low static power consumption.

XC3000A devices can use powerdown to ignore all input activity and tolerate Vcc down to 2.3V, while maintaining configuration.

Spartan/XC4000E/EX devices must be configured for CMOS input thresholds, and the user must shut down clock and logic activities externally.

21. For best protection against Illegal copying of a design (design security):

Use XC9500 with security bit activated.

Use XC3000A or XC3000L with powerdown battery-back-up configuration.

Further Information

For further information on any of the Xilinx products discussed in this application note, see the Xilinx WEBLINX at http://www.xilinx.com, or call your local sales office.

Table 1: Selecting a Xilinx Family

Feature	XC3000A	XC3000L	XC3100A	XC3100L	XC4000E	XC4000EX	XC4000XL	XC4000XV	XC5200	Spartan	SpartanXL	XC9500
1. Shortest pin-to-pin			X		X	X	X			X	X	X
2. Fastest state machines			X		X	X	X	X	X	X	X	X
3. Fastest arithmetic counters			X		X		X	X	X	X	X	
4. Fastest compilation												X
5. Lowest cost										X	X	
6. Footprint compatible families					X	X	X	X	X			
7. DSP (multiply/accumulate)					X	X	X	X		X	X	
8. RAM					X	X	X	X		X	X	
9. Bidirectional busses	X	X	X	X	X	X	X	X	X	X	X	X
10. Non-volatile/single chip												X
11. Low power @ 5V	X				X	X			X	X		
12. Tolerates pin-locking						X	X	X	X			X
13. Boundary scan					X	X	X	X	X	X	X	X
14. Full-swing 5V output	X		X		option	option			X	option		
15. 3.3V operation		X		X			X	X			X	
16. 5V out drives 3.3V					option	option				option		X
17. In-system programmable	X	X	X	X	X	X	X	X	X	X	X	X
18. PCI-compatible					X		X			X	X	X
19. Hi-rel, mil, mil-temp					X	X	X					
20. Low standby current	X	X			X	X	X	X		X	X	
21. Design security	X	X										X