TRACE

Preface

About This Manual

This manual describes Xilinx's TRACE program, a tool used for providing static timing analysis of a design based on input timing constraints.

Before using this manual, you should be familiar with the operations that are common to all Xilinx's software tools: how to bring up the system, select a tool for use, specify operations, and manage design data. These topics are covered in the *Development System Reference Guide*.

Other publications you can consult for related information are the Timing Analyzer Reference / User Guide manual.

Conventions

Typographical

This manual uses the following conventions. An example illustrates each convention.

- `Courier font` indicates messages, prompts, and program files that the system displays.

  ```
  speed grade: -100
  ```

- **`Courier bold`** indicates literal commands that you enter in a syntactical statement.

  `rpt_del_net=`

  `Courier bold` also indicates commands that you select from a menu.

  `File` → **`Open`**

- *Italic font* denotes the following items.

  - Variables in a syntax statement for which you must supply values

    `edif2ngd` *design_name*

  - References to other manuals

    See the *Development System Reference Guide* for more information.

  - Emphasis in text

    If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.

- Square brackets “[ ]” indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

  `edif2ngd` [*option_name*] *design_name*

  Square brackets also enclose footnotes in tables that are printed out as hardcopy in DynaText®.

- Braces “{ }” enclose a list of items from which you choose one or more.

  `lowpwr ={on|off}`

- A vertical bar “ | ” separates items in a list of choices.

  `symbol` *editor_name* `[bus|pins]`

- A vertical ellipsis indicates repetitive material that has been omitted.

  ```
  IOB #1: Name = QOUT’
  IOB #2: Name = CLKIN’
  .
  .
  .
  ```

- A horizontal ellipsis “. . .” indicates that an item can be repeated one or more times.

  `allow block` *block_name loc1 loc2* `...` *locn;*

Contents

TRACE

This program is compatible with the following families:

- XC3000A / L
- XC3100A / L
- XC4000E / L
- XC4000EX / XL / XV
- XC5200
- Spartan

This chapter describes the TRACE program. The chapter contains the following sections.

- "The TRACE Program" section
- "TRACE Syntax" section
- "TRACE Files" section
- "TRACE Options" section
- "Command Line Examples" section
- "TRACE Input Details" section
- "TRACE Output Details" section

The TRACE Program

TRACE (Timing Reporter And Circuit Evaluator) provides static timing analysis of a design based on input timing constraints.

Note: On the command line, the TRACE command is entered as **`trce`** (without an "A").

TRACE performs two major functions:

- Timing verification——the process of verifying that the design meets your timing constraints.
- Reporting—the process of enumerating input constraint violations and placing them into an accessible file. TRACE can be run on unplaced designs, completely placed and routed designs, or

designs that are placed and / or routed to any degree of completion.

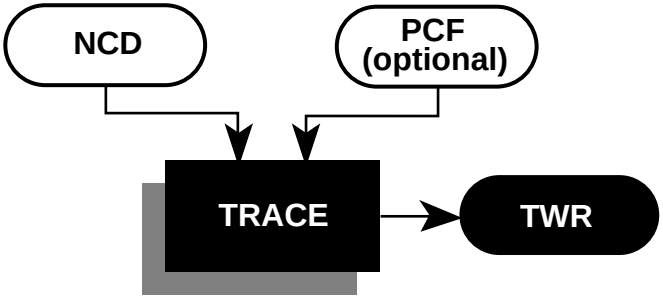

Figure 0-1 TRACE

TRACE Syntax

The following syntax runs TRACE:

trce [*options***] *design*[.ncd] [***constraint***[.pcf]]**

Options can be any number of the TRACE options listed in the "TRACE Options" section. They do not need to be listed in any particular order. Separate multiple options with spaces.

Design[.ncd] is the name of the input physical design file. If you enter a file name with no extension, TRACE looks for an NCD file with the name you specified.

Constraint[.pcf] specifies the name of a timing physical constraints file. This file is used to define timing constraints for the design. If you do not specify a physical constraints file, TRACE looks for one with the same root name as the NCD file.

TRACE Files

This section describes the TRACE input and output files.

Input Files

Input files to TRACE are:

- NCD file—a mapped design. The type of timing information you receive depends on whether the design is unplaced, placed only, or placed and routed.
- PCF file—an optional user-modifiable ASCII Physical Constraints File produced by the MAP program. The PCF file contains timing constraints used in the TRACE timing analysis.

Note: The Viewlogic CAE tools create a file with a .pcf extension when generating a plot of a Viewlogic schematic. This PCF file is not related to a Xilinx PCF file. Since TRACE automatically reads a PCF file with the same root name as your design file, make sure your directory does not contain a Viewlogic PCF file with the same root name as your NCD file.

Output Files

Output from TRACE is a timing report (TWR) file. There are three different types of timing reports: summary report, error report, and verbose report. The type or report produced is determined by the TRACE command line options you enter, as shown in the following table.

Table 0-1 TRACE Options and Reports

TRACE Option	Report Produced
No –e or –v	Summary report
–e	Error report
–v	Verbose report

TRACE Options

This section describes the options to the TRACE command.

–a (Advanced Analysis)

The –a option can only be used if you are not supplying any timing constraints (in a PCF file) to TRACE. The –a option writes out a timing report containing:

- An analysis that enumerates all clocks and the required OFFSETs for each clock.

- An analysis of paths having only combinatorial logic, ordered by delay.

This information is supplied in place of the default information for the output timing report type (summary, error, or verbose).

–e (Generate an Error Report)

-e [*limit*]

The –e option generates an error report. The report has the same root name as the input design and a .twr extension. You can assign a different root name for the report on the command line, but the extension must be .twr.

The *limit* is an integer limit on the number of items reported per constraint. The integer limit can be used to limit the number of items reported for each timing constraint in the report file (the default is 4096 items).

–f (Execute Commands File)

-f *command_file*

The –f option executes the command line arguments in the specified *command_file*. For more information on the –f option, see "The –f Option" section of the "Introduction" chapter**.**

–o (Output File Name)

-o *outfile***[.twr]**

The –o option specifies the name of output timing report. The .twr extension is optional.

–s (Change Speed)

-s [*speed*]

The –s option overrides the device speed contained in the input NCD file and instead performs an analysis for the device *speed* you specify. The –s option applies to whichever report type you produce in this TRACE run. The option allows you to see if faster or slower speed grades meet your timing requirements.

The device *speed* can be entered with or without the leading dash. For example, both –s 3 and –s –3 are allowable entries.

Note: The –s option only changes the speed grade for which the timing analysis is performed; it does not save the new speed grade to the NCD file.

–u (Report Uncovered Paths)

The –u option reports delays for paths that are not covered by timing constraints. The option adds an "Unconstrained path analysis" constraint to your existing constraints. This constraint performs a default path enumeration on any paths for which no other constraints apply. The default path enumeration includes circuit paths to data and clock pins on sequential components and data pins on primary outputs.

In the TRACE report, the following is included for the "Unconstrained path analysis" constraint:

- The minimum period for all of the uncovered paths to sequential components.
- The maximum delay for all of the uncovered paths containing only combinatorial logic.
- For a verbose report only, a listing of periods for sequential paths and delays for combinatorial paths. The list is ordered by delay in descending order, and the number of entries in the list can be controlled by specifying a limit when you enter the –v (Generate a Verbose Report) command line option.

-v (Generate a Verbose Report)

–v [*limit*]

The –v option generates a verbose report. The report has the same root name as the input design and a .twr extension. You can assign a different root name for the report on the command line, but the extension must be .twr.

The *limit* is an integer limit on the number of items reported per constraint. The integer limit can be used to limit the number of items reported for each timing constraint in the report file (the default is 4096 items).

Command Line Examples

The following command verifies the timing characteristics of the design named design1.ncd, generating a summary timing report. Timing constraints contained in the file group1.pcf are the timing constraints for the design. This generates the report file design1.twr.

```
trce  design1.ncd  group1.pcf
```

The following command produces a file listing all delay characteristics for the design named design1.ncd, using the timing constraints contained in the file group1.pcf. The verbose report file is called output.twr.

```
trce  –v  design1.ncd  group1.pcf  –o output.twr
```

The following command analyzes the file design1.ncd and reports on the three worst errors for each constraint in timing.pcf. The report is called design1.twr.

```
trce   –e 3   design1.ncd   timing.pcf
```

TRACE Input Details

Input to TRACE is a mapped NCD design and an optional physical constraints (PCF) file based upon timing constraints that you specify. Constraints can indicate such things as clock speed for input signals, the external timing relationship between two or more signals, absolute maximum delay on a design path, or a general timing requirement for a class of pins.

TRACE Output Details

TRACE output is an ASCII timing report file which enables you to see how well the timing constraints for the design have been met. The file is written into your current working directory and has a .twr extension. The default name for the file is the same root name as the NCD file. You can designate a different root name for the file, but it must have a .twr extension. The extension .twr is assumed if not specified.

The timing report lists statistics on the design, any detected timing errors, and a number of warning conditions.

Timing errors indicate absolute or relative timing constraint violations. These include:

- Path delay errors—where the path delay exceeds the maximum delay constraint for a path.
- Net delay errors—where a net connection delay exceeds the maximum delay constraint for the net.
- Offset errors—where either the delay offset between an external clock and its associated data-in pin is insufficient to meet the internal logic's timing requirements or the delay offset between an external clock and its associated data-out pin exceeds the external logic's timing requirements.
- Net skew errors—where skew between net connections exceeds the maximum skew constraint for the net.

Timing errors may require design modifications, running PAR, or both.

Warnings point out potential problems such as circuit loops or a constraint that does not define any paths.

Four types of reports are available; you determine the report type by entering the appropriate option entry on the UNIX or DOS command line or by selecting the type of report from the Timing Analyzer (see "TRACE Options" section). Each type of report is described in the "Reporting with TRACE" section.

Timing Verification with TRACE

TRACE checks the delays in the NCD design file against your timing constraints. If delays are exceeded, TRACE issues the appropriate timing error.

Net Delay Constraints

The delay for a constrained net is checked to ensure that the constraint is equal to or greater than the routedelay.

constraint ≥ **routedelay**

where:

routedelay is the signal delay between the driver pin and the load pin(s) on a net. This is an estimated delay if the design is placed but not routed.

Any nets showing delays that do not meet this condition generate timing errors in the timing report.

Net Skew Constraints

Signal skew on a net with multiple load pins is the difference between minimum and maximum load delays. Skew is checked against the specified maximum skew for constrained nets in the PCF file.

constraint ≥ (maxdelay - mindelay)

where:

maxdelay is the maximum delay between the driver pin and a load pin.

mindelay is the minimum delay between the driver pin and a load pin.

If the skew is found to exceed the maximum skew constraint, the timing report shows a skew error.

Path Delay Constraints

The delay through a constrained path is checked to ensure that the constraint is greater than or equal to the sum of logic (component) delay, route (wire) delay, and setup time (if any).

constraint ≥ logicdelay + routedelay + setuptime

where:

logicdelay is the pin-to-pin delay through a component.

routedelay is the signal delay between component pins in a path. This is an estimated delay if the design is placed but not routed.

setuptime (for clocked paths only) is the time that data must be present on an input pin before the arrival of the triggering edge of a clock signal.

Paths showing delays that do not meet this condition generate timing errors in the timing report.

Reporting with TRACE

The timing report produced by TRACE is an ASCII file prepared for a particular design. It reports statistics on the design, a summary of timing warnings and errors, and optional detailed net and path delay reports.

Note: All TRACE reports are formatted for viewing in a monospace (non-proportional) font. If the text editor you use for viewing the reports uses a proportional font, the columns in the reports do not line up correctly.

This section covers the four different types of timing reports generated by TRACE. They are:

- The summary report—Contains summary information, design statistics, and statistics for each constraint in the PCF file.
- The error report—Lists timing errors and associated net / path delay information.
- The verbose report—Lists delay information for all nets and paths.

In each type of report, the header specifies the type of report, the input design name, the optional input physical constraints file name, and device and speed data for the input NCD file. At the end of each report is a timing summary, which includes the following information:

- The number of timing errors found in the design. This information appears in all reports.
- A timing score, showing the total amount of error (in picoseconds) for all timing constraints in the design.
- The number of paths and nets covered by the constraints
- The number of route delays and the percentage of connections covered by timing constraints

Note: The percentage of connections covered by timing constraints is given in a “% coverage” statistic. The statistic does not indicate the percentage of paths covered; it indicates the percentage of connections covered. Even if you have entered constraints that cover all paths in the design, this percentage may be less than 100%, since

some connections are never included for timing analysis (for example, connections to the STARTUP component).

- The number of nets covered by constraints
- A list of global statistics for the design

In the following sections, a description of each report is accompanied by a sample.

Some additional notes about timing reports:

- For any of the four types of reports, if you specify a physical constraints file that contains invalid data, a list of physical constraints file errors appears at the beginning of the report. These include errors in constraint syntax.
- In a TRACE report, a tilde (~) preceding a delay value indicates that the delay value is approximate. Values with the tilde cannot be calculated exactly because of excessive delays, resistance, or capacitance on the net. You can use the PENALIZE TILDE constraint to penalize these delays by a specified percentage (see the "TRACE" chapter and the "Attributes, Constraints, and Carry Logic" chapter of the *Libraries Guide* for a description of the PENALIZE TILDE constraint).
- In a TRACE report, an "R" appended to a delay value indicates the value was calculated for a rising signal, and an "F" indicates the value for a falling signal. If rising and falling values are different, TRACE reports the appropriate delay.
- TRACE detects when a path loops, (that is, when the path passes through a driving output more than once), and reports the total number of loops detected in the design. When TRACE detects a loop, it disables the loop from being analyzed. If the loop itself is made up of many possible routes, each route is disabled for all paths which converge through the loop in question and the total number is included in the reported loop tally.

  A path is considered to loop outside of the influence of other paths in the design. Thus if a valid path follows a loop from another path, but actually converges at an input and not a driving output, the path is not disabled and will contain the elements of the loop which may be disabled on another path.
- In Xilinx FPGAs, tristate buffer (TBUF) outputs are always routed on longlines. Pullup resistors may also be tied to these longlines.

The timing effects of a TBUF / pullup combination is handled differently in the various FPGA architectures.

- In XC3000A / L, XC3100A / L, 4000E / L, XC5200, and Spartan designs, the delay associated with the longline is built into the component delay for the TBUF, and is not included in the delay reported for the net on the longline.
- In XC4000EX / XL / XV designs, the net delay on the longline is computed and reported as if the pullup (and not the TBUF output) is driving the net. If you want the delay to be computed with the TBUF driving the net, do not include any pullups at the output of the TBUF.

Summary Report

The summary report includes the name of the design file being analyzed, the device speed and report level, followed by a statistical brief that includes the summary information (timing errors, etc. described above) and design statistics. The report also list statistics for each constraint in the PCF file, including the number of timing errors for each constraint.

A summary report is produced when you do not enter a –e (error report) or –v (verbose report) option on the TRACE command line.

Two sample summary reports are shown below. The first sample shows the results without having a physical constraints file. The second sample shows the results when a physical constraints file is specified.

If no physical constraints file exists or if there are no timing constraints in the PCF file, TRACE performs default path and net enumeration to provide timing analysis statistics. Default path enumeration includes all circuit paths to data and clock pins on sequential components and all data pins on primary outputs. Default net enumeration includes all nets.

Summary Report (Without a Physical Constraints File Specified)

The following sample summary report represents the output of this TRACE command:

```
trce -o summary1.twr trc_test.ncd
```

The name of the report is summary1.twr. No preference file is specified on the command line, and the directory containing the file tr_test.ncd did not contain a PCF file called tr_test.pcf.

```
--------------------------------------------------------------------------
Xilinx TRACE, Version M1.4
Copyright (c) 1995-1997 Xilinx, Inc.  All rights reserved.

Design file:              trc_test.ncd
Device,speed:             xc4006e,-4 (x1_0.86)
Report level:             summary report
--------------------------------------------------------------------------

WARNING:bastw:170 - No timing constraints found, doing default
enumeration.
13 circuit loops found and disabled.

==========================================================================
Timing constraint: Default period analysis
 5231 items analyzed, 0 timing errors detected.
 Minimum period is  64.536ns.
--------------------------------------------------------------------------

==========================================================================
Timing constraint: Default net enumeration
 620 items analyzed, 0 timing errors detected.
 Maximum net delay is  41.022ns.
--------------------------------------------------------------------------


All constraints were met.


Timing summary:
---------------

Timing errors: 0  Score: 0

Constraints cover 5231 paths, 620 nets, and 2029 connections (100.0%
coverage)

Design statistics:
   Minimum period:  64.536ns (Maximum frequency:  15.495MHz)
   Maximum net delay:  41.022ns
```

```
Analysis completed Tue Oct 28 17:49:41 1997
--------------------------------------------------------------------
```

Summary Report (With a Physical Constraints File Specified)

The following sample summary report represents the output of this TRACE command:

```
trce -o summary2.twr trc_test.ncd trc_test.pcf
```

The name of the report is summary2.twr. The timing analysis represented in the file were performed by referring to the constraints in the file tr_test.pcf.

```
--------------------------------------------------------------------
Xilinx TRACE, Version M1.4
Copyright (c) 1995-1997 Xilinx, Inc.  All rights reserved.

Design file:              trc_test.ncd
Physical constraint file: trc_test.pcf
Device,speed:             xc4006e,-4 (x1_0.86)
Report level:             summary report
--------------------------------------------------------------------

26 circuit loops found and disabled.

====================================================================
Timing constraint: allpaths MAXDELAY = 65 ;
 2240 items analyzed, 0 timing errors detected.
 Maximum delay is  62.813ns.
--------------------------------------------------------------------

====================================================================
Timing constraint: FROM TIMEGRP “pads” TO TIMEGRP “pads” MAXDELAY = 100 ;
 11 items analyzed, 0 timing errors detected.
 Maximum delay is  49.816ns.
--------------------------------------------------------------------

====================================================================
Timing constraint: TS00 = MAXDELAY FROM TIMEGRP “ffs” TO TIMEGRP “ffs”
80.0 ;
 2951 items analyzed, 0 timing errors detected.
 Maximum delay is  62.566ns.
--------------------------------------------------------------------

====================================================================
Timing constraint: TS01 = MAXDELAY FROM TIMEGRP “rising_ffs” TO TIMEGRP
```

```
“falling_ffs” TS00 / 2 ;
 11 items analyzed, 0 timing errors detected.
 Maximum delay is  32.268ns.
--------------------------------------------------------------------------------

================================================================================
Timing constraint: TS02 = MAXDELAY FROM TIMEGRP “falling_ffs” TO TIMEGRP
“rising_ffs” TS00 / 2 ;
 17 items analyzed, 0 timing errors detected.
 Maximum delay is  15.895ns.
--------------------------------------------------------------------------------

================================================================================
Timing constraint: allclocknets MAXSKEW = 5.0 ;
 14 items analyzed, 1 timing error detected.
 Maximum net skew is   5.009ns.
--------------------------------------------------------------------------------

================================================================================
Timing constraint: FROM TIMEGRP “myinputs” TO TIMEGRP “myoutputs” MAXDELAY
= 45 ;
 1 item analyzed, 1 timing error detected.
 Maximum delay is  47.660ns.
--------------------------------------------------------------------------------


2 constraints not met.


Timing summary:
---------------

Timing errors: 2  Score: 2669

Constraints cover 5231 paths, 14 nets, and 2028 connections (100.0%
coverage)

Design statistics:
   Maximum path delay from/to any node:  62.813ns
   Maximum net skew:   5.009ns


Analysis completed Tue Oct 28 17:44:22 1997
--------------------------------------------------------------------------------
```

When the physical constraints file includes timing constraints, the summary report lists the percentage of all design connections covered by timing constraints. If there are no timing constraints, the report shows 100 percent coverage.

Error Report

The error report lists timing errors and associated net / path delay information. Errors are ordered by constraint and, within constraints, by slack (the difference between the constraint and the analyzed value, with a negative slack indicationg an error condition). The number of errors listed for each constraint is set by the limit you enter on the command line. The error report also contains a list of all time groups defined in the PCF file, and all of the members defined within each group.

The main body of the error report lists all timing constraints as they appear in the input PCF file. If the constraint is met, the report simply states the number of items scored by TRACE, reports no timing errors detected, and issues a brief report line, indicating important information (for example, the maximum delay for the particular constraint). If the constraint is not met, it gives the number of items scored by TRACE, the number of errors encountered, and a detailed breakdown of the error. For errors in which the path delays are broken down into individual net and component delays, the report lists each physical resource and the logical resource from which the physical resource was generated.

As in the other three types of reports, descriptive material appears at the top. A timing summary always appears at the end of the report. A sample error report follows.

Sample Error Report

The following sample error report (error.twr) represents the output of this TRACE command:

```
trce -o error.twr -e 2 trc_test.ncd trc_test.pcf
```

```
--------------------------------------------------------------------------
Xilinx TRACE, Version M1.4
Copyright (c) 1995-1997 Xilinx, Inc.  All rights reserved.

Design file:              trc_test.ncd
Physical constraint file: trc_test.pcf
```

```
Device,speed:             xc4006e,-4 (x1_0.86)
Report level:             error report, limited to 2 items per constraint
------------------------------------------------------------------------

26 circuit loops found and disabled.

========================================================================
Timing constraint: allpaths MAXDELAY = 65 ;
 2240 items analyzed, 0 timing errors detected.
 Maximum delay is  62.813ns.
------------------------------------------------------------------------

========================================================================
Timing constraint: FROM TIMEGRP “pads” TO TIMEGRP “pads” MAXDELAY = 100 ;
 11 items analyzed, 0 timing errors detected.
 Maximum delay is  49.816ns.
------------------------------------------------------------------------

========================================================================
Timing constraint: TS00 = MAXDELAY FROM TIMEGRP “ffs” TO TIMEGRP “ffs”
80.0 ;
 2951 items analyzed, 0 timing errors detected.
 Maximum delay is  62.566ns.
------------------------------------------------------------------------

========================================================================
Timing constraint: TS01 = MAXDELAY FROM TIMEGRP “rising_ffs” TO TIMEGRP
“falling_ffs” TS00 / 2 ;
 11 items analyzed, 0 timing errors detected.
 Maximum delay is  32.268ns.
------------------------------------------------------------------------

========================================================================
Timing constraint: TS02 = MAXDELAY FROM TIMEGRP “falling_ffs” TO TIMEGRP
“rising_ffs” TS00 / 2 ;
 17 items analyzed, 0 timing errors detected.
 Maximum delay is  15.895ns.
------------------------------------------------------------------------

========================================================================
Timing constraint: allclocknets MAXSKEW = 2.0 ;
 14 items analyzed, 3 timing errors detected.
 Maximum net skew is   5.009ns.
------------------------------------------------------------------------
Slack:    -3.009ns FAD_RGCK
```

```
Error:     5.009ns skew exceeds   2.000ns timing constraint by 3.009ns
From                          To                            Delay(ns)  Skew(ns)
CLB_R3C4.XQ                   CLB_R6C15.K                     7.186      0.000
CLB_R3C4.XQ                   CLB_R11C7.K                    11.222      4.036
CLB_R3C4.XQ                   CLB_R10C8.K                    10.898      3.712
CLB_R3C4.XQ                   CLB_R12C7.K                    11.050      3.864
CLB_R3C4.XQ                   CLB_R13C15.K                   12.052      4.866
CLB_R3C4.XQ                   CLB_R12C15.K                   12.195      5.009
CLB_R3C4.XQ                   CLB_R16C15.K                   11.621      4.435
CLB_R3C4.XQ                   CLB_R6C10.K                     7.203      0.017
CLB_R3C4.XQ                   CLB_R16C16.K                    9.297      2.111

--------------------------------------------------------------------------------
Slack:    -2.609ns 16US_CLK
Error:     4.609ns skew exceeds   2.000ns timing constraint by 2.609ns
From                          To                            Delay(ns)  Skew(ns)
CLB_R8C15.XQ                  CLB_R6C15.G2                    1.899      0.465
CLB_R8C15.XQ                  CLB_R8C15.G1                    1.434      0.000
CLB_R8C15.XQ                  CLB_R7C8.K                      6.043      4.609
CLB_R8C15.XQ                  CLB_R8C6.K                      5.760      4.326
CLB_R8C15.XQ                  CLB_R7C6.K                      6.043      4.609

--------------------------------------------------------------------------------

================================================================================
Timing constraint: FROM TIMEGRP “myinputs” TO TIMEGRP “myoutputs” MAXDELAY
= 45 ;
 1 item analyzed, 1 timing error detected.
 Maximum delay is  47.660ns.
--------------------------------------------------------------------------------
Slack:    -2.660ns path CRESETN to VCASN2 relative to
          45.000ns delay constraint

Path CRESETN to VCASN2 contains 5 levels of logic:
Path starting from Comp: P93.PAD
To                    Delay type         Delay(ns)  Physical Resource
                                                    Logical Resource(s)
-------------------------------------------------  --------
P93.I1                Tpid                 3.000R  CRESETN
                                                    CRESETN
                                                    RESETN
CLB_R12C14.F4         net (fanout=1)       2.609R  RESETN
CLB_R12C14.X          Tilo                 2.700R  RESET
                                                    RESET
CLB_R7C1.F3           net (fanout=124)    15.135R  RESET
```

```
CLB_R7C1.X           Tilo                  2.700R  ADDR2
                                                   ADDR2
CLB_R1C1.F4          net (fanout=8)        3.600R  ADDR2
CLB_R1C1.X           Tilo                  2.700R  CAS_EN2
                                                   CAS_EN2
P3.T                 net (fanout=1)        1.506R  CAS_EN2
P3.PAD               Ttsons               13.710R  VCASN2
                                                   VCASN2.OUTBUF
                                                   VCASN2
----------------------------------------
Total (24.810ns logic, 22.850ns route)    47.660ns
      (52.1% logic, 47.9%% route)

--------------------------------------------------------------------------------


2 constraints not met.


Table of Timegroups:
-------------------
TimeGroup pads:
BELs:
 D24              D25              D26              D27              D28
 D29              D30              D31              D16              D23
 D22              D21              D20              D19              D18
           .
           .
           .
 BTKN_SYNCN       BSLOT3           BSLOT2           BSLOT1           BSLOT0



TimeGroup ffs:
BELs:
 TIMOUT0           TIMOUT1           TIMOUT2           TIMOUT3
 TIMOUT4           TIMOUT5           TIMOUT6           TIMOUT7
           .
           .
           .
 TOK_CNT4          TOK_CNT2          TOK_CNT1          200NS_CLK
 400NS_CLK         XMT_TIMOUT        32US_CLK          CSLOADPC

TimeGroup rising_ffs:
BELs:
```

```
 TIMOUT0           TIMOUT1           TIMOUT2           TIMOUT3
 TIMOUT4           TIMOUT5           TIMOUT6           TIMOUT7
           .
           .
           .
 TOK_CNT3          TOK_CNT4          TOK_CNT2          TOK_CNT1
 200NS_CLK         400NS_CLK         XMT_TIMOUT        32US_CLK

TimeGroup falling_ffs:
BELs:
 HSEL              FAD_RGCK          HCAS              HTOL

TimeGroup myinputs:
BELs:
 CRESETN

TimeGroup myoutputs:
BELs:
 VCASN2




Timing summary:
---------------

Timing errors: 28  Score: 171832

Constraints cover 5239 paths, 14 nets, and 2004 connections (100.0%
coverage)

Design statistics:
   Maximum path delay from/to any node:  49.171ns
   Maximum net skew:   2.096ns



Analysis completed Tue Oct 28 17:46:15 1997
------------------------------------------------------------------------
```

Verbose Report

The verbose report is similar to the error report, providing more details on delays for all constrained paths and nets in the design. Entries are ordered by constraint and, within constraints, by slack. The number of items listed for each constraint is set by the limit you enter on the command line. The verbose report also contains a list of all time groups defined in the PCF file, and all of the members defined within each group.

As in the other three types of reports, descriptive material appears at the top.

The body of the verbose report enumerates each constraint as it appears in the input physical constraints file, the number of items scored by TRACE for that constraint, and the number of errors detected for the constraint. Each item is described, ordered by descending slack. A Report line for each item provides important information, such as the amount of delay on a net and by how much the constraint is met.

For path constraints, if there is an error, the report indicates the amount by which the constraint is exceeded. For errors in which the path delays are broken down into individual net and component delays, the report lists each physical resource and the logical resource from which the physical resource was generated.

If there are no errors, the report indicates that the constraint passed and by how much. Each logic and route delay is analyzed, totaled, and reported.

Sample Verbose Report

The following sample verbose report (verbose.twr) represents the output of this TRACE command:

```
trce -o verbose.twr -v 2 trc_test.ncd trc_test.pcf
```

```
--------------------------------------------------------------------
Xilinx TRACE, Version M1.4.12
Copyright (c) 1995-1997 Xilinx, Inc.  All rights reserved.

Design file:              trc_test.ncd
Physical constraint file: trc_test.pcf
Device,speed:             xc4006e,-4 (x1_0.86)
Report level:             verbose report, limited to 2 items per constraint
```

```
--------------------------------------------------------------------------

26 circuit loops found and disabled.

==========================================================================
Timing constraint: allpaths MAXDELAY = 65 ;
 2240 items analyzed, 0 timing errors detected.
 Maximum delay is  62.813ns.
--------------------------------------------------------------------------
Slack:     2.187ns path DR/_299_ to VCASN1 relative to
          65.000ns delay constraint

Path DR/_299_ to VCASN1 contains 7 levels of logic:
Path starting from Comp: CLB_R9C16.K (from MSCLK)
To                    Delay type         Delay(ns)  Physical Resource
                                                    Logical Resource(s)
-------------------------------------------------  --------
CLB_R9C16.XQ          Tcko                 3.700R  DR/_299_
                                                    BUFSTOP_ACS
CLB_R8C14.F4          net (fanout=9)       2.561R  BUFSTOP_ACS
CLB_R8C14.X           Tilo                 2.700R  A_RCV_REG
                                                    A_RCV_REG
CLB_R7C7.F3           net (fanout=1)       4.976R  A_RCV_REG
CLB_R7C7.Y            Tiho                 4.700R  REG_ACS
                                                    REG_ACS
                                                    DE/MX/_43_
CLB_R14C5.G4          net (fanout=3)       8.376R  DE/MX/_43_
CLB_R14C5.X           Tiho                 4.700R  D_OUT_02
                                                    DE/MX/_153_
                                                    D_OUT_02
CLB_R7C1.F4           net (fanout=2)       4.728R  D_OUT_02
CLB_R7C1.X            Tilo                 2.700R  ADDR2
                                                    ADDR2
CLB_R2C1.F4           net (fanout=8)       3.600R  ADDR2
CLB_R2C1.X            Tilo                 2.700R  CAS_EN310
                                                    CAS_EN310
P150.T                net (fanout=3)       3.662R  CAS_EN310
P150.PAD              Ttsons              13.710R  VCASN1
                                                    VCASN1.OUTBUF
                                                    VCASN1
-------------------------------------------------
Total (34.910ns logic, 27.903ns route)    62.813ns
      (55.6% logic, 44.4%% route)

--------------------------------------------------------------------------
```

```
Slack:     2.265ns path DR/RST1 to VCASN1 relative to
          65.000ns delay constraint

Path DR/RST1 to VCASN1 contains 7 levels of logic:
Path starting from Comp: CLB_R7C11.K (from MSCLK)
To                    Delay type         Delay(ns)  Physical Resource
                                                    Logical Resource(s)
-------------------------------------------------  --------
CLB_R7C11.XQ          Tcko                 3.700R  DR/RST1
                                                    DR/RST1
CLB_R8C14.F3          net (fanout=7)       2.483R  DR/RST1
CLB_R8C14.X           Tilo                 2.700R  A_RCV_REG
                                                    A_RCV_REG
CLB_R7C7.F3           net (fanout=1)       4.976R  A_RCV_REG
CLB_R7C7.Y            Tiho                 4.700R  REG_ACS
                                                    REG_ACS
                                                    DE/MX/_43_
CLB_R14C5.G4          net (fanout=3)       8.376R  DE/MX/_43_
CLB_R14C5.X           Tiho                 4.700R  D_OUT_02
                                                    DE/MX/_153_
                                                    D_OUT_02
CLB_R7C1.F4           net (fanout=2)       4.728R  D_OUT_02
CLB_R7C1.X            Tilo                 2.700R  ADDR2
                                                    ADDR2
CLB_R2C1.F4           net (fanout=8)       3.600R  ADDR2
CLB_R2C1.X            Tilo                 2.700R  CAS_EN310
                                                    CAS_EN310
P150.T                net (fanout=3)       3.662R  CAS_EN310
P150.PAD              Ttsons              13.710R  VCASN1
                                                    VCASN1.OUTBUF
                                                    VCASN1
-------------------------------------------------
Total (34.910ns logic, 27.825ns route)    62.735ns
      (55.6% logic, 44.4%% route)

--------------------------------------------------------------------------

==========================================================================
           .
           .
           .
==========================================================================
Timing constraint: allclocknets MAXSKEW = 5.0 ;
 14 items analyzed, 1 timing error detected.
 Maximum net skew is   5.009ns.
```

```
--------------------------------------------------------------------------
Slack:    -0.009ns FAD_RGCK
Error:     5.009ns skew exceeds   5.000ns timing constraint by 0.009ns
From                        To                            Delay(ns)  Skew(ns)
CLB_R3C4.XQ                 CLB_R6C15.K                     7.186      0.000
CLB_R3C4.XQ                 CLB_R11C7.K                    11.222      4.036
CLB_R3C4.XQ                 CLB_R10C8.K                    10.898      3.712
CLB_R3C4.XQ                 CLB_R12C7.K                    11.050      3.864
CLB_R3C4.XQ                 CLB_R13C15.K                   12.052      4.866
CLB_R3C4.XQ                 CLB_R12C15.K                   12.195      5.009
CLB_R3C4.XQ                 CLB_R16C15.K                   11.621      4.435
CLB_R3C4.XQ                 CLB_R6C10.K                     7.203      0.017
CLB_R3C4.XQ                 CLB_R16C16.K                    9.297      2.111

--------------------------------------------------------------------------
Slack:     0.391ns 16US_CLK
Report:    4.609ns skew meets   5.000ns timing constraint by 0.391ns
From                        To                            Delay(ns)  Skew(ns)
CLB_R8C15.XQ                CLB_R6C15.G2                    1.899      0.465
CLB_R8C15.XQ                CLB_R8C15.G1                    1.434      0.000
CLB_R8C15.XQ                CLB_R7C8.K                      6.043      4.609
CLB_R8C15.XQ                CLB_R8C6.K                      5.760      4.326
CLB_R8C15.XQ                CLB_R7C6.K                      6.043      4.609

--------------------------------------------------------------------------

==========================================================================
Timing constraint: FROM TIMEGRP “myinputs” TO TIMEGRP “myoutputs” MAXDELAY
= 45 ;
 1 item analyzed, 1 timing error detected.
 Maximum delay is  47.660ns.
--------------------------------------------------------------------------
Slack:    -2.660ns path CRESETN to VCASN2 relative to
          45.000ns delay constraint

Path CRESETN to VCASN2 contains 5 levels of logic:
Path starting from Comp: P93.PAD
To                  Delay type         Delay(ns)  Physical Resource
                                                  Logical Resource(s)
-------------------------------------------------  --------
P93.I1              Tpid                  3.000R  CRESETN
                                                  CRESETN
                                                  RESETN
CLB_R12C14.F4       net (fanout=1)        2.609R  RESETN
CLB_R12C14.X        Tilo                  2.700R  RESET
```

```
                                                      RESET
CLB_R7C1.F3          net (fanout=124)     15.135R     RESET
CLB_R7C1.X           Tilo                  2.700R     ADDR2
                                                      ADDR2
CLB_R1C1.F4          net (fanout=8)        3.600R     ADDR2
CLB_R1C1.X           Tilo                  2.700R     CAS_EN2
                                                      CAS_EN2
P3.T                 net (fanout=1)        1.506R     CAS_EN2
P3.PAD               Ttsons               13.710R     VCASN2
                                                      VCASN2.OUTBUF
                                                      VCASN2
------------------------------------------------
Total (24.810ns logic, 22.850ns route)    47.660ns
      (52.1% logic, 47.9%% route)

--------------------------------------------------------------------------------


2 constraints not met.


Table of Timegroups:
-------------------
TimeGroup pads:
BELs:
 D24             D25             D26             D27             D28
 D29             D30             D31             D16             D23
           .
           .
           .
 BTKN_SYNCN      BSLOT3          BSLOT2          BSLOT1          BSLOT0



TimeGroup ffs:
BELs:
 TIMOUT0          TIMOUT1          TIMOUT2          TIMOUT3
 TIMOUT4          TIMOUT5          TIMOUT6          TIMOUT7
           .
           .
           .
 64US             32US             TOK_CNT0         TOK_CNT3
 TOK_CNT4         TOK_CNT2         TOK_CNT1         200NS_CLK
```

```
TimeGroup rising_ffs:
BELs:
 TIMOUT0           TIMOUT1           TIMOUT2           TIMOUT3
 TIMOUT4           TIMOUT5           TIMOUT6           TIMOUT7
           .
           .
           .
 TOK_CNT3          TOK_CNT4          TOK_CNT2          TOK_CNT1
 200NS_CLK         400NS_CLK         XMT_TIMOUT        32US_CLK

TimeGroup falling_ffs:
BELs:
 HSEL                FAD_RGCK             HCAS
BEL_TPKT_ENVN.OUTFF


TimeGroup myinputs:
BELs:
 CRESETN


TimeGroup myoutputs:
BELs:
 VCASN2




Timing summary:
---------------


Timing errors: 28  Score: 171832


Constraints cover 5239 paths, 14 nets, and 2004 connections (100.0%
coverage)


Design statistics:
   Minimum period:  45.012ns (Maximum frequency:  22.216MHz)
   Maximum path delay from/to any node:  49.171ns
   Maximum net skew:   2.096ns
```

```
Analysis completed Tue Oct 28 17:47:59 1997
--------------------------------------------------------------------------------
```

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