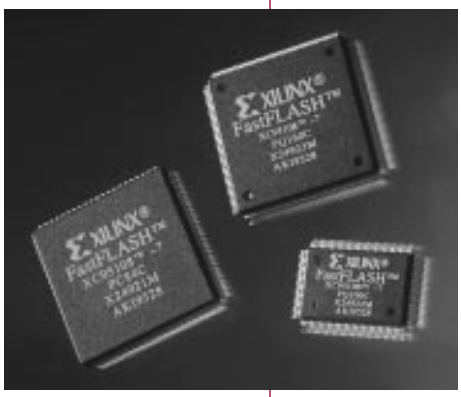
# Using XC9500 JTAG and ISP in Manufacturing

Our XC9500 CPLD family includes a unique combination of JTAG test capability and in-system programmability (ISP) that can save considerable time and money during the manufacturing process. Because the ISP and JTAG functions are both controlled through the same industry-standard, four-wire JTAG port, automatic test equipment (ATE) can perform system test, device test, and device programming in one integrated operation. And, Xilinx supplies the tools that make this easy.



A large number of Xilinx customers have successfully integrated the XC9500 ISP capability into their manufacturing flows, choosing to simply integrate JTAGProgrammer (formerly known as EZTag) into their final test process to program their XC9500 devices. Because Xilinx devices are shipped from the factory in an erased state, the "skip erase before programming" option can be used to reduce programming time, maximize product flow through the process, and reduce costs.

Other Xilinx customers have determined that it is more economical to integrate the programming step directly into their manufacturing tests. This effectively uses their ATE as programming hardware. This method, while conceptually more complicated, can make better use of available hardware resources. It can also reduce the total number of steps in the manufacturing process, thereby streamlining and optimizing operations, and eliminating fallout due to increased handling.

Xilinx supplies a set of free tools to facilitate this integration (available from our Web site, WebLINX, at www.xilinx.com). These tools retarget the standard serial vector format (SVF) Boundary-Scan stimulus description language to the native stimulus input formats for the industry's most popular ATEs. Full support is available for the Hewlett Packard HP3070 series, the GenRad GR228X series, and the Teradyne Z1800 series of ATE.

In the manufacturing environment, stray electrical noise can result in incorrect Boundary-Scan test failures. In the same manner, this noise can contribute to ISP operation failures. Therefore, all XC9500 devices include the optional Boundary-Scan HIGHZ instruction which forces all device pins into a 3-state condition. Xilinx XC9500 CPLDs are the only type that make this optional instruction available. You can use this instruction to make certain that XC9500 devices act as a "quiet" Boundary-Scan neighbor during ISP and test operations.

By forcing the XC9500 device outputs into a 3-state condition, while other parts are being tested or programmed, you can minimize the noise generated by active system signals and effectively "silence" the board. Many test engineers have made use of this functionality in improving their overall system test and ISP reliability.

By supporting the optional Boundary-Scan IDCODE and USERCODE instructions, XC9500 devices are fully identifiable as to their type and programmed contents so that you can selectively run tests based on the PLD composition of the system under test, or based on the contents of those devices.

Finally, gross functional test via the 4-pin Boundary-Scan interface is supported by the optional INTEST instruction. This allows for the application of functional test stimuli using low-pin-count testers or other Boundary-Scan-based tools.

Xilinx is the only CPLD manufacturer providing this high level of JTAG and ISP functionality, thus continuing to make major advancements in the practical application of ISP in the manufacturing environment. ◆

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