XC4000 High-Reliability Logic Cell Array Family

March 1997 (version 1.0) Product Description

Features

- Available in Class B fully compliant and military temperature range only versions
  - MIL-STD-883 Class B processing complies with paragraph 1.2.1
- Third Generation Field-Programmable Gate Array
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry propagation circuit
  - Wide edge decoders
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and Interconnect
  - Low power consumption
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Programmable output slew rate (2 modes)
  - Programmable input pull-up or pull-down resistors
  - 4-mA sink current per output (8 mA XC4003A)
  - 8-mA sink current per output pair (16 mA XC4003A)
- Configured by Loading Binary File
  - Unlimited re-programmability
  - Six programming modes
- XACT® Development System runs on '386/486'-type PC, Apollo, Sun-4, Sparc and HP700
  - Interfaces to popular design environments like FutureNet, Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The XC4000 family of Field-Programmable Gate Arrays (FPGAs) provides the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array.

The XC4000 families provide a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources surrounded by a perimeter of programmable Input/Output Blocks (IOBs).

All XC4000-family devices have generous routing resources to accommodate the most complex interconnect patterns. XC4000A devices have reduced sets of routing resources, sufficient for their smaller size.

The devices are customized by loading configuration data into the internal memory cells. The FPGA can either actively read its configuration data out of an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA (slave and peripheral modes).

The XC4000 family is supported by powerful and sophisticated software, covering every aspect of design: from schematic entry, to simulation, to automatic block placement and routing of interconnects, and finally the creation of the configuration bit stream.

Since Xilinx FPGAs can be re-programmed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications.

Table 1. The XC4000 High-Reliability Family of Field-Programmable Gate Arrays

Device	XC4003A	XC4005	XC4010	XC4013
Appr. Gate Count:	3,000	5,000	10,000	13,000
CLB Matrix:	10 x 10	14 x 14	20 x 20	24 x 24
Number of CLBs:	100	196	400	576
Number of Flip-Flops:	360	616	1,120	1,536
Max RAM Bits:	3,200	6,272	12,800	18,432
Number of IOBs:	80	112	160	192

XC4000 Family Configuration Pin Assignments

CONFIGURATION MODE: <M2:M1:M0>						
SLAVE <1:1:1>	MASTER-SER <0:0:0>	SYN.PERIPH <0:1:1>	ASYN.PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	USER OPERATION
				A16	A16	PGI-I/O
				A17	A17	I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
						SGI-I/O
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	(O)
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	(I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	(I)
						PGI-I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
* $\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	I/O
						SGI-I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
						PGI-I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
			$\overline{\text{CS0}}$ (I)			**I/O**
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)		I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
			$\overline{\text{RS}}$ (I)			I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
		RDY/$\overline{\text{BUSY}}$	RDY/$\overline{\text{BUSY}}$	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGI-I/O
CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK(O)	CCLK (O)	CCLK (I)
TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			$\overline{\text{WS}}$ (I)	A0	A0	I/O
				A1	A1	PGI-I/O
			CS1 (I)	A2	A2	I/O
				A3	A3	I/O
				A4	A4	I/O
				A5	A5	I/O
				A6	A6	I/O
				A7	A7	I/O
				A8	A8	I/O
				A9	A9	I/O
				A10	A10	I/O
				A11	A11	I/O
				A12	A12	I/O
				A13	A13	I/O
				A14	A14	I/O
				A15	A15	SGI-I/O
						ALL OTHERS

Represents a 50 kΩ to 100 kΩ pull-up before and during configuration

* INIT is an open-drain output during configuration

(I) Represents an input

X5265

XC4003A Pinouts

Pin Description	CB100	PG120	Bound Scan
VCC	89	G3	-
I/O (A8)	90	G1	32
I/O (A9)	91	F1	35
I/O	92	E1	38
I/O	93	F2	41
I/O (A10)	94	F3	44
I/O (A11)	95	D1	47
-	-	E2*	-
I/O (A12)	96	C1	50
I/I (A13)	97	D2	53
-	-	E3*	-
-	-	B1*	-
I/O (A14)	98	C2	56
PGCK1 (A15, I/O)	99	D3	59
VCC	100	C3	-
GND	1	C4	-
PGCK1 (A16, I/O)	2	B2	62
I/O (A17)	3	B3	65
-	-	A1*	-
-	-	A2*	-
I/I (TDI)	4	C5	68
I/O (TCK)	5	B4	71
-	-	A3*	-
I/O (TMS)	6	B5	74
I/O	7	A4	77
I/O	-	C6	80
I/O	8	A5	83
I/O	9	B6	86
I/O	10	A6	89
GND	11	B7	-
VCC	12	C7	-
I/O	13	A7	92
I/O	14	A8	95
I/O	15	A9	98
I/O	-	B8	101
I/O	16	C8	104
I/O	17	A10	107
I/O	18	B9	110
I/O	19	A11	113
-	-	B10*	-
I/O	20	C9	116
SGCK2 (I/O)	21	A12	119
O (M1)	22	B11	122
GND	23	C10	-
I (M0)	24	C11	125†
VCC	25	D11	-
I (M2)	26	B12	126†
PGCK2 (I/O)	27	C12	127
I/O (HDC)	28	A13	130
-	-	B13*	-
-	-	E11*	-
I/O	29	D12	133
I/O ($\overline{\text{LDC}}$)	30	C13	136
I/O	31	E12	139
I/O	32	D13	142
I/O	33	F11	145
I/O	34	E13	148
I/O	35	F12	151
I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	36	F13	154
VCC	37	G12	-

Pin Description	CB100	PG120	Bound Scan
GND	38	G11	-
I/O	39	G13	157
I/O	40	H13	160
I/O	41	J13	163
I/O	42	H12	166
I/O	43	H11	169
I/O	44	K13	172
I/O	45	J12	175
I/O	46	L13	178
-	-	K12*	-
-	-	J11*	-
I/O	47	M13	181
SGCK3 (I/O)	48	L12	184
GND	49	K11	-
DONE	50	L11	-
VCC	51	L10	-
$\overline{\text{PROG}}$	52	M12	-
I/O (D7)	53	M11	187
PGCK3 (I/O)	54	N13	190
-	-	N12*	-
-	-	L9*	-
I/O (D6)	55	M10	193
I/O	56	N11	196
I/O (D5)	57	M9	199
I/O (CS0)	58	N10	202
I/O	59	L8	205
I/O	60	N9	208
I/O (D4)	61	M8	211
I/O	62	N8	214
VCC	63	M7	-
GND	64	L7	-
I/O (D3)	65	N7	217
I/O ($\overline{\text{RS}}$)	66	N6	220
I/O	67	N5	223
I/O	-	M6	226
I/O (D2)	68	L6	229
I/O	69	N4	232
I/O (D1)	70	M5	235
I/O (RCLK-$\overline{\text{BUSY}}$/RDY)	71	N3	238
-	-	M4*	-
-	-	L5*	-
I/O (D0, DIN)	72	N2	241
SGCK4 (DOUT, I/O)	73	M3	244
CCLK	74	L4	-
VCC	75	L3	-
O (TDO)	76	M2	-
GND	77	K3	-
I/O (A0, $\overline{\text{WS}}$)	78	L2	2
PGCK4 (A1, I/O)	79	N1	5
-	-	M1*	-
-	-	J3*	-
I/O (CS1, A2)	80	K2	8
I/O (A3)	81	L1	11
I/O (A4)	82	J2	14
I/O (A5)	83	K1	17
I/O	84	H3	20
I/O	85	J1	23
I/O (A6)	86	H2	26
I/O (A7)	87	H1	29
GND	88	G2	-

* Indicates unconnected package pins

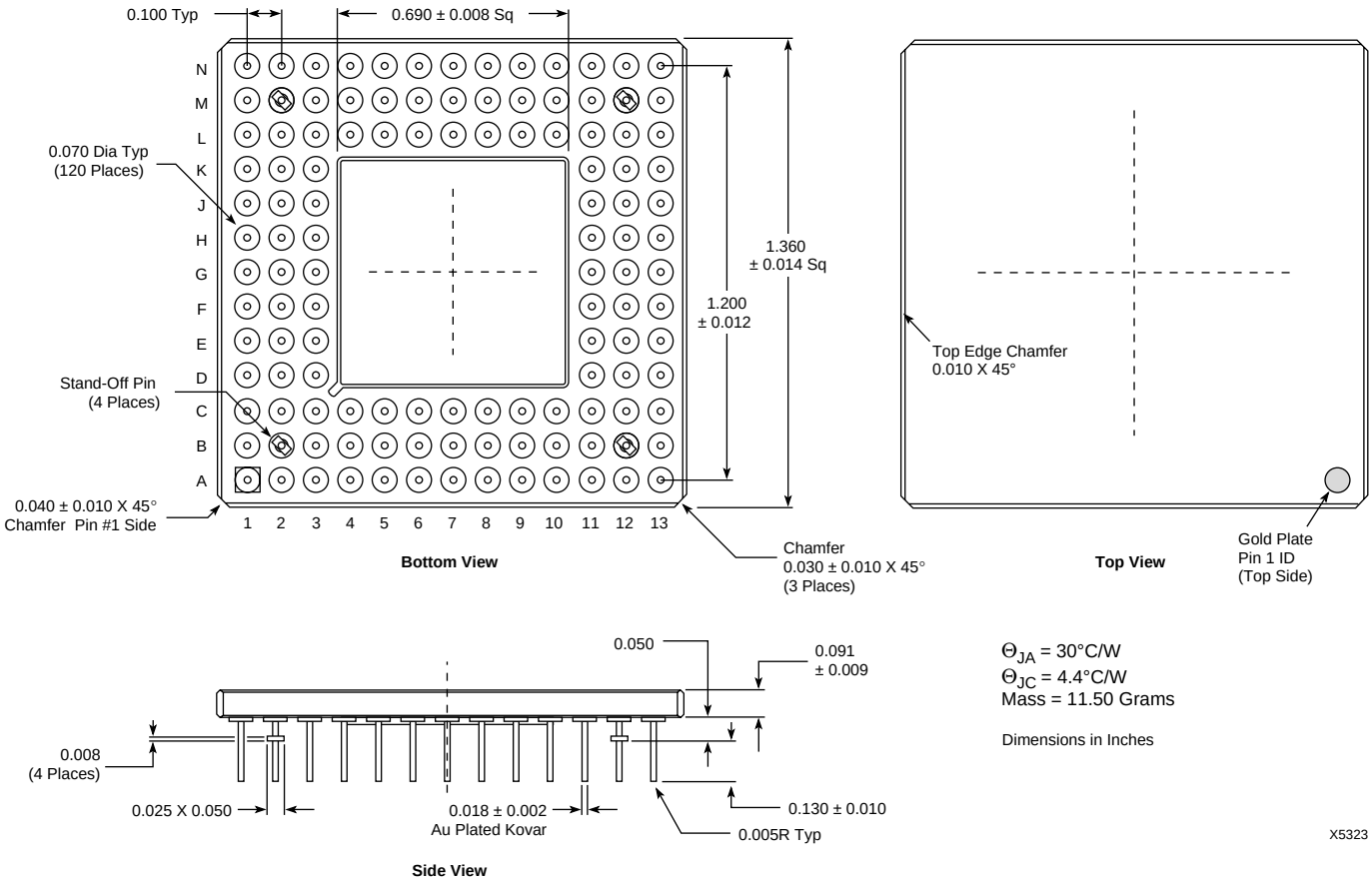
† Contributes only one bit (.i) to the boundary scan register

Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1= TDO.O

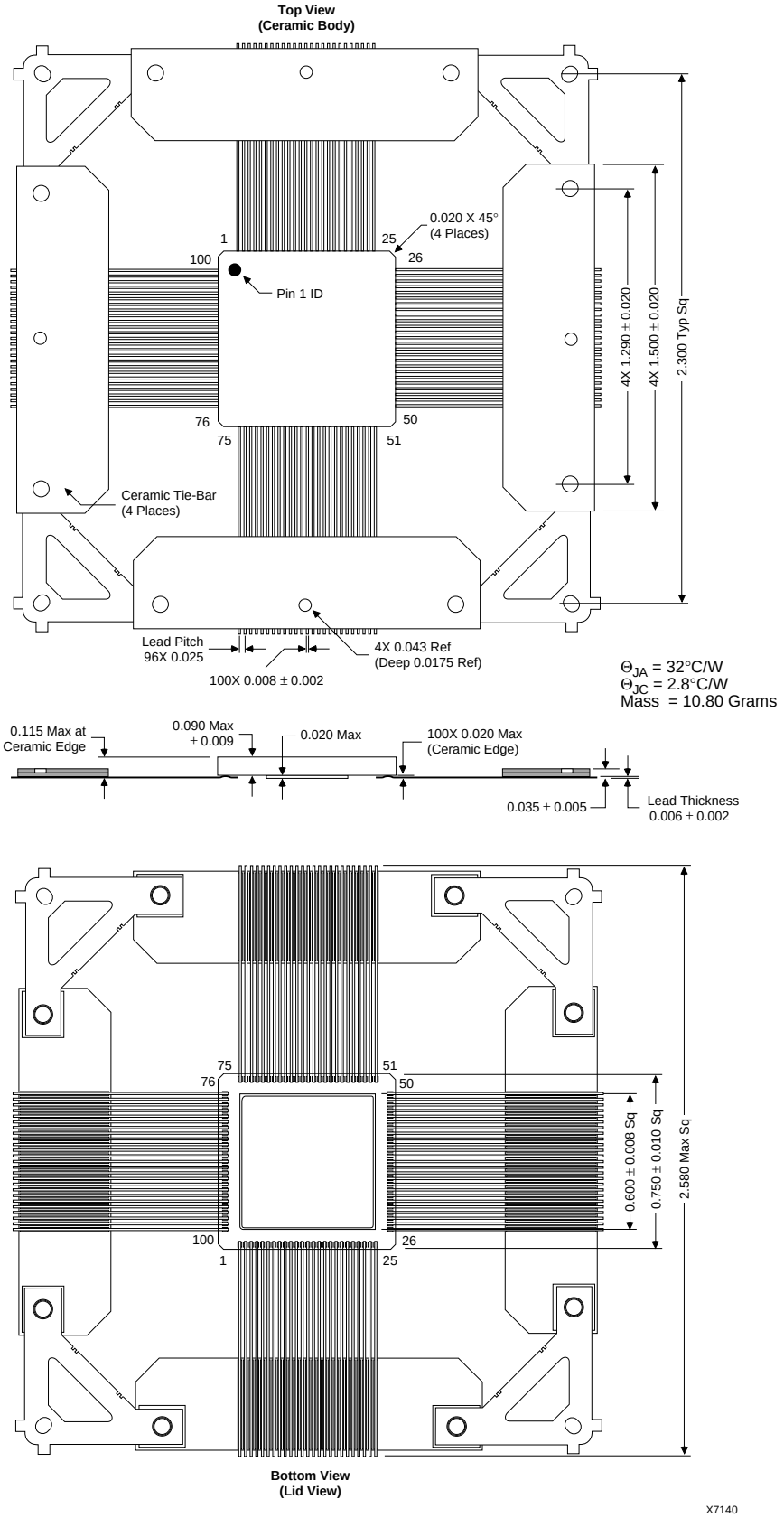
Boundary Scan Bit 247 = BSCANT.UPD

Package Outline



120-Pin Ceramic PGA (PG120)

Package Outline



100-Pin Ceramic QFP (CB100)

XC4005 Pinouts

Pin Description	CB164	PG156	Bound Sca
VCC	145	H3	-
I/O (A8)	146	H1	44
I/O (A9)	147	G1	47
I/O	148	G2	50
I/O	149	G3	53
-	-	-	-
-	-	-	-
I/O (A10)	150	F1	56
I/O (A11)	151	F2	59
I/O	152	E1	62
I/O	153	E2	65
GND	154	F3	-
-	-	-	-
-	-	-	-
-	155*	D1*	-
-	156*	D2*	-
I/O (A12)	157	E3	68
I/O (A13)	158	C1	71
-	159*	-	-
I/O	160	C2	74
I/O	161	D3	77
I/O (A14)	162	B1	80
SGCK1(A15, I/O)	163	B2	83
VCC	164	C3	-
-	-	-	-
-	-	-	-
-	-	-	-
-	-	-	-
GND	1	C4	-
-	-	-	-
PGCK1 (A16, I/O)	2	B3	86
I/O (A17)	3	A1	89
I/O	4	A2	92
I/O	5	C5	95
-	6*	-	-
I/O (TDI)	7	B4	98
I/O (TCK)	8	A3	101
-	9*	A4*	-
-	-	-	-
-	-	-	-
-	-	-	-
GND	10	C6	-
I/O	11	B5	104
I/O	12	B6	107
I/O (TMS)	13	A5	110
I/O	14	C7	113
-	-	-	-
-	-	-	-
I/O	15	B7	116
I/O	16	A6	119
I/O	17	A7	122
I/O	18	A8	125
GND	19	C8	-
VCC	20	B8	-
I/O	21	C9	128
I/O	22	B9	131
I/O	23	A9	134
I/O	24	B10	137
-	25*	-	-
-	-	-	-
I/O	26	C10	140
I/O	27	A10	143
I/O	28	A11	146
I/O	29	B11	149
GND	30	C11	-
-	-	-	-
-	-	-	-
-	31*	A12*	-
-	-	-	-
I/O	32	B12	152
I/O	33	A13	155
I/O	34	A14	158

Pin Description	CB164	PG156	Bound Sca
I/O	35	C12	161
-	36*	-	-
I/O	37	B13	164
SGCK2 (I/O)	38	B14	167
O (M1)	39	A15	170
GND	40	C13	-
I (M0)	41	A16	173†
-	-	-	-
-	-	-	-
-	-	-	-
VCC	42	C14	-
I (M2)	43	B15	174†
PGCK2 (I/O)	44	B16	175
I/O (HDC)	45	D14	178
I/O	46	C15	181
-	47*	-	-
I/O	48	D15	184
I/O	49	E14	187
I/O ($\overline{LDC}$)	50	C16	190
-	51*	E15*	-
-	52*	D16*	-
-	-	-	-
-	-	-	-
GND	53	F14	-
I/O	54	F15	193
I/O	55	E16	196
I/O	56	F16	199
I/O	57	G14	202
-	-	-	-
-	-	-	-
I/O	58	G15	205
I/O	59	G16	208
I/O	60	H16	211
I/O ($\overline{ERR}$,$\overline{INIT}$)	61	H15	214
VCC	62	H14	-
GND	63	J14	-
I/O	64	J15	217
I/O	65	J16	220
I/O	66	K16	223
I/O	67	K15	226
-	-	-	-
-	-	-	-
I/O	68	K14	229
I/O	69	L16	232
I/O	70	M16	235
I/O	71	L15	238
GND	72	L14	-
-	-	-	-
-	-	N16*	-
-	73*	M15*	-
-	74*	P16	241
I/O	75	M14	244
I/O	76	N15	247
I/O	77	P15	250
I/O	78	N14	253
I/O	79	T16	256
SGCK3 (I/O)	80	P14	-
GND	81	-	-
-	-	-	-
DONE	82	R15	-
-	-	-	-
-	-	-	-
VCC	83	P13	-
-	-	-	-
$\overline{PROG}$	84	R14	-
I/O (D7)	85	T16	259
PGCK3 (I/O)	86	T15	262
I/O	87	R13	265
-	88*	-	-
I/O	89	P12	268
I/O (D6)	90	T14	271

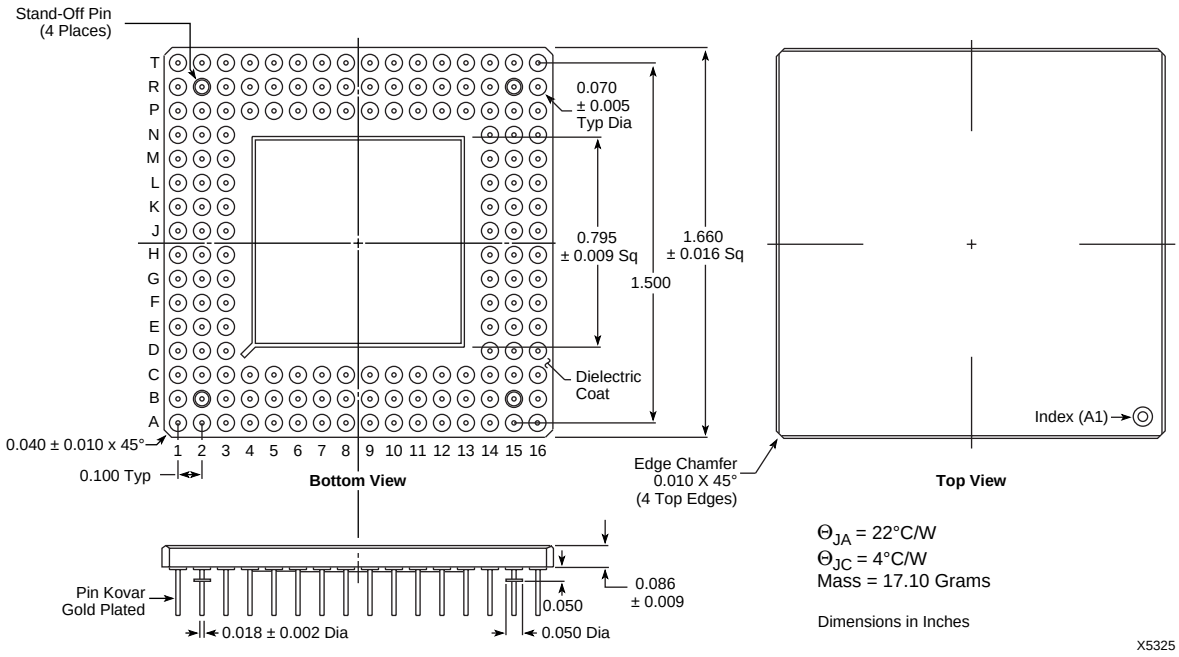
Pin Description	CB164	PG156	Bound Sca
I/O	91	T13	274
-	92*	R12*	-
-	-	-	-
-	93*	T12*	-
-	-	-	-
-	-	-	-
GND	94	P11	-
I/O	95	R11	277
I/O	96	T11	280
I/O (D5)	97	T10	283
I/O (CS0)	98	P10	286
-	-	-	-
-	-	-	-
I/O	99	R10	289
I/O	100	T9	292
I/O (D4)	101	R9	295
I/O	102	P9	298
VCC	103	R8	-
GND	104	P8	-
I/O (D3)	105	T8	301
I/O ($\overline{RS}$)	106	T7	304
I/O	107	T6	307
I/O	108	R7	310
-	-	-	-
-	-	-	-
I/O (D2)	109	P7	313
I/O	110	T5	316
I/O	111	R6	319
I/O	112	T4	322
GND	113	P6	-
-	-	-	-
-	-	-	-
-	114*	R5*	-
-	-	-	-
I/O (D1)	115	T3	325
I/O (RCLK-$\overline{BUSY}$/RDY)	116	P5	328
I/O	117	R4	331
-	118*	-	-
I/O	119	R3	334
I/O (D0, DIN)	120	P4	337
SGCK4 (DOUT, I/O)	121	T2	340
CCLK	122	R2	-
VCC	123	P3	-
-	-	-	-
-	-	-	-
-	-	-	-
-	-	-	-
O (TDO)	124	T1	-
GND	125	N3	-
I/O (A0, $\overline{WS}$)	126	**R1**	2
PGCK4 (A1, I/O)	127	P2	5
I/O	128	N2	8
-	129*	-	-
I/O	130	M3	11
I/O (CS1, A2)	131	P1	14
I/O (A3)	132	N1	17
-	133*	M2*	-
-	134*	M1*	-
-	-	-	-
-	-	-	-
GND	135	L3	-
I/O	136	L2	20
I/O	137	L1	23
I/O (A4)	138	K3	25
I/O (A5)	139	K2	29
-	-	-	-
-	-	-	-
I/O	140	K1	32
I/O	141	J1	35
I/O (A6)	142	J2	38
I/O (A7)	143	J3	41
GND	144	H2	-

* Indicates unconnected package pins

† Contributes only one bit (.i) to the boundary scan register

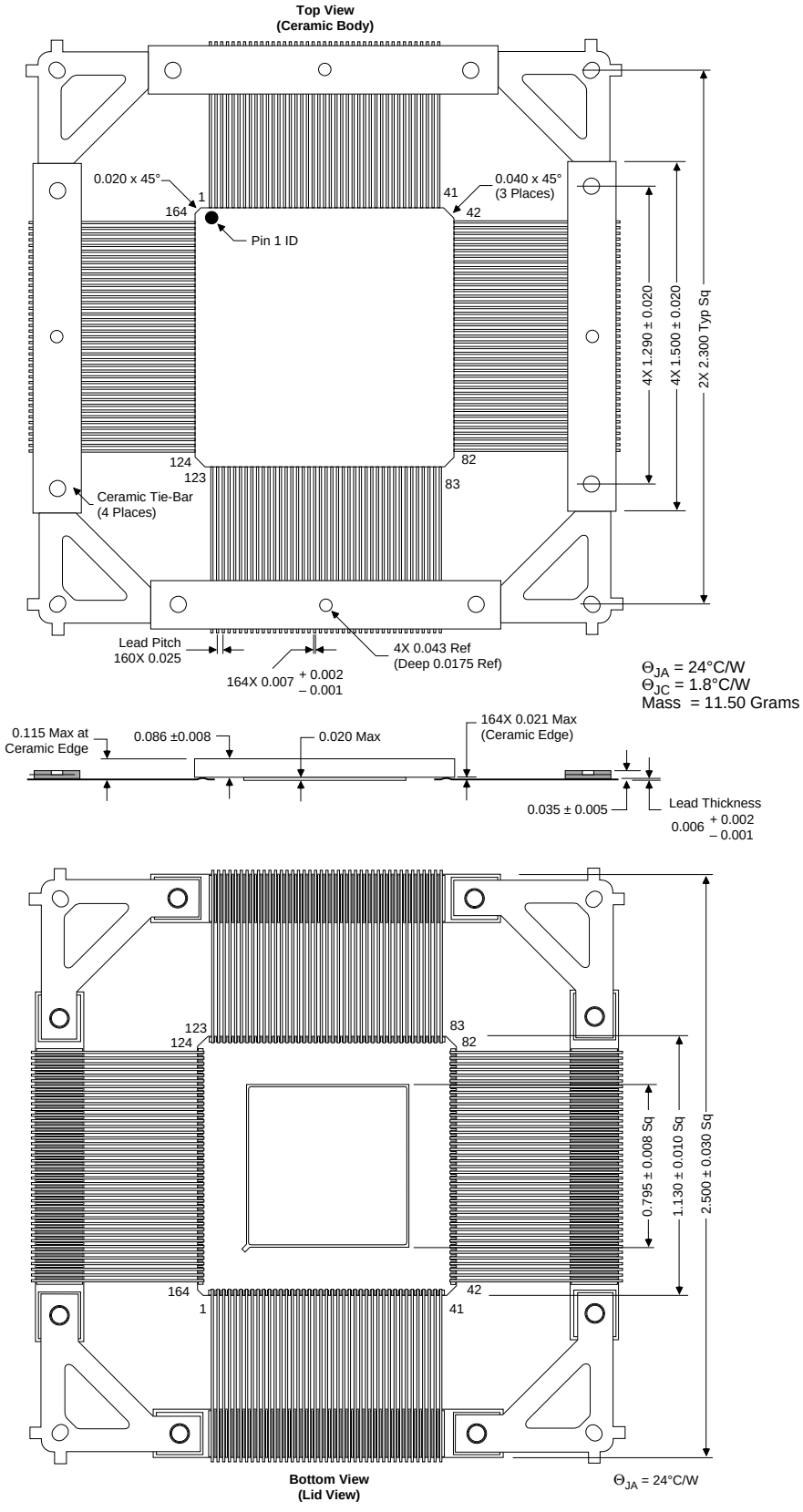
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1= TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

Package Outline



156-Pin Ceramic PGA (PG156)

Package Outline



164-Pin Ceramic QFP (CB164)

XC4010 Pinouts

Pin Description	PG191	CB196	Bound Scan
VCC	J4	173	-
I/O (A8)	J3	174	62
I/O (A9)	J2	175	65
I/O	J1	176	68
I/O	H1	177	71
I/O	H2	178	74
I/O	H3	179	77
I/O (A10)	G1	180	80
I/O (A11)	G2	181	83
I/O	F1	182	86
I/O	E1	183	89
GND	G3	184	-
I/O	F2	185	92
I/O	D1	186	96
I/O	C1	187	98
I/O	E2	188	101
I/O (A12)	F3	189	104
I/O (A13)	D2	190	107
I/O	B1	191	110
–	–	192*	–
I/O	E3	193	113
I/O (A14)	C2	194	116
SGCK1 (A15, I/O)	B2	195	119
VCC	D3	196	-
-	-	-	-
-	-	-	-
GND	D4	1	-
-	-	-	-
PGCK1 (A16, I/O)	C3	2	122
I/O (A17)	C4	3	125
I/O	B3	4	128
-	-	5*	-
I/O	C5	6	131
I/O (TDI)	A2	7	134
I/O (TCK)	B4	8	137
I/O	C6	9	140
I/O	A3	10	143
I/O	B5	11	146
I/O	B6	12	149
GND	C7	13	-
I/O	A4	14	152
I/O	A5	15	155
I/O (TMS)	B7	16	158
I/O	A6	17	161
I/O	C8	18	164
I/O	A7	19	167
I/O	B8	20	170
I/O	A8	21	173
I/O	B9	22	176
I/O	C9	23	179
GND	D9	24	-
VCC	D10	25	-

Pin Description	PG191	CB196	Bound Scan
I/O	C10	26	182
I/O	B10	27	185
I/O	A9	28	188
I/O	A10	29	191
I/O	A11	30	194
I/O	C11	31	197
I/O	B11	32	200
I/O	A12	33	203
I/O	B12	34	206
I/O	A13	35	209
GND	C12	36	-
I/O	B13	37	212
I/O	A14	38	215
I/O	A15	39	218
I/O	C13	40	221
I/O	B14	41	224
I/O	A16	42	227
I/O	B15	43	230
I/O	C14	44	233
I/O	A17	45	236
SGCK2 (I/O)	B16	46	239
M1	C15	47	242
GND	D15	48	
M0	A18	49	245†
-	-	-	-
-	-	-	-
VCC	D16	50	-
M2	C16	51	246†
PGCK2 (I/O)	B17	52	247
I/O (HDC)	E16	53	250
-	-	54*	-
I/O	C17	55	253
I/O	D17	56	256
I/O	B18	57	259
I/O (LDC)	E17	58	262
I/O	F16	59	265
I/O	C18	60	268
I/O	D18	61	271
I/O	F17	62	274
GND	G16	63	-
I/O	E18	64	277
I/O	F18	65	280
I/O	G17	66	283
I/O	G18	67	286
I/O	H16	68	289
I/O	H17	69	291
I/O	H18	70	295
I/O	J18	71	298
I/O	J17	72	301
I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	J16	73	304
VCC	J15	74	-

* Indicates unconnected package pins

† Contributes only one bit (.i) to the boundary scan register

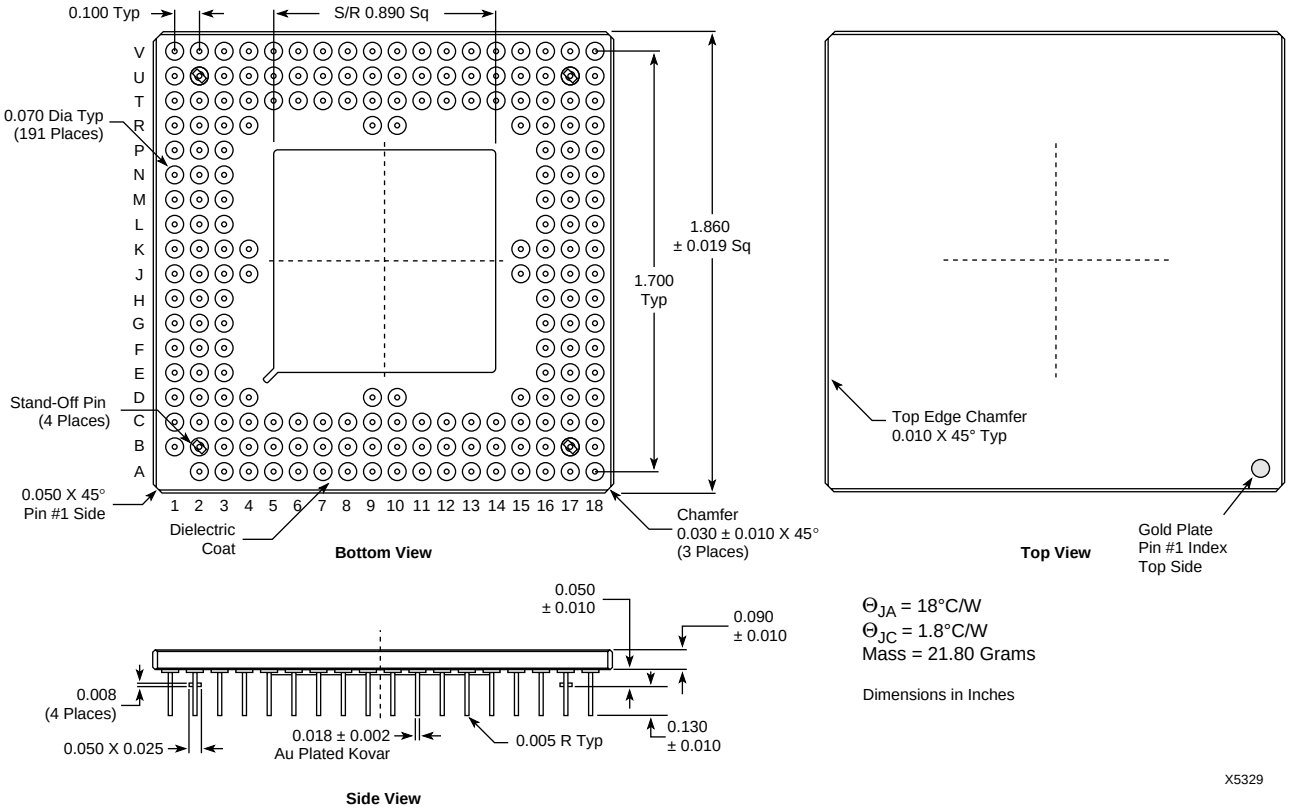
XC4010 Pinouts (continued)

Pin Description	PG191	CB196	Bound Scan
GND	K15	75	-
I/O	K16	76	307
I/O	K17	77	310
I/O	K18	78	313
I/O	L18	79	316
I/O	L17	80	319
I/O	L16	81	322
I/O	M18	82	325
I/O	M17	83	328
I/O	N18	84	331
I/O	P18	85	334
GND	M16	86	-
I/O	N17	87	337
I/O	R18	88	340
I/O	T18	89	343
I/O	P17	90	346
I/O	N16	91	349
I/O	T17	92	352
I/O	R17	93	355
I/O	P16	94	358
I/O	U18	95	361
SGCK3 (I/O)	T16	96	364
GND	R16	97	-
-	-	-	-
DONE	U17	98	-
VCC	R15	99	-
-	-	-	-
$\overline{\text{PROG}}$	V18	100	-
I/O (D7)	T15	101	367
PGCK3 (I/O)	U16	102	370
-	-	103*	-
I/O	T14	104	373
I/O	U15	105	376
I/O (D6)	V17	106	379
I/O	V16	107	382
I/O	T13	108	385
I/O	U14	109	388
I/O	V15	110	391
I/O	V14	111	394
GND	T12	112	-
I/O	U13	113	397
I/O	V13	114	400
I/O (D5)	U12	115	403
I/O ($\overline{\text{CSO}}$)	V12	116	406
I/O	T11	117	409
I/O	U11	118	412
I/O	V11	119	415
I/O	V10	120	418
I/O (D4)	U10	121	421
I/O	T10	122	424
VCC	R10	123	-

Pin Description	PG191	CB196	Bound Scan
GND	R9	124	-
I/O (D3)	T9	125	427
I/O ($\overline{\text{RS}}$)	U9	126	430
I/O	V9	127	433
I/O	V8	128	436
I/O	U8	129	439
I/O	T8	130	442
I/O (D2)	V7	131	445
I/O	U7	132	448
I/O	V6	133	451
I/O	U6	134	454
GND	T7	135	-
I/O	V5	136	457
I/O	V4	137	460
I/O	U5	138	463
I/O	T6	139	466
I/O (D1)	V3	140	469
I/O ($\overline{\text{RCLK}}$-$\overline{\text{BUSY}}$/RDY)	V2	141	472
I/O	U4	142	475
I/O	T5	143	478
I/O (D0, DIN)	U3	144	481
SGCK4 (DOUT, I/O)	T4	145	484
CCLK	V1	146	-
VCC	R4	147	-
-	-	-	-
-	-	-	-
TD0	U2	148	-
GND	R3	149	-
I/O (A0, $\overline{\text{WS}}$)	T3	150	2
PGCK4 (I/O, A1)	U1	151	5
-	-	152*	-
I/O	P3	153	8
I/O	R2	154	11
I/O (CS1, A2)	T2	155	14
I/O (A3)	N3	156	17
I/O	P2	157	20
I/O	T1	158	23
I/O	R1	159	26
I/O	N2	160	29
GND	M3	161	-
I/O	P1	162	32
I/O	N1	163	35
I/O (A4)	M2	164	38
I/O (A5)	M1	165	41
I/O	L3	166	44
I/O	L2	167	47
I/O	L1	168	50
I/O	K1	169	53
I/O (A6)	K2	170	56
I/O (A7)	K3	171	59
GND	K4	172	-

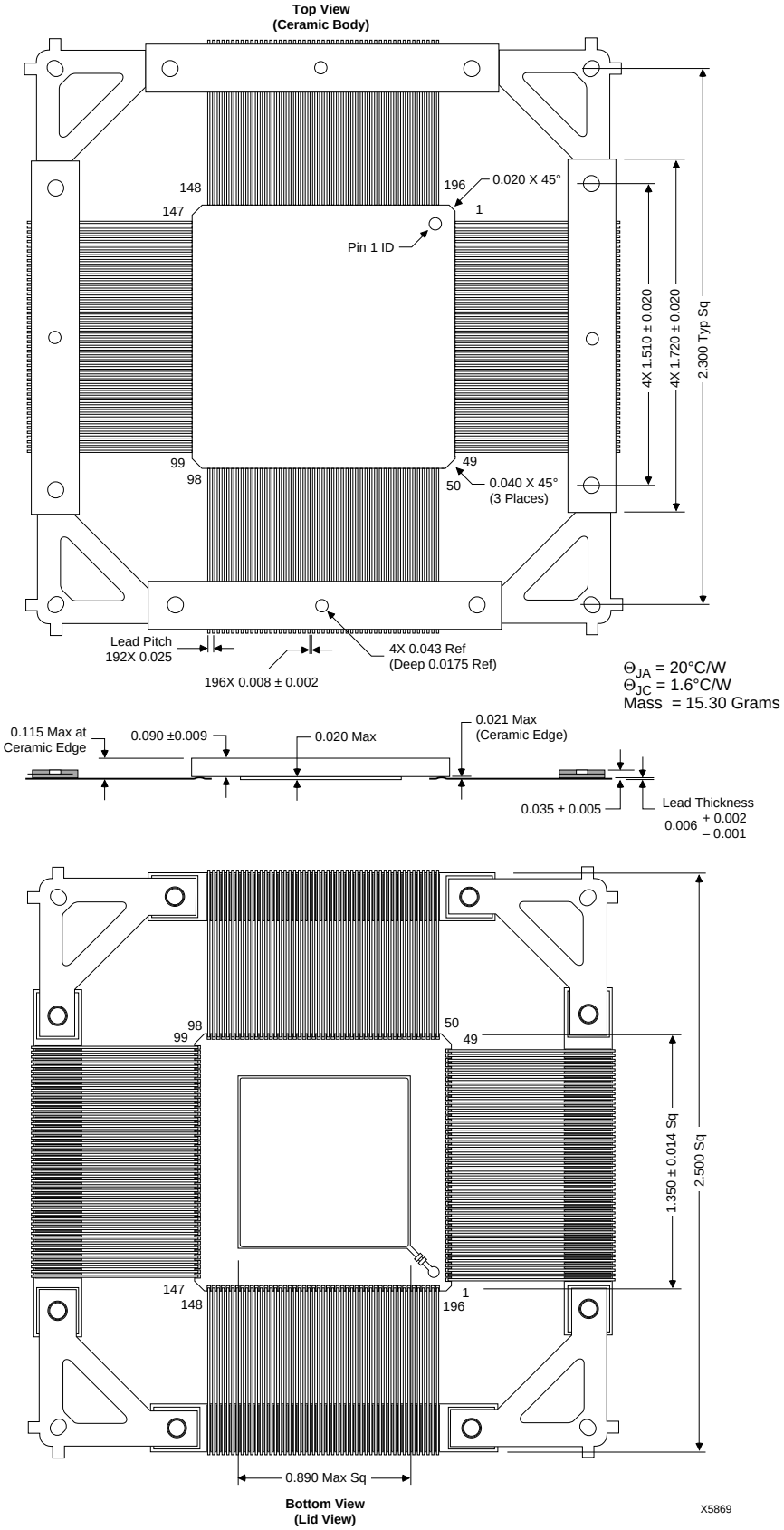
* Indicates unconnected package pins
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1= TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

Package Outline



191-Pin Ceramic PGA (PG191)

Package Outline



196-Pin Ceramic QFP (CB196)

XC4013 Pinouts

Pin Description	PG223	CB228	Bound Scan
VCC	J4	P201	-
I/O (A8)	J3	P202	74
I/O (A9)	J2	P203	77
I/O	J1	P204	80
I/O	H1	P205	83
I/O	H2	P206	86
I/O	H3	P207	89
I/O (A10)	G1	P208	92
I/O (A11)	G2	P209	95
VCC	-	P210	-
I/O	H4	P211	98
I/O	G4	P212	101
I/O	F1	P213	104
I/O	E1	P214	107
GND	G3	P215	-
I/O	F2	P216	110
I/O	D1	P217	113
I/O	C1	P218	116
I/O	E2	P219	119
I/O (A12)	F3	P220	122
I/O (A13)	D2	P221	125
I/O	F4	P222	128
I/O	E4	P223	131
I/O	B1	P224	134
I/O	E3	P225	137
I/O (A14)	C2	P226	140
SGCK1 (A15, I/O)	B2	P227	143
VCC	D3	P228	-
GND	D4	P1	-
PGCK1 (A16, I/O)	C3	P2	146
I/O (A17)	C4	P3	149
I/O	B3	P4	152
I/O	C5	P5	155
I/O (TDI)	A2	P6	158
I/O (TCK)	B4	P7	161
I/O	C6	P8	164
I/O	A3	P9	167
I/O	B5	P10	170
I/O	B6	P11	173
I/O	D5	P12	176
I/O	D6	P13	179
GND	C7	P14	-
I/O	A4	P15	182
I/O	A5	P16	185
I/O (TMS)	B7	P17	188
I/O	A6	P18	191
VCC	-	VCC	-
I/O	D7	P19	194
I/O	D8	P20	197
I/O	C8	P21	200
I/O	A7	P22	203
I/O	B8	P23	206
I/O	A8	P24	209
I/O	B9	P25	212
I/O	C9	P26	215
GND	D9	P27	-
VCC	D10	P28	-
I/O	P29	P29	218

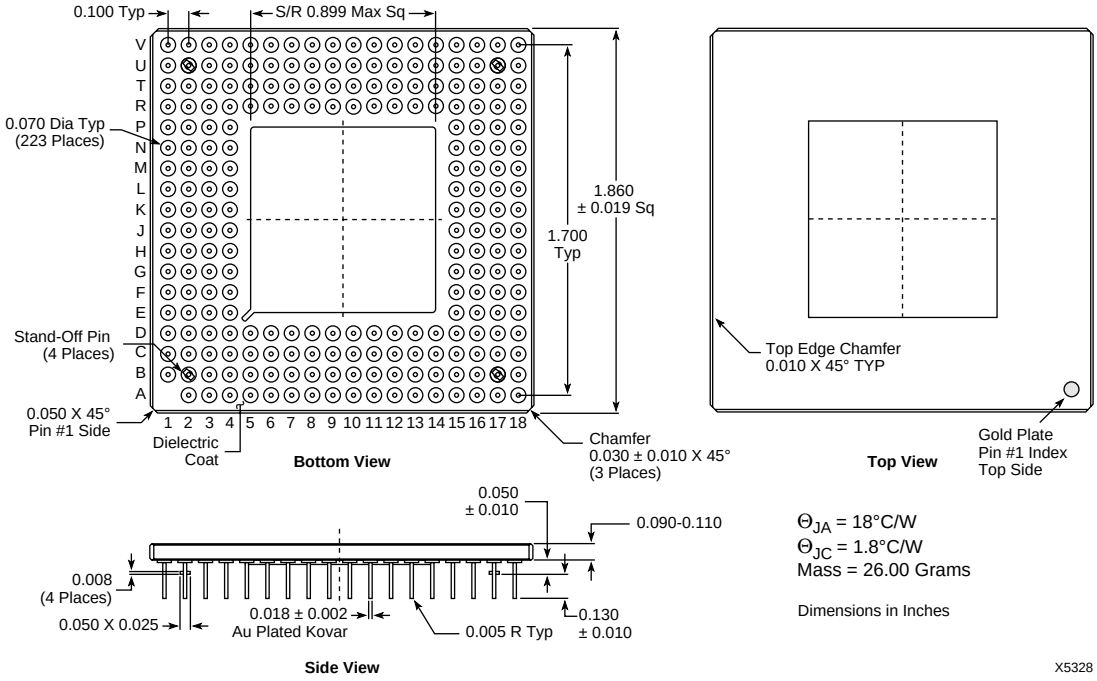
Pin Description	PG223	CB228	Bound Scan
I/O	B10	P30	221
I/O	A9	P31	224
I/O	A10	P32	227
I/O	A11	P33	230
I/O	C11	P34	233
I/O	D11	P35	236
I/O	D12	P36	239
VCC	-	P37	-
I/.O	B11	P38	242
I/O	A12	P39	245
I/O	B12	P40	248
I/O	A13	P41	251
GND	C12	P42	-
I/O	D13	P43	254
I/O	D14	P44	257
I/O	B13	P45	260
I/O	A14	P46	263
I/O	A15	P47	266
I/O	C13	P48	269
I/O	B14	P49	272
I/O	A16	P50	275
I/O	B15	P51	278
I/O	C14	P52	281
I/O	A17	P53	284
SGCK2 (I/O)	B16	P54	287
M1	C15	P55	290
GND	D15	P56	-
M0	A18	P57	293
VCC	D16	P58	-
M2	C16	P59	294
PGCK2 (I/O)	B17	P60	295
I/O (HDC)	E16	P61	298
I/O	C17	P62	301
I/O	D17	P63	304
I/O	B18	P64	307
I/O (LDC)	E17	P65	310
I/O	F16	P66	313
I/O	C18	P67	316
I/O	D18	P68	319
I/O	F17	P69	322
I/O	E15	P70	325
I/O	F15	P71	328
GND	G16	P72	-
I/O	E18	P73	331
I/O	F18	P74	334
I/O	G17	P75	337
I/O	G18	P76	340
VCC	-	VCC	-
I/O	H16	P77	343
I/O	H17	P78	346
I/O	G15	P79	349
I/O	H15	P80	352
I/O	H18	P81	355
I/O	J18	P82	358
I/O	J17	P83	361
I/O ($\overline{\text{ERR}}$,$\overline{\text{INT}}$)	J16	P84	364
VCC	-	P85	-
GND	-	P86	-

XC4013 Pinouts (continued)

Pin Description	PG223	CB228	Bound Scan
VCC	J15	P85	-
GND	K15	P86	-
I/O	K16	P87	367
I/O	K17	P88	370
I/O	K18	P89	373
I/O	L18	P90	376
I/O	L17	P91	379
I/O	L16	P92	382
I/O	L15	P93	385
I/O	M15	P94	388
VCC	-	P95	-
I/O	M18	P96	391
I/O	M17	P97	394
I/O	N18	P98	397
I/O	P18	P99	400
GND	M16	P100	-
I/O	N15	P101	403
I/O	P15	P102	406
I/O	N17	P103	409
I/O	R18	P104	412
I/O	T18	P105	415
I/O	P17	P106	418
I/O	N16	P107	421
I/O	T17	P108	424
I/O	R17	P109	427
I/O	P16	P110	430
I/O	U18	P111	433
SGCK3 (I/O)	T16	P112	436
GND	R16	P113	-
DONE	U17	P114	-
VCC	R15	P115	-
$\overline{\text{PROG}}$	V18	P116	-
I/O (D7)	T15	P117	439
PGCK3 (I/O)	U16	P118	442
I/O	T14	P119	445
I/O	U15	P120	448
I/O	R14	P121	451
I/O	R13	P122	454
I/O (D6)	V17	P123	457
I/O	V16	P124	460
I/O	T13	P125	463
I/O	U14	P126	466
I/O	V15	P127	469
I/O	V14	P128	472
GND	T12	P129	-
I/O	R12	P130	475
I/O	R11	P131	478
I/O	U13	P132	481
I/O	V13	P133	484
VCC	-	**VCC**	-
I/O (D5)	U12	P134	487
I/O ($\overline{\text{CS0}}$)	V12	P135	490
I/O	T11	P136	493
I/O	U11	P137	496
I/O	V11	P138	499
I/O	V10	P139	502
I/O (D4)	U10	P140	505
I/O	T10	P141	508
VCC	R10	P142	-

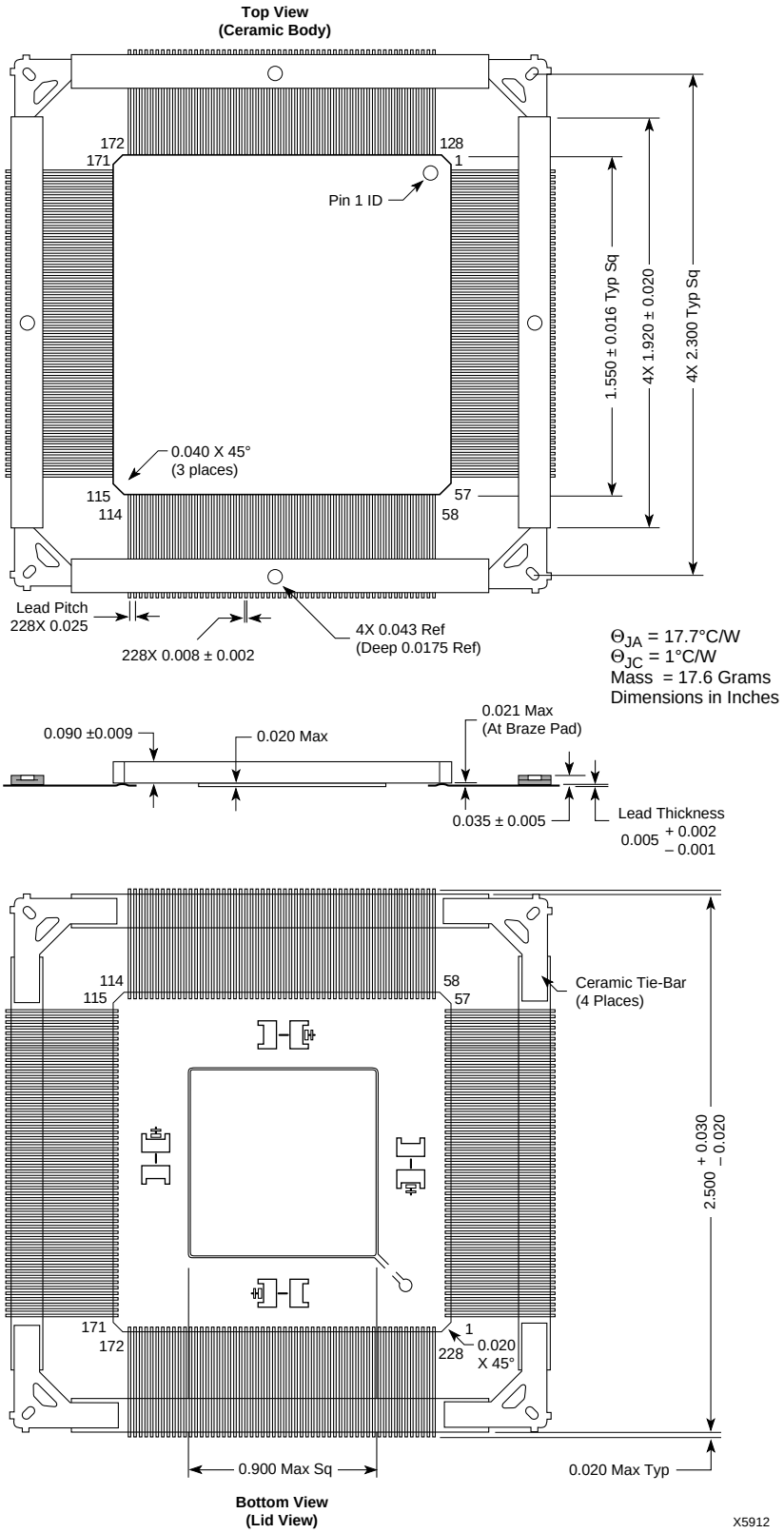
Pin Description	PG223	CB228	Bound Scan
GND	R9	P143	-
I/O (D3)	T9	P144	511
I/O ($\overline{\text{/RS}}$)	U9	P145	514
I/O	V9	P146	517
I/O	V8	P147	520
I/O	U8	P148	523
I/O	T8	P149	526
I/O (D2)	V7	P150	529
I/O	U7	P151	532
VCC	-	P152	-
I/O	V6	P153	535
I/O	U6	P154	538
I/O	R8	P155	541
I/O	R7	P156	544
GND	T7	P157	-
I/O	R6	P158	547
I/O	R5	P159	550
I/O	V5	P160	553
I/O	V4	P161	556
I/O	U5	P162	-
I/O	T6	P163	559
I/O (D1)	V3	P164	562
I/O ($\overline{\text{RCLK}}$, $\overline{\text{BUSY}}$/RDY)	V2	P165	565
I/O	U4	P166	568
I/O	T5	P167	571
I/O (D0, DIN)	U3	P168	574
SGCK4 (DOUT, I/O)	T4	P169	577
CCLK	V1	P170	-
VCC	R4	P171	-
TDO	U2	P172	-
GND	R3	P173	-
I/O (A0, $\overline{\text{WS}}$)	T3	P174	2
PGCK4 (I/O, A1)	U1	P175	5
I/O	P3	P176	8
I/O	R2	P177	11
I/O (CS1, A2)	T2	P178	14
I/O (A3)	N3	P179	17
I/O	P4	P180	20
I/O	N4	P181	23
I/O	P2	P182	26
I/O	T1	P183	29
I/O	R1	P184	32
I/O	N2	P185	35
GND	M3	P186	-
I/O	P1	P187	38
I/O	N1	P188	41
I/O	M4	P189	44
I/O	L4	P190	47
VCC	-	P191	-
I/O (A4)	M2	P192	50
I/O (A5)	M1	P193	53
I/O	L3	P194	56
I/O	L2	P195	59
I/O	L1	P196	62
I/O	K1	P197	65
I/O (A6)	K2	P198	68
I/O (A7)	K3	P199	71
GND	K4	P200	-

Package Outline



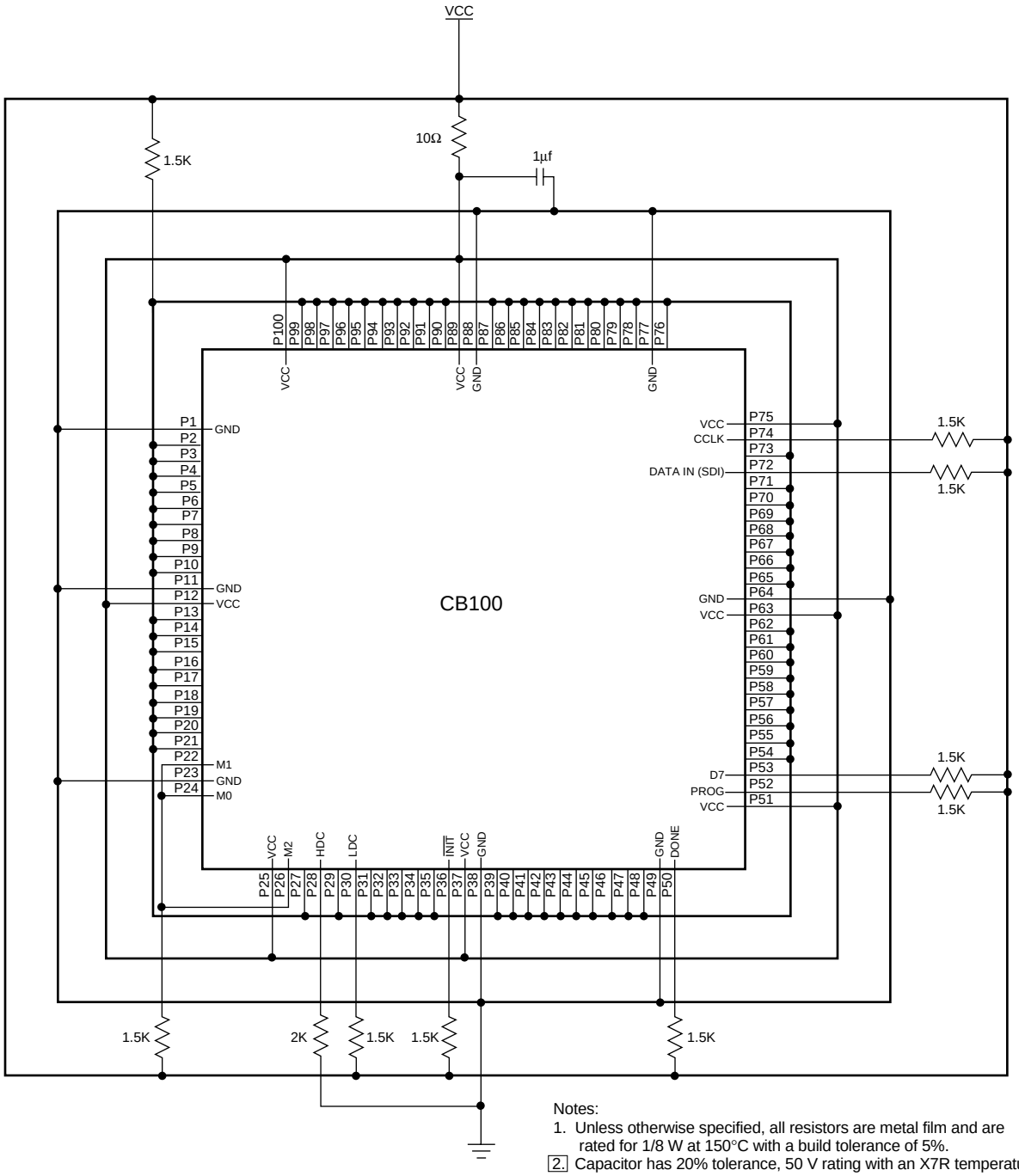
223-Pin Ceramic PGA (PG223)

Package Outline



228-Pin Ceramic QFP (CB228)

Static Burn-In Circuit

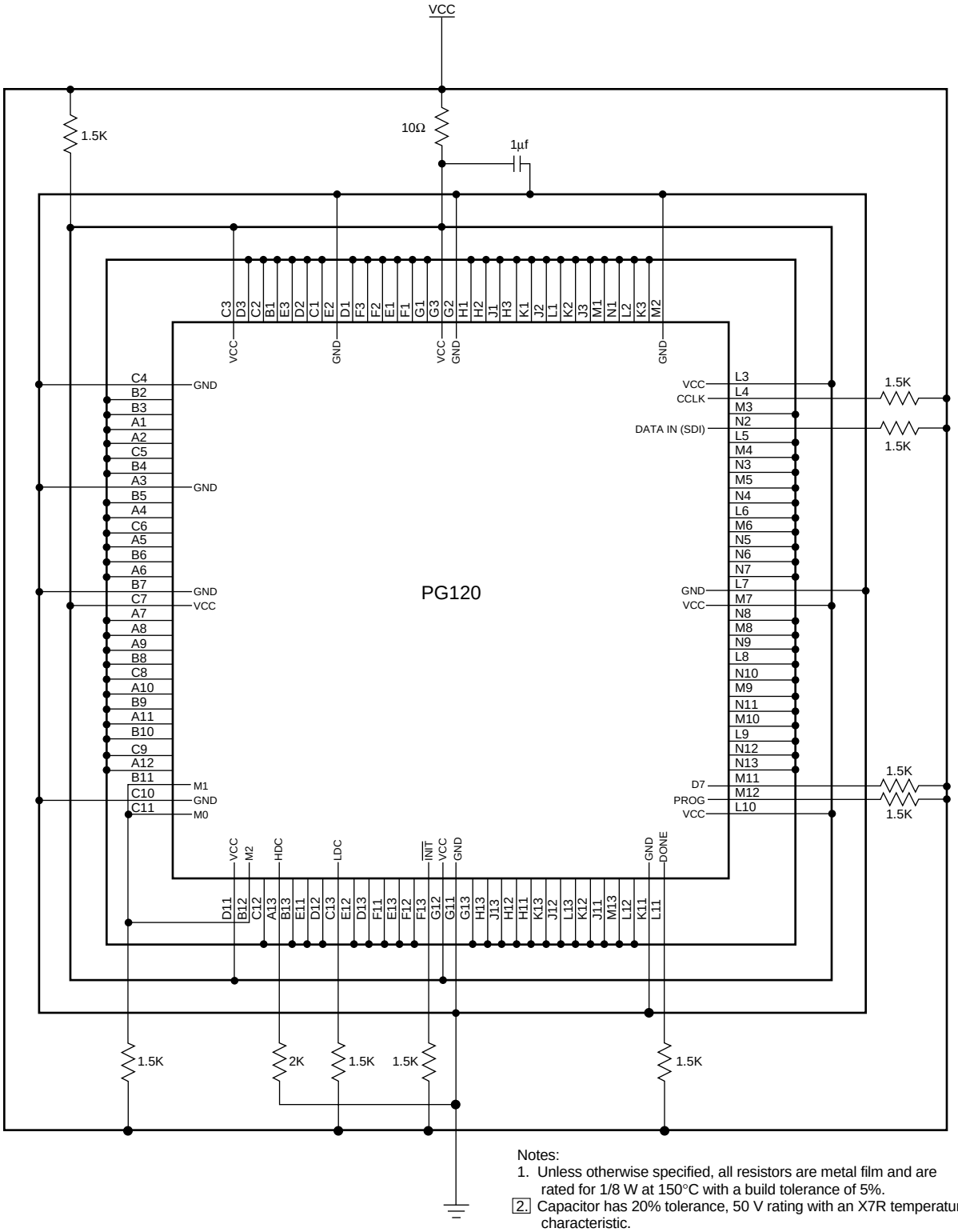


Notes:
1. Unless otherwise specified, all resistors are metal film and are rated for 1/8 W at 150°C with a build tolerance of 5%.
2. Capacitor has 20% tolerance, 50 V rating with an X7R temperature characteristic.
3. 10 Ω resistor is metal oxide and is rated for 1 W at 150°C with a tolerance of 5%.

X7139

XC4003A (CB100)

Static Burn-In Circuit

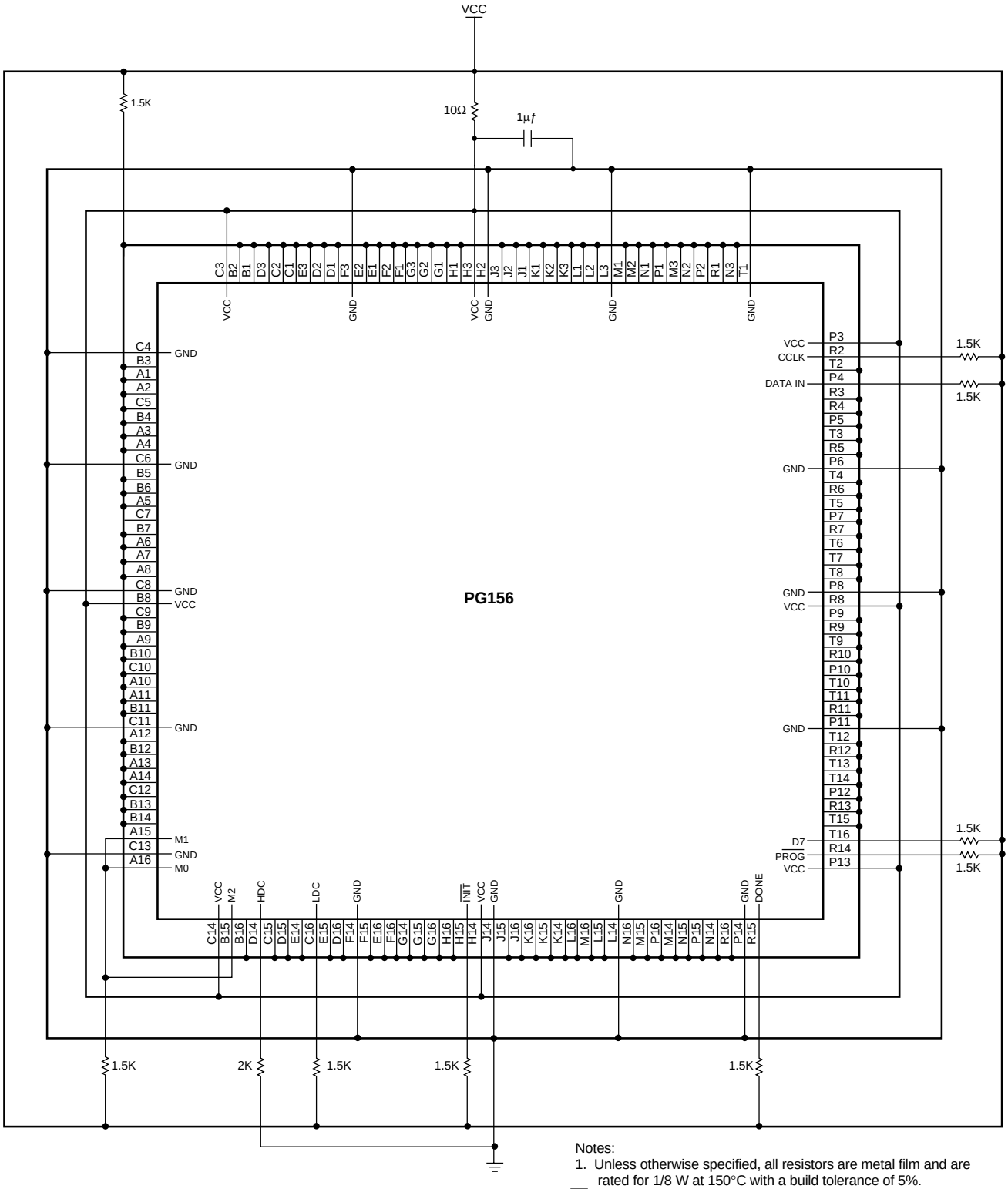


Notes:
1. Unless otherwise specified, all resistors are metal film and are rated for 1/8 W at 150°C with a build tolerance of 5%.
2. Capacitor has 20% tolerance, 50 V rating with an X7R temperature characteristic.
3. 10 Ω resistor is metal oxide and is rated for 1 W at 150°C with a tolerance of 5%.

X7138

XC4003A (PG120)

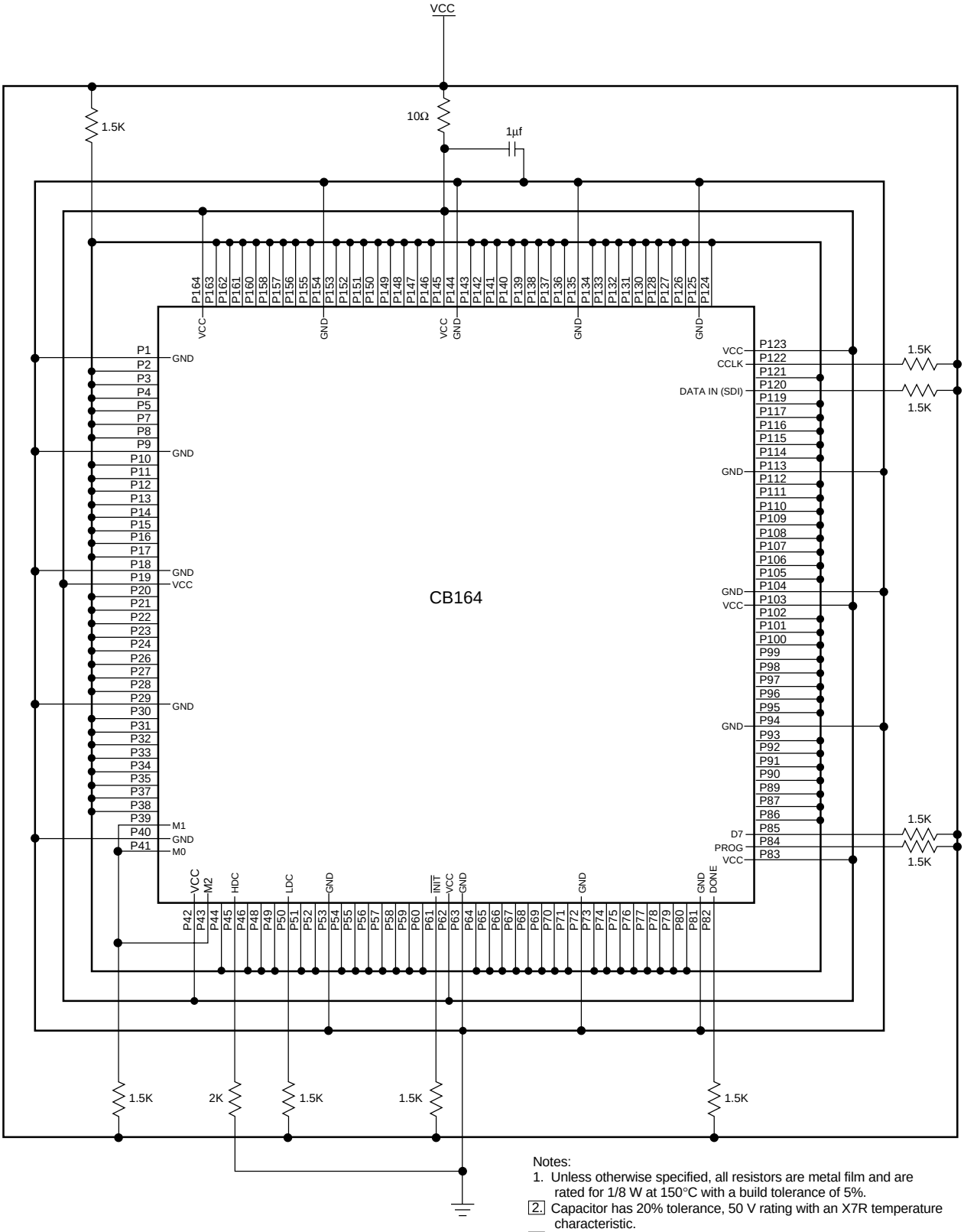
Static Burn-In Circuit



Notes:
1. Unless otherwise specified, all resistors are metal film and are rated for 1/8 W at 150°C with a build tolerance of 5%.
2. Capacitor has 20% tolerance, 50 V rating with an X7R temperature characteristic.
3. 10 Ω resistor is metal oxide and is rated for 1 W at 150°C with a tolerance of 5%.

X7137

Static Burn-In Circuit

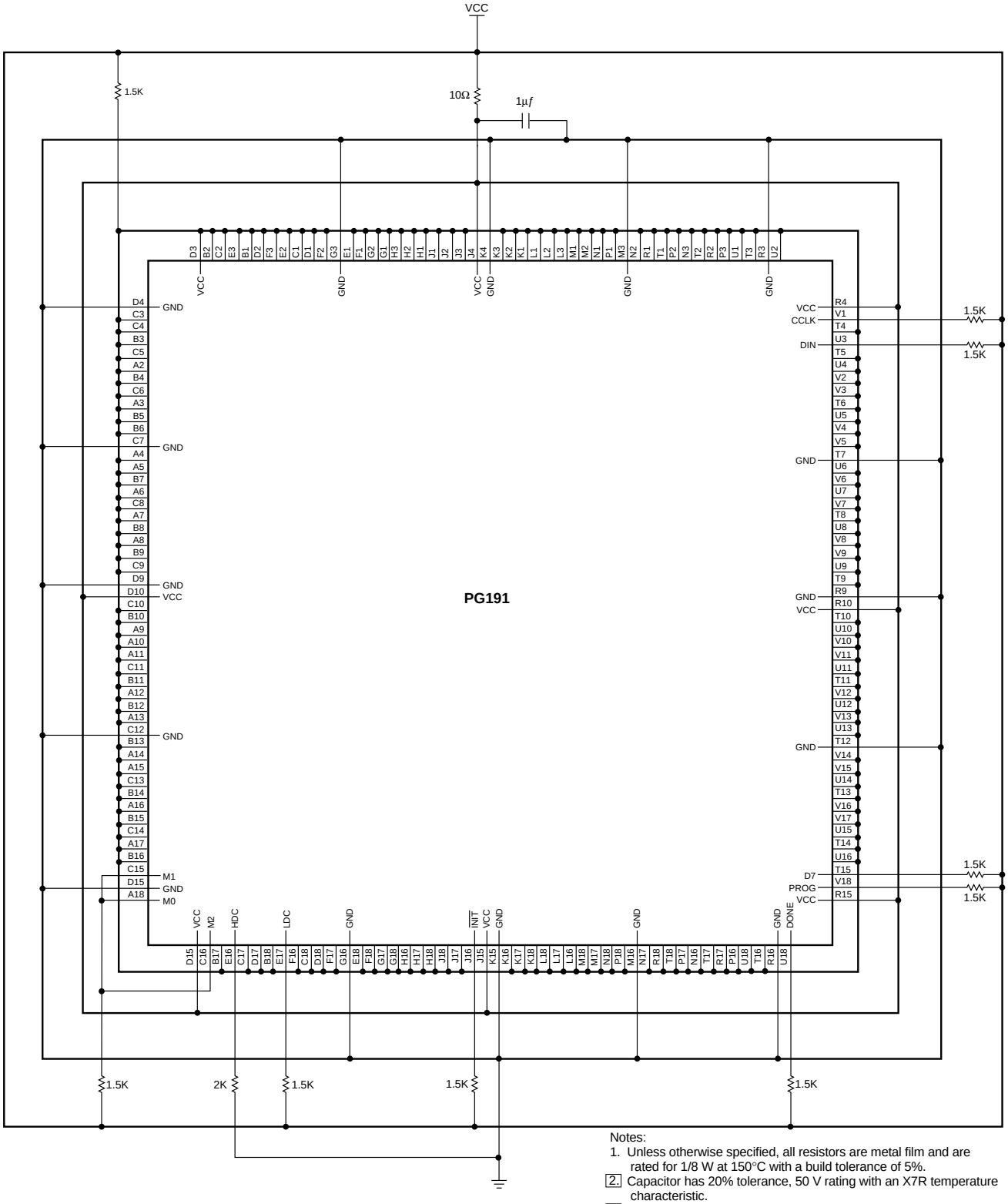


Notes:
1. Unless otherwise specified, all resistors are metal film and are rated for 1/8 W at 150°C with a build tolerance of 5%.
2. Capacitor has 20% tolerance, 50 V rating with an X7R temperature characteristic.
3. 10 Ω resistor is metal oxide and is rated for 1 W at 150°C with a tolerance of 5%.

X7136

XC4005 (CB164)

Static Burn-In Curcuit

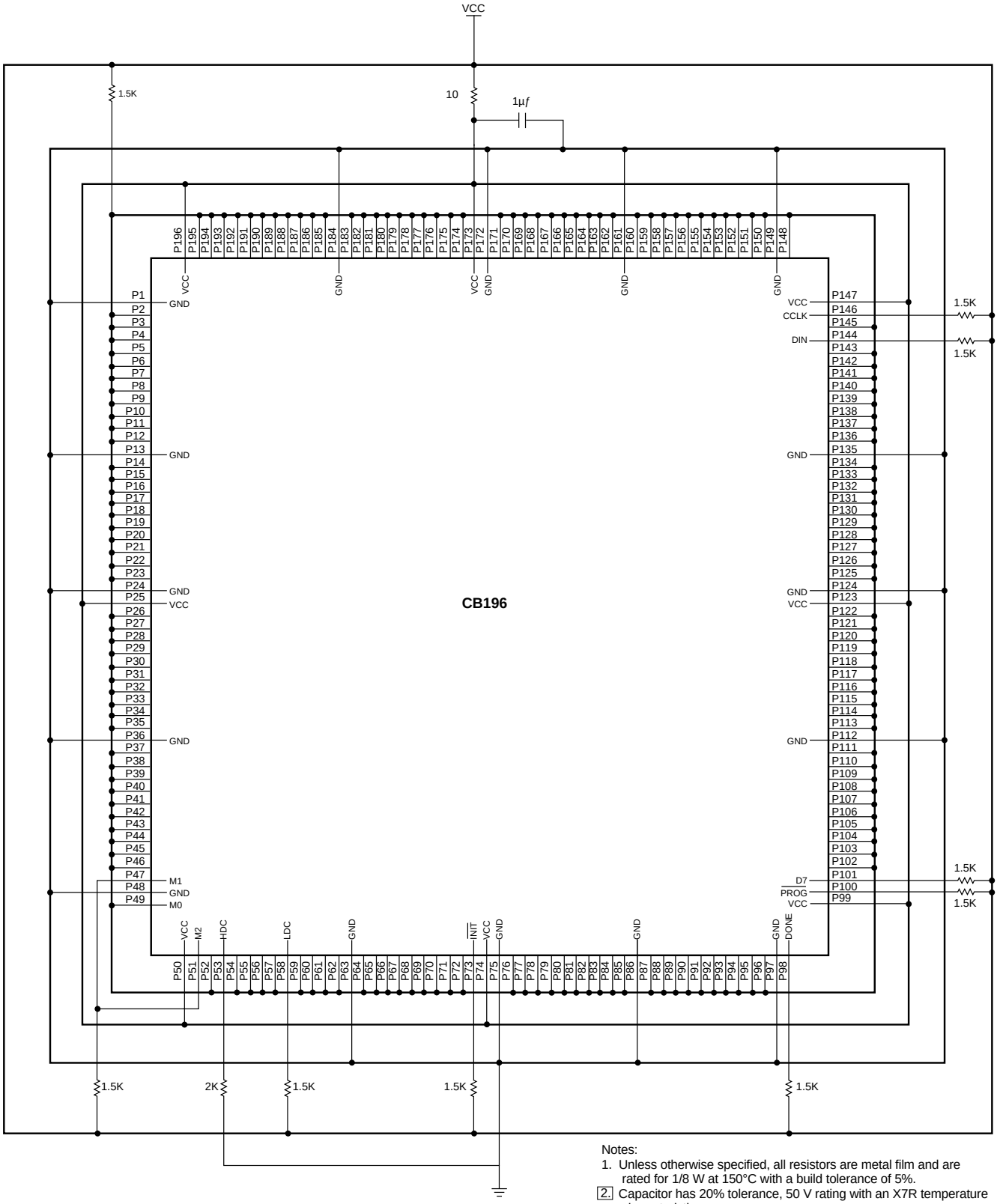


Notes:
1. Unless otherwise specified, all resistors are metal film and are rated for 1/8 W at 150°C with a build tolerance of 5%.
2. Capacitor has 20% tolerance, 50 V rating with an X7R temperature characteristic.
3. 10 Ω resistor is metal oxide and is rated for 1 W at 150°C with a tolerance of 5%.

X7135

XC4010 (PG191)

Static Burn-In Circuit

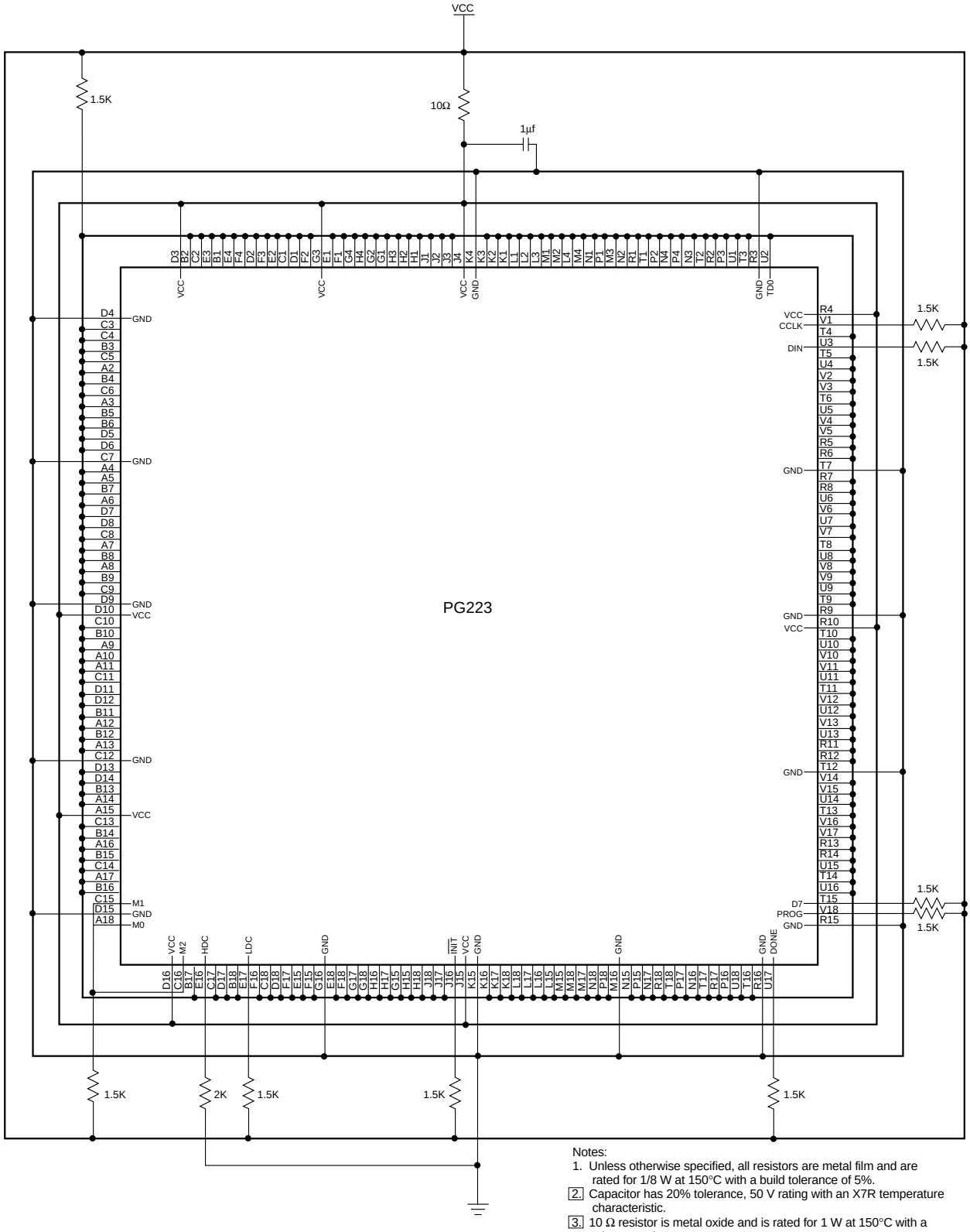


Notes:
1. Unless otherwise specified, all resistors are metal film and are rated for 1/8 W at 150°C with a build tolerance of 5%.
2. Capacitor has 20% tolerance, 50 V rating with an X7R temperature characteristic.
3. 10 Ω resistor is metal oxide and is rated for 1 W at 150°C with a tolerance of 5%.

X6569

XC4010 (CB196)

Static Burn-In Circuit

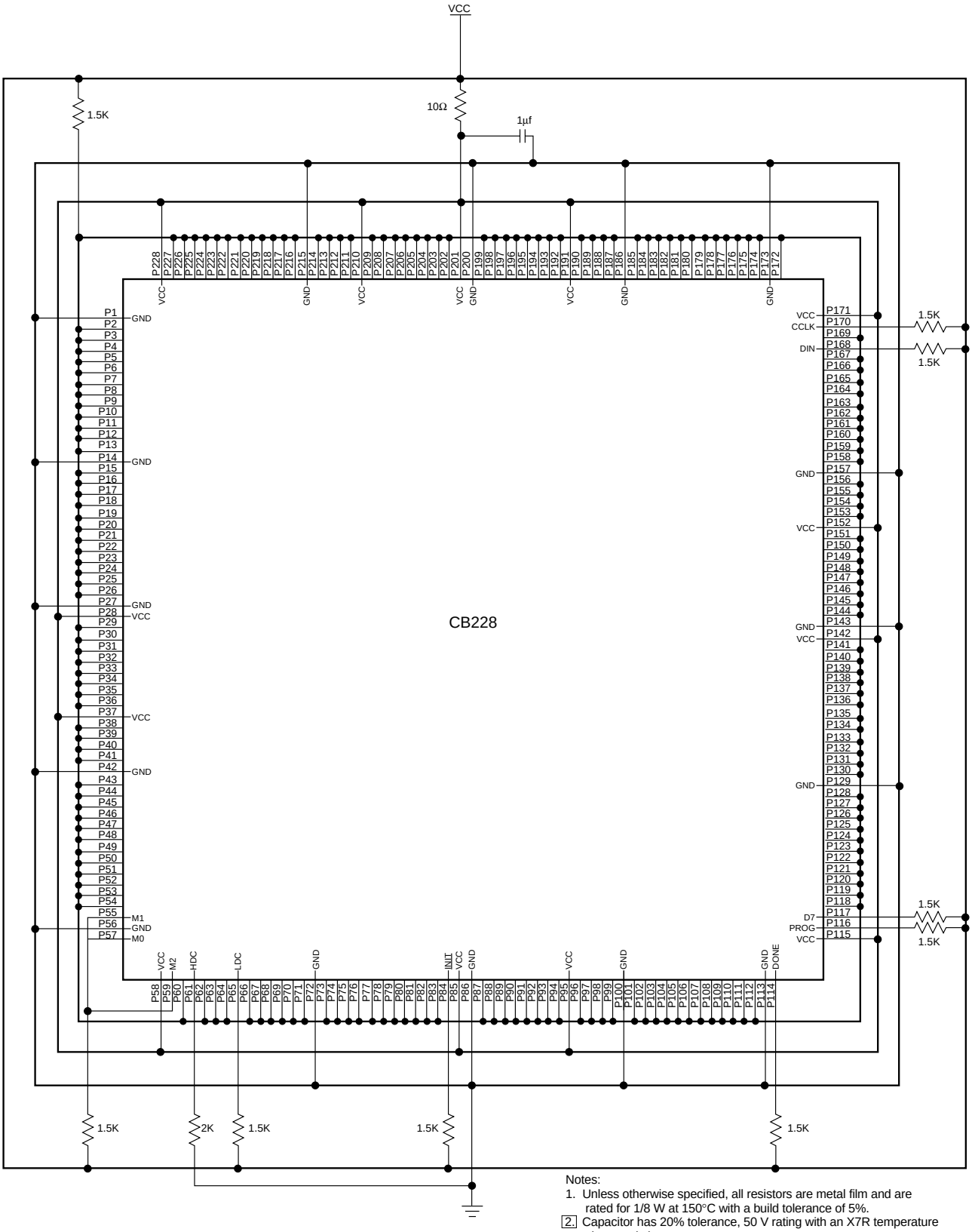


Notes:
1. Unless otherwise specified, all resistors are metal film and are rated for 1/8 W at 150°C with a build tolerance of 5%.
2. Capacitor has 20% tolerance, 50 V rating with an X7R temperature characteristic.
3. 10 Ω resistor is metal oxide and is rated for 1 W at 150°C with a tolerance of 5%.

X7134

XC4013 (PG223)

Static Burn-In Circuit



XC4013 (CB228)

Absolute Maximum Ratings

		Limits	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 ns @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature	+150	°C

Note: Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

-55 °C≤T_C≤+125°C, VCC = 5.0 V ±10%		**Group A Subgroups**	**Min**	**Max**	**Units**
V_{IH}	High-level input voltage (XC4000 has TTL-like input thresholds)	1, 2, 3		V_{CC}	V
V_{IL}	Low-level input voltage (XC4000 has TTL-like input thresholds)	1, 2, 3		0.8	V
T_{IN}	Voltage applied to 3-state output			250	ns

DC Characteristics Over Operating Conditions

-55 °C≤T_C≤+125°C, VCC = 5.0 V ±10%		**Group A Subgroups**	**Min**	**Max**	**Units**
V_{OH}	High-level input voltage @ I_{OH} = -4.0 mA, V_{CC} min	1, 2, 3	2.4		V
V_{OL}	Low-level input voltage @ I_{OL} = 4.0 mA (XC4005/XC4010/XC4013) I_{OL} = 8.0 mA (XC4003A)	1, 2, 3		0.4	V
I_{CCO}	Quiescent LCA supply current (Note 2)	1, 2, 3		50	mA
I_{IL}	Leakage current	1, 2, 3	-10	+10	µA
C_{IN}	Input capacitance (sample tested)	1, 2, 3		16	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V	1, 2, 3		0.5	mA
I_{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low XC4003A, XC4005 XC4010, XC4013	1, 2, 3		 2.5 5.0	 mA mA

Note: 1. With 50% of the outputs simultaneously sinking 4 mA (XC4005/XC4010/XC4013) or 8 mA (XC4003A).

2. With no output current loads, no active input or long line pull-resistors, all package pins at VCC or GND, and the LCA configured with a MakeBits “tie” option.

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