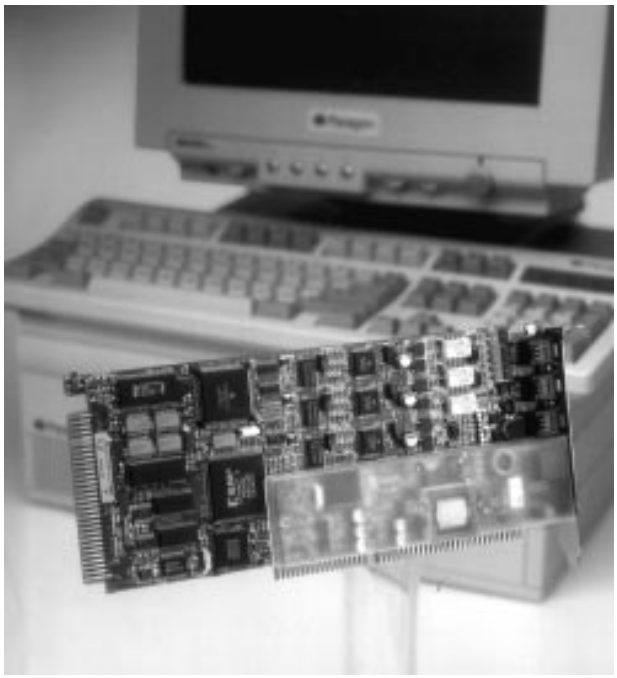
FPGAs Go "Down Under" in an

Engineers at communications equipment specialist Tennyson Technologies (Notting Hill, Victoria, Australia) are experienced users of Xilinx XC3000 and XC4000 series FPGAs. Thus, when a new project created a need for high integration levels, design flexibility, and a fast time-to-market, all at a reasonable cost, it was no surprise that they turned to the latest Xilinx FPGA technology — the XC5200 series. In Tennyson's new MicroAccess PCTA terminal adapter card, both bus interface and communication control functions are integrated into a single XC5206-6 FPGA device.



The MicroAccess system includes a plug-in card for PC systems and the accompanying software. It allows any PC or PC LAN to automatically make connections to off-site systems; the connection can be made to last only as long as information is being exchanged, much like a telephone call. With support for voice and data transfers, the MicroAccess system permits connectivity through ISDN, regular telephone line or X.25 services.

The logic functions implemented in the FPGA device include the ISA-bus interface, FIFO control, communications control, V110 rate adaptation, data compression/decompression, and other glue logic. The bus interface supports plug-and-play capability and accounts for about one-half of the logic in the FPGA. The bulk of the communications control logic consists of the counters used to assemble and synchronize the frames of data. About 75% of the available CLBs are used in this design, as well as most of the I/O pins available on the PQ208 package.

While any of several FPGA families could have provided the required density and functionality, Tennyson's engineers were attracted to the XC5200 architecture's VersaRing™ feature, in which extra routing channels around the perimeter of the array increase the flexibility of I/O connections. In order to meet the time-to-market goals, the designers realized that the printed circuit board (PCB) would need to be designed in parallel with the system's logic. Thus, the pinout for the XC5206 FPGA was fixed prior to the design of its internal logic. Through each design iteration, the VersaRing concept held true; changes to the FPGA design did not force any changes to the original PCB layout.

The flexibility provided by the SRAM-based FPGA was key to the successful design of the system. For example, the board was originally intended to support a 16-bit ISA bus interface only, but the specification was later changed to require support for both 8-bit XT and 16-bit AT systems. Since the entire bus interface is implemented in the FPGA, this requirement was accommodated, without requiring changes to the PCB layout as a result.

Taking advantage of the in-system-programmable FPGA technology, the MicroAccess board has been designed in anticipation of future field upgrades. New

ISDN Terminal Adapter

software (stored in Flash memory on the board) and new FPGA configuration programs can be downloaded to units in the field via an ISDN interface. In fact, one set of FPGA configuration programs has been dubbed the "Emergency Xilinx" diagnostic mode; this configuration runs just the ISDN channel, allowing for the downloading of new software and configuration bitstreams to the system.

Tennyson Technology's development environment is PC-based, and includes Viewlogic System's schematic editor and simulator, as well as the Xilinx XACT® development system. XACT-Performance™ time specifications and some floorplanning of the FPGA placement were used to meet the required 33 MHz system clock rate, a fairly aggressive goal when using the -6 speed grade. Both the Viewsim simulator and the X-Delay timing calculator were used to verify the functionality and timing of the FPGA design.

With the aid of Xilinx FPGAs, Tennyson Technology's MicroAccess system is allowing some of Australia's leading organizations to combine telephone and data traffic into single services, providing for better communications with branch offices and other remote locations while reducing overall communication costs. ◆