XC4085XL FPGA Sets New Density Standard

This May, Xilinx began shipping sample quantities of the new XC4085XL FPGA. The XC4085XL device is now the largest member of the XC4000XL family (a position previously held by the XC4062XL device). It is the industry's leading high-performance 3.3V FPGA solution, with 7,448 logic cells (3,136 CLBs) and 448 I/O blocks.

With the introduction of the high-density XC4062XL and XC4085XL devices, FPGA technology can now effectively address new, high-density markets such as telecommunications, data processing and industrial applications. As FPGA costs decline and densities increase, all gate array designers who are currently using devices with up to 100,000 gates can now secure the convenience and time-to-market benefits of FPGA technology.

The development system software for the XC4000XL family, available now, is included as part of the new XACT*step* version M1 design environment. The additional routing available in the XC4000XL family architecture, along with improved routing algorithms in the new M1 release, result in dramatically-reduced software compilation times for these high-density FPGAs.

The XC4085XL device is available in 560-pin super ball grid array and 559-pin pin grid array packages. Please contact your local Xilinx sales representative for the latest price and availability information. ◆

Extends Density of XC4000XL FPGA Family by 40%

XC6264 Added to XC6200 Family of RPUs

Xilinx recently announced the addition of the 64,000-gate XC6264 device to the XC6200 family of reconfigurable processing units (RPUs). The XC6264 and XC6216 RPUs are the only programmable logic devices that have been optimized for reconfigurable logic applications such as real-time adaptive filtering and algorithm acceleration.

While FPGAs traditionally have been used to implement individual logic designs, RPUs are intended to support multiple designs in a single piece of silicon — either by "swapping out" unnecessary pieces of a design to save silicon space or by changing logic on-the-fly to increase performance.

Innovative XC6200 features such as fast partial reconfiguration, a built-in microprocessor interface and an open bitstream format make RPUs the component of choice for system designers exploring or using dynamic hardware designs.

For more information on the XC6200 RPU family, visit WebLINX at www.xilinx.com. ◆