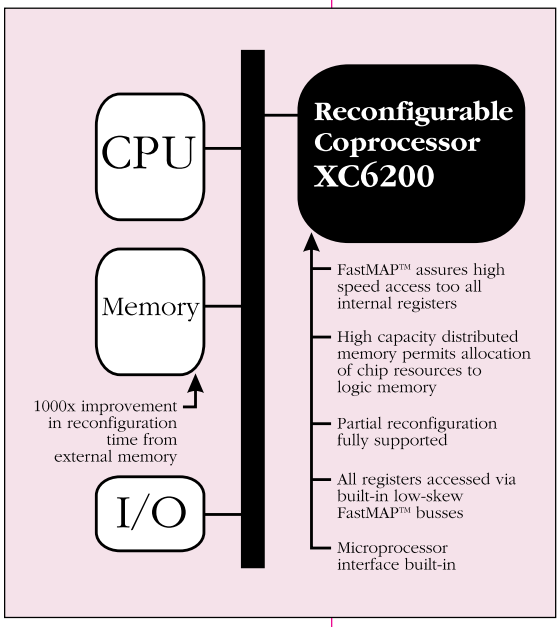
Introducing the XC6200 FPGA Architecture:

Reconfigurable processing refers to the use of in-system-programmable FPGAs as processing elements, combining the versatility of a programmable solution with the performance of dedicated hardware. *(See XCELL #16.)* Most FPGA-based processors are implemented as coprocessors dedicated to offloading computationally-intensive tasks from a host processor; in other words, the main program is executed by a traditional processor, and certain tasks are assigned to the FPGA-based coprocessor to accelerate their execution.

This approach exploits the fact that most of the processing time for compute-intensive tasks is spent in relatively small portions of the code, and hardware acceleration can significantly improve overall performance. Tasks can be swapped in and out of the coprocessor as needed through reconfiguration of the FPGAs.



Today's FPGA architectures are being used to construct reconfigurable coprocessors. (The XC4000 FPGA family, with it's on-chip memory capability, has been particularly popular for reconfigurable computing applications.) However, these general-purpose architectures have some limitations.

The interface to the main processor's bus must be implemented using programmable logic resources in the FPGA, which may consume a significant portion of the FPGA resources. The internal FPGA architectures are not always optimal for the data-path algorithms typical of coprocessing applications. Providing bus access to large numbers of internal registers requires careful design. On-chip memory capacities are too small for some algorithms. Reconfiguration times are relatively long (several milliseconds) for computing operations, and partial reconfiguration (reconfiguring just a portion of the FPGA) is difficult.

These limitations have been addressed in the new XC6200 FPGA architecture — an SRAM-based FPGA architecture specifically designed for implementing reconfigurable coprocessors in embedded system applications. The XC6200 architecture features a built-in processor interface, a fine-grained cell structure, abundant routing, and support for fast partial or full reconfiguration. The register-rich XC6200 is ideally suited for computationally-intensive datapath applications.

XC6200 FPGA Architectural Features

- **FastMAP™ interface.** Besides the usual progammable I/O, the XC6200 architecture includes a dedicated interface, called the FastMAP interface, designed to connect directly to a host processor bus. The interface can be configured for a 32-bit, 16-bit or 8-bit interface. This built-in, memory-like interface simplifies system design and directly interfaces to most embedded processors without consuming any FPGA resources. The FastMAP interface provides high-speed access to all internal registers in the logic cells. Any register can be mapped into the memory address space of the host processor, allowing for simple hardware and fast data transfers.
- **Ultra fast configuration and reconfiguration.** The FastMAP interface also provides ultra-fast configura-

The First FPGA Architecture Optimized for Coprocessing in Embedded System Applications

tion capability — up to 1,000 times faster than traditional FPGAs. System performance is further improved by the dynamic partial configuration capability, allowing the modification of parts of the FPGA while the other algorithms in the FPGA continue uninterrupted. A serial configuration mode is available.

- **Flexible, fine-grained logic cell.** The programmable logic of an XC6200 FPGA is composed of a large array of simple, reconfigurable logic cells. Each cell contains both programmable logic and routing resources. The cells are simpler than previous FPGA generations, since coprocessing applications tend to be more regular and register-intensive than random logic. Each cell contains a flip-flop and combinatorial logic capable of implementing any two-input function or any type of 2-to-1 multiplexer. Cells are arranged in 4-by-4 blocks and 16-by-16 tiles.
- **High capacity distributed memory.** The very nature of coprocessing demands varying amounts of memory depending on the algorithm being executed at a given time. The XC6200 addresses this by offering high-capacity distributed memory that the user can tailor to suit the application. Each cell can be used for either logic or memory functions. In the memory mode, each cell can be configured to provide two bytes of ROM or RAM. This memory can be accessed via the FastMap interface, by logic implemented in the FPGA, or both.
- **Abundant routing resources.** Six different types of hierarchical routing resources are offered in the XC6200 architecture yielding fast predictable routing delays. In most other architectures these routing delays grow geometrically with distance, whereas in the XC6200 they grow logarithmically.
- **Symmetric architecture for position independent design mapping.** The XC6200 architecture is very symmetric in cell structure and routing resources, making it possible to implement designs that are position-independent. This ability to relocate designs within the FPGA can greatly increase utilization and provides greater latitude in swapping algorithms in and out of an XC6200 family FPGA.

The XC6200 Product Family

The initial product roadmap consists of devices with gate counts as high as 100K gates or memories as large as 256K bits. Products will become available over the next four quarters.

New XACT*step* Series 6000 Development System

The advanced XC6200 architecture has an equally advanced development system. The system fully exploits the architecture with the push of a button or give the designer complete hands-on control. At about 100 gates/second of place and route time, it's every bit as fast as the XC6200 architecture. ◆

Product	Function Cells	Usable Gates[1]	Max. Memory	Availability
XC6209	2304	9K ~ 14K	36K bytes	1H96
XC6216	4096	16K ~ 25K	64K bytes	4Q95
XC6236	9216	36K ~ 56K	144K bytes	1H96
XC6264	16348	64K ~ 100K	256K bytes	2H96

[1]based upon 4~6 gates/function cell.