Low Power Benefits Of XC4000E/X: Overview

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Application Brief By: Richard Mitchell

Summary

The Xilinx XC4000E/EX/XL families offer low power architectures which have been optimized for high speed, high density operation, giving the customer reliable operation with many package options while satisfying the need for very high performance designs. Xilinx devices consume one half to one third the power of competitive devices.

Xilinx Family

XC4000E, XC4000EX, XC4000XL

Related Documents

XBRF 014, XBRF 015, XBRF 016, XBRF 017

Introduction

As the size and speed of today's FPGAs increase, power consumption also increases. With the increase in power consumption, the package power dissipation limit becomes a factor to be considered in the overall design evaluation process. In the days of low density/low speed designs, the designer could ignore the package power limit because the power consumption of designs was safely below the package limits (Figure 1). The designer today using high density/high speed devices must not only go through the process of evaluating how much logic can be packed into the device and whether the device will run at the required speed, the designer must also evaluate the expected power dissipation and evaluate if the desired package will handle the required power dissipation while maintaining the target device reliability.

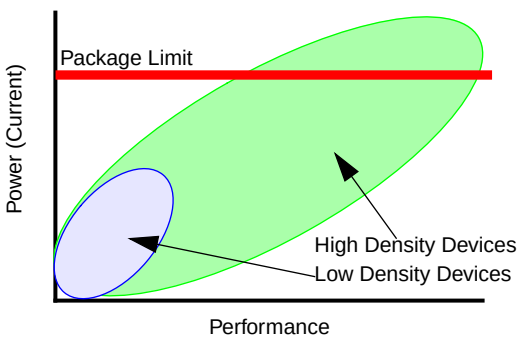

Figure 1: Package Power Limit

There are four design factors which are directly affected by the power consumption of the design and the package power dissipation limit. These limits are listed below and will each be covered in detail in other Application Briefs (XBRF 014-017).

The four design factors are;

- The device performance limit.
- The device utilization limit.
- The package options available.
- The device failure rate.

Device Architecture For Low Power Consumption

The device architecture directly affects the power efficiency which can be expected in any given design. Xilinx and Altera have each chosen different interconnect methodologies which inherently define the power associated with a given level of performance.

The XC4000E family as well as the new XC4000EX/XL families have been architected to minimize power consumption despite their large size and high speed operation. Specific architecture features such as the segmented interconnect (Figure 2) have been incorporated to minimizing line capacitances with line length control and buffering, while maintaining versatile logic cell connectivity and high performance.

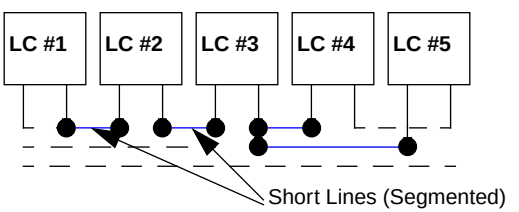

Figure 2: Xilinx Segmented Interconnect

Conversely Altera's 10K family continues the oversimplification of their interconnect structure with heavy reliance on global long lines (Figure 3). These long lines are inherently high capacitance lines and require large currents to switch the line as the device operates. The overall power dissipation is so high that a device like the 10K100 is only available in an expensive, ceramic PGA, which for most designs even require the fan and heatsink Altera specifies in their data sheet.

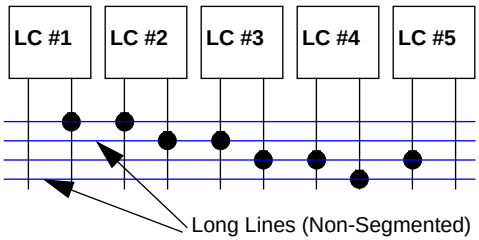

Figure 3: Altera Non-Segmented Interconnect

The power benefits which Xilinx achieves from using the segmented interconnect translates to between 125% and 221% lower power consumption for the same design implemented in Xilinx vs. Altera Device families

Measurement Methodology: Comparing Apples With Apples

Every design will have a different power consumption, based on many factors such as the number of signals which are switching, the speed at which each is switching, how often each signal switches, how many outputs are being used, the load each output is driving and how power efficient the specific device architecture is. The general equation for this is;

- Total I_{CC} = Static I_{CC} + Active I_{CC} + Output I_{CC}

The Static I_{CC} is the amount of current the device requires when it is inactive and is generally negligible in today's CMOS FPGAs. The Output I_{CC} of the device is the amount of current required to switch unloaded device outputs which again is usually negligible, however the loads that are applied to the device outputs can affect the power dissipation and must be estimated by the designer and considered in actual system designs. This leaves the Active I_{CC} which is a major portion of the overall power dissipation within a device. The Active I_{CC} is the current required to switch all the signals within the device and this is the current which will be evaluated and presented in the comparisons.

One Half To One Third Less Power Required Than Competition

In an effort to provide a direct comparison between Xilinx and Altera device I_{CC}, Xilinx used the methodology published in Altera's data sheets. The engineer can then compare the 10K device specifications with the same numbers for the Xilinx XC4000E/X devices derived using the identical methodology.

The measurement methodology is to fill a device with 16-bit counters (12.5% of the signals toggling at any clock edge) all running with no loads. The device I_{CC} is measured as the clock frequency is varied from around 1 MHz to 80-100 MHz. The device architecture current scale factor ("K" factor) is then calculated using the following equation.

- Active I_{CC} = K * #LEs * F_{CLK} * $\%_{TOG}$
  - I_{CC} = device active current in uA
  - K = device architecture current scale factor
  - #LEs = number of signals switching
  - F_{CLK} = device clock frequency in MHz
  - $\%_{TOG}$ = percent of signals switching each clock edge.

This equation is used by Altera for use in estimating the power required by one of their devices. The equation has some limitations which makes it inaccurate for designs that don't switch 12.5% of the time. Most real designs don't switch at this precise rate. The 12.5% figure is derived from a 16-bit counter which is what was used to do the measurements. Real device designs run all the way from a few at < 10% through the more common 20-25% up to a few at >50% (large shift register type designs).

Xilinx recommends that these numbers be used for comparison purposes only because they are only accurate at 12.5% toggling (for 16-bit counters).

Xilinx measured several of its devices in the XC4000E, XC4000EX and XC4000XL families. A few competitor devices were also measured to validate the measurements against the data sheet specifications. The "K" factors are shown in Table 1. As can be seen from the equation above, the lower the "K" factor the lower the current.

Xilinx	K	K	Altera
4013E	72	98	10K20
4028EX	47	101	10K40
4036EX	47	104	10K50
		93	10K70
		97	10K100
4036XL	29	45	10K50V
4062XL	29		

Table 1: Xilinx and Altera "K" Factors

Using the K factor

The “K” factor is used to compare the current requirements of different devices. For example with the same design placed in a 4036EX and a 10K50 the current ratio will be 47:104 or in other words the Altera device will require over 2X the amount of current as the Xilinx device. One of the benefits of using the first broad line of 3.3V FPGAs (XC4000XL family) is the large power savings. For example, compare a 4028XL with Altera‘s offering at that size, the 10K40. The ratio will be 29:101 or the 10K40 will require 3X more current than the 4028XL will need.

Conclusion

The XC4000E, XC4000EX and XC4000XL families have been designed from the ground up for low power high-speed, high-density operation. As shown in Table 1, the Xilinx devices offer lower Active I_{CC} than the Altera FLEX 10K. With the Xilinx device requiring only half the power that the Altera device requires for the same design, Xilinx delivers several advantages to the designer. The advantages are higher performance limits, higher utilization, more package options and lower die temperature giving higher device reliability.

XILINX® The Programmable Logic Company℠

Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
U.S.A.

Tel: 1 (800) 255-7778
or 1 (408) 559-7778
Fax: 1 (800) 559-7114

Net: hotline@xilinx.com
Web: http://www.xilinx.com

North America

Irvine, California
(714) 727-0780

Englewood, Colorado
(303)220-7541

Sunnyvale, California
(408) 245-9850

Schaumburg, Illinois
(847) 605-1972

Nashua, New Hampshire
(603) 891-1098

Raleigh, North Carolina
(919) 846-3922

West Chester, Pennsylvania
(610) 430-3300

Dallas, Texas
(214) 960-1043

Europe

Xilinx Sarl
Jouy en Josas, France
Tel: (33) 1-34-63-01-01
Net: frhelp@xilinx.com

Xilinx GmbH
Aschheim, Germany
Tel: (49) 89-99-1549-01
Net: dlhelp@xilinx.com

Xilinx, Ltd.
Byfleet, United Kingdom
Tel: (44) 1-932-349401
Net: ukhelp@xilinx.com

Japan

Xilinx, K.K.
Tokyo, Japan
Tel: (03) 3297-9191

Asia Pacific

Xilinx Asia Pacific
Hong Kong
Tel: (852) 2424-5200
Net: hongkong@xilinx.com

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