How to Evaluate the XC4000XL for Your Next Application

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A lot of data and applications information is available on our XC4000 FPGA families. This article will help you find what you need, focusing specifically on the XC4000XL. All page numbers listed here refer to the Xilinx 1998 Data Book, available in print, on the AppLINX #5 CD, and at www.xilinx.com.

If you have never used Xilinx FPGAs, read **XC3000, XC4000, and XC5200: A Technical Overview for the First Time User** (page13-5). This will give you a broad overview of the basic features common to all Xilinx FPGAs.

If you want to get a more detailed comparison between the different Xilinx FPGA families, read **Choosing a Xilinx Product Family** (page 13-7) and see the table on page 13-12. This will give you a feel for the relative advantages of the different families.

If you have narrowed your choice to the 3.3-V XC4000XL family, then see page 4-5, the first page of the data sheet, for a list of important features. The ten XC4000XL devices represent the most advanced evolution of the industry's most popular FPGAs — the XC4000 series. The XC4000XL family uses 0.35 micron technology to achieve the highest speed and the lowest power. This cutting-edge technology requires a 3.3-V supply, but all XC4000XL inputs and outputs are fully compatible with 5-V devices. You can thus mix devices using old and new-technology on the same PC board.

The basic advantages of all XC4000 families lie in their architectural features:

- SelectRAM offers thousands of very fast 16 x 1 bit RAMs with synchronous or asynchronous write; also configurable as dual-port RAMs.
- Dedicated carry logic speeds up arithmetic and counters
- Segmented routing supports high clock rates

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➤ Powerful I/O structures allow fast inter-chip operation.

The architecture of all XC4000-series devices is described on page 4-9. The functionality of the dedicated pins is described on page 4-41. The methods of configuring (programming or customizing) the devices are covered on page 4-46.

Capacity

The table on page 4-6 gives you a feel for the capacity of the 10 different XC4000XL family members. Logic capacity can be expressed in many different ways. The trailing digits of the part name describe the capacity in kilogates (e.g., the XC4010XL holds roughly 10,000 gates). However, gate-count is not really a meaningful metric — Xilinx FPGAs implement their logic in look-up tables, not in gate-array-like 2-input NAND gates.

Capacity is better described by Logic Cells, where each Logic Cell is one 4-input look-up table plus one flip-flop. Most designers have a good feel for the number of flip-flops required. It is reasonable to assume that less than two Logic Cells are needed for every flip-flop in a typical design. This allocates, on average, up to two look-up tables in front of each flip-flop. Highly structured and pipelined designs might use only one look-up table per flip-flop, and thus use only one Logic Cell per user flip-flop.

Speed

XC4000XL devices come in four speed grades: -09, -1, -2, and -3. The lower the number, the faster the device (read 09 as 0.9). Page 4-71 lists the delays of a large number of parameters inside the chip, and for the inputs and outputs. All parameters are guaranteed over the operating range of 0-to-85° C junction temperature and 3.0 to 3.6-V supply voltage. Xilinx never publishes “typical” numbers, because they are of little use and can be misleading.

I/O Pin-to-Pin Parameters

➤ Input set-up time (with zero hold time guaranteed) on page 4-78.

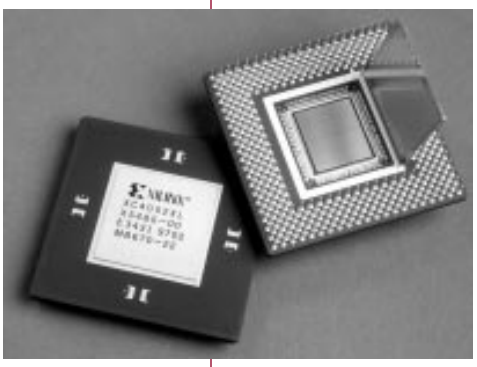
➤ Clock input to output data delay on page 4-77.

The sum of these two parameters defines the clock period for inter-chip communication.

I/O electrical characteristics are described in *I/O Characteristics of the ‘XL FPGAs*, on page 13-13, covering 5-V tolerance, PCI compliance, sink and source I/V curves, and the effect of capacitive loading.

On-chip Performance

The delay through a 4-input look-up table (page 4-74) is the shortest logic delay (1.2 to 2.7 ns). It is independent of the complexity of the equation. (For example, three cascaded XORS are as fast as a single inverter.) Other parameters describe the flip-flop set-up time of 0.6 to 1.1 ns (either through a 4-input look-up table or bypassing it) and the internal clock-to-out delay of 1.5 to 2.1 ns.



RAM

Any 4-input look-up table can be used as a 16x1 RAM, and two tables can be combined to be a 16x1 dual-port RAM. The write operation can be made synchronous; the 16 locations can be written into as if they were flip-flops. Note that the XC4000XL devices do not have any pulse-width constraints in their synchronous clocking. (The restrictive note on page 4-15 does not apply to any XC4000XL device.)

Dedicated Carry

A dedicated carry structure simplifies adders, subtractors, comparators, accumulators, and counters, and makes them faster; a 32-bit accumulator can run at 60 MHz.

Interconnect Resources

The XC4000XL family has considerably more interconnect resources than the 5-V XC4000E family, although both families use identical logic structures. Interconnect delays can be a short as 0.1 ns (between neighbors) or more than 20 ns when the signal has to

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pass through many intermediate switching points. Interconnect delays are not listed in the data sheet, but they are reported with 0.1 ns accuracy by the design software. You can constrain the software to achieve a specified maximum delay for any path in your design. This method can make interconnect delays as predictable as logic delays.

Available Package Options

Available package/device type options are listed on page 4-147. Note that Xilinx offers many chips in the same package with identical footprints. This makes it easy to migrate to a larger or smaller device when features must be added or deleted.

Page 4-111 lists the specific pin-outs per device type and package.

Configuration Modes

There are six ways to load configuration data into the device, as described in **FPGA Configuration Guidelines** on page 13-31. The most popular mode is master serial mode, described in detail on page 4-62. The device is configured from data stored in a Xilinx serial PROM as described in section 5. Page 4-50 lists the number of configuration bits required, while pages 5-2 and 5-12 list the number of bits available in the different SPROM devices.

Power Consumption

Static power consumption is negligible, just a few milliwatts. Dynamic power consumption is proportional to the clock frequency, and is thus design dependent.

The typical dynamic power ranges from milliwatts for small devices at low clock rates, to several watts for large devices clocked at 50 to 100 MHz. When compared to competing devices, the XC4000XL family uses less power because of its 3.3-V supply voltage and because of its segmented routing structure that minimizes interconnect capacitance.

Xilinx guarantees the performance parameters up to a junction temperature of 85°C (commercial grade), and provides a de-rating factor of 0.35% per degree C for junction temperatures up to 125°C in plastic packages.

The junction temperature can be calculated from the power consumption and the ambient temperature by using the package-dependent values for thermal impedance, with and without airflow, as printed on page 10-5. ◆

Application Notes

The XC4000XL architecture is a functional superset of the XC4000E architecture, which in turn is a superset of the original XC4000 architecture. All application notes written for any of these families are applicable to the XC4000XL. The following examples are all available at http://www.xilinx.com/apps/4000.htm:

XAPP080: Supply-voltage Migration, 5V to 3.3V

XAPP088: I/O Characteristics of the XL FPGAs

XAPP065: XC4000 Series Edge-Triggered and Dual-Port RAM Capability

XAPP057: Using Select-RAM Memory in XC4000 Series FPGAs

XAPP056: System Design with New XC4000X I/O Features

XAPP051: Synchronous and Async. FIFO Designs

XAPP052: Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators

XAPP013: Using the Dedicated Carry Logic in XC4000E

XAPP023: Accelerating Loadable Counters in XC4000

XAPP018: Estimating the Performance of XC4000E Adders and Counters

XAPP014: Ultra-Fast Synchronous Counters

XAPP010: Bus-Structured Serial Input/Output Device

XAPP009: Harmonic Frequency Synthesizer and FSK Modulator

XAPP008: Complex Digital Waveform Generator 16-Tap, 8-Bit FIR Filter

XAPP054: Constant Coefficient Multipliers for the XC4000E

XAPP055: Block Adaptive Filter

XAPP062: Design Migration from XC4000 to XC4000E

XAPP015: Using the XC4000 Readback Capability

XAPP079: 4MBit Virtual SPROM

XAPP017: Boundary Scan in XC4000 and XC5200 Series Devices

XAPP011: LCA Speed Estimation: Asking the Right Question

Using Programmable Logic to Accelerate DSP Functions. A Guide to Using Programmable Gate Arrays for Application-Specific DSP Performance

Building High Performance FIR Filters Using KCMs

The Fastest FFT in the West

The Fastest Filter in the West

Plug and Play ISA in Xilinx FPGAs

Dynamic Microcontroller in XC4000

Pulse-Width Modulation in Xilinx

Configuring Mixed FPGA Daisy Chains

XC4000/XC5200 PC84 Footprint Compatibility