Cisco Systems
Using the XC4036XL

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Cisco Systems is the worldwide leader in networking for the Internet. We recently developed a new ESCON Channel Port Adapter that allows mainframe computers to connect to our Cisco 7200 Router Family. Xilinx FPGAs helped us create a very successful product.

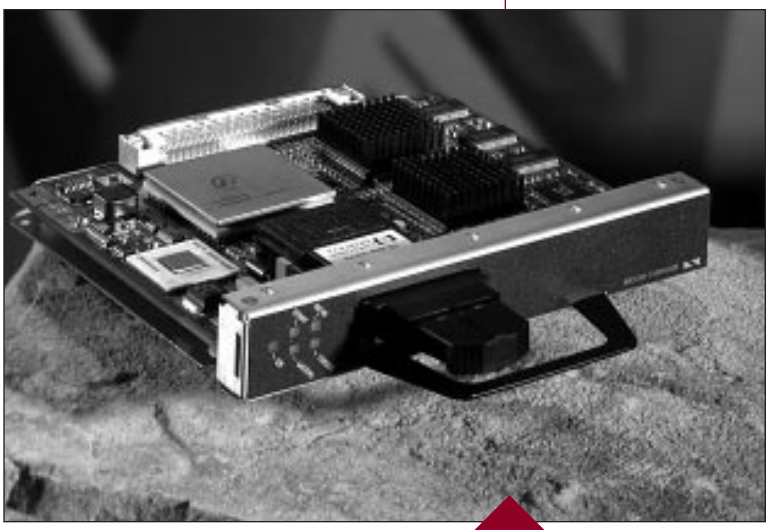
The first prototype of our system did not use Xilinx FPGAs. However, one of the critical elements of our design is a dual-port FIFO, and we could not achieve the speed we needed or keep the power consumption within limits using a non-Xilinx device. So, we had to look for a lower-power, higher-performance alternative.

After a careful evaluation, we chose the Xilinx XC4036XL for five reasons:

1. **3.3-V operation.** We were able to achieve much lower power consumption.
2. **Device performance.** The XC4036XL meets all of our speed requirements.
3. **Dual-port RAM capability**. The Xilinx RAM allowed us to create an efficient, high-performance FIFO that we could not create with the previous FPGAs we tried to use.
4. **Very flexible I/O structure**. The dual IOB flip-flops provide high-speed bi-directional bus capability.
5. **Flexible clock structure**. We used three separate clocks in our design, which were well supported by the XC4036 architecture.

My design team — Joydeep Chowdhury, Marc Edwards, Bill Harris, and Jeff Kidd — needed to pack a 50-MHz system controller, a DRAM controller, and two FIFOs into the device. Although we had never used Xilinx FPGAs before, we were able to complete a working design within about two months.

Using Xilinx SelectRAM, it was easy for us to implement both shallow and wide FIFOs that met our requirements. The XC4036 did a great job for us, and the FIFOs were a "piece of cake." The Xilinx architecture is well suited to creating high performance FIFOs.



We created our design using Verilog with a Synplicity design flow, doing both RTL and gate-level simulation. The local Xilinx FAEs helped us implement the design using the Xilinx Alliance Series software. The design phase went very smoothly. Although we did call the FAEs several times because we were new to Xilinx, we quickly resolved all of the issues. ◆

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