XC4000 Series Select-RAM Memory:

Advantages and Uses

The XC4000 Series of FPGA devices (i.e., the XC4000E and XC4000EX families, and their low-voltage counterparts, the XC4000L and XC4000XL families) includes several architectural improvements over the highly-successful XC4000 FPGA family. One of the most important new features is Select-RAM™ memory. Select-RAM memory can be defined as the capability of programming the look-up tables in Configurable Logic Blocks (CLBs) as ROM or as single- or dual-port RAM, with edge-triggered (synchronous) or level-sensitive (asynchronous) timing. Select-RAM memory also can be initialized to a known value in all RAM and ROM modes.

Select-RAM memory is unique in its range of options and ability to deliver high-speed dual-port memory. The advantages of the Select-RAM capability include flexibility, increased ease-of-use, shorter design cycles and increased performance.

Flexibility

Clearly, the options of edge-triggered or level-sensitive and single-port or dual-port RAM provide a wide selection of choices for the designer. The distributed nature of the RAM, which is implemented in individual CLBs, also contributes to the flexibility of Select-RAM memory. Only sufficient CLBs to implement a given memory block need be allocated as RAM: the memory block size can be scaled to exactly match the requirements of the application. Each RAM block can be placed close to related logic. There is no need to consume a large block of dedicated memory to implement a small RAM function, nor to route control and data lines across the device to reach such dedicated blocks. Each CLB can be individually configured, so the designer can "mix and match" RAM modes. Select-RAM is the most flexible memory implementation available in an FPGA today.

Ease of Use

Traditional RAM capability, now referred to as the level-sensitive or asynchronous option to Select-RAM memory, has never been simple to use. Meeting the required timing relationships often involved careful layout and detailed timing analysis. To guarantee correct behavior, a 2X clock is typically required, in order to generate the Write Enable during the third quadrant of the write clock cycle. This type of RAM is the only available option in the original XC4000 family devices.

None of these delicate timing relationships need be maintained when using one of the edge-triggered Select-RAM modes available in XC4000-Series devices. Instead, writing to a memory block is just like writing to a data register: set up the address and data, enable the RAM and apply the effective clock edge. A conceptual model for a Select-RAM block in edge-triggered mode is shown in the **Figure 1**.

The ability to initialize RAM, as well as ROM, as part of device configuration eliminates the need for logic to perform that initialization. Reduced logic results in smaller, simpler and more reliable designs.

All of the Select-RAM options are directly and easily implemented using any of the schematic entry, MemGen memory block generator tool, X-BLOX™ schematic-based synthesis, or HDL synthesis design environments. Detailed information on how to use these tools to implement Select-RAM is available in the new Xilinx application note "Using Select-RAM Memory in XC4000 Series FPGAs."

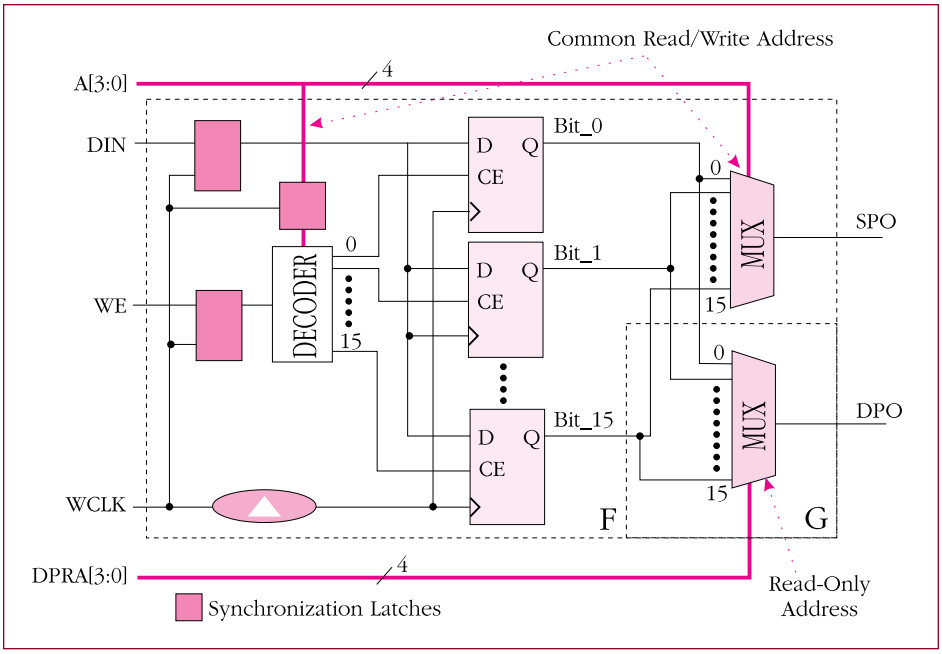

Figure 1: *XC4000 Series Conceptual Model for Edge-Triggered Memory*

Shorter Design Cycles

The ease-of-use associated with edge-triggered memory design results in shorter design cycles as compared to using level-sensitive RAM. The design, simulation and testing steps are all simplified.

Performance

As mentioned above, level-sensitive RAM designs may require both a 2X clock and significant signal manipulation to meet the stringent timing requirements on the Write Enable signal. The Address and Data inputs must be set-up at the RAM input pins by the time the Write Enable signal arrives, typically halfway through the write cycle.

When the same design is implemented using edge-triggered RAM, Address and Data may change in response to (for example) the rising edge of the input clock. The Write can occur on the next rising edge of the same clock. Therefore, the Address and Data have the full write cycle to set-up at the RAM input pins. The result is a memory block that operates at approximately twice the speed of the level-sensitive version of the design. When the simultaneous read/write capability of the dual-port Select-RAM option is taken into account, data throughput can be doubled again, resulting in a total four-fold increase in effective data rates. These results are demonstrated in a simple FIFO design in the Xilinx application note "Implementing FIFOs in XC4000 Series RAM."

Distributed RAM provides an additional speed advantage: locating RAM blocks closer to related logic minimizes routing delays on critical paths.

Uses of Select-RAM Memory

The edge-triggered RAM capability can and should be used in all new designs requiring RAM. These applications include register files, FIFO buffers, multipliers, shift registers and pseudo-random sequence generators.

The dual-port option adds the ability to read and write simultaneously from two different addresses. This ability considerably simplifies FIFO designs and is useful for constructing dual-port register files. ◆

The Application Notes referenced in this article are available on the Xilinx WebLINX web site at www.xilinx.com, or by contacting the Xilinx Technical Hotline.